MPC8572E PowerQUICC® III Processor

Evolutionary and Revolutionary

Freescale's next-generation PowerQUICC[®] III integrated communications processors are designed to provide solutions for symmetric and asymmetric multicore systems. Based on the scalable e500 system-on-chip (SoC) platform built on Power Architecture[®] technology, they deliver dual-core gigahertz-plus communications processing performance with advanced content processing and security features.

The MPC8572E family of processors is designed to offer clock speeds from 1.067 GHz up to 1.5 GHz, combining two powerful processor cores, enhanced peripherals and high-speed interconnect technology to balance processor performance with I/O system throughput. These processors also contain an application acceleration block that integrates four powerful engines: a table lookup unit (TLU) that offloads complex table searches and header inspections, a pattern-matching engine (PME) to handle regular expression matching, a deflate engine to manage file decompression, and a security engine that accelerates crypto operations in IPSec and SSL/TLS for virtual private networks.

Based on Freescale's 90 nm silicon-on-insulator (SOI) copper interconnect process technology, the MPC8572E is designed to deliver higher performance with lower power dissipation. The MPC8572E processors provide a significant performance increase and represent the next step in continuous innovation from the popular PowerQUICC family. With uncompromising integration, the MPC8572E platform builds on the embedded core performance of Power Architecture technology and adds new features to enhance traffic management and security acceleration.

Support for high-speed interfaces on the MPC8572E enables scalable connectivity to

network processors and/or ASICs in the data plane while the MPC8572E platform handles complex, computationally demanding control plane processing tasks. These processors also include a next-generation double data rate (DDR2/DDR3) memory controller, enhanced Gigabit Ethernet support, double precision floating point and an integrated security engine.

Key Features

- Dual integrated DDR2/DDR3 memory controllers for memory technology future proofing
- Pattern-matching engine
- Four integrated Ethernet controllers (enhanced TSEC) with IEEE[®] 1588 support and lossless flow control
- Flexible high-speed interfaces
 - Serial RapidIO[®]
- PCI Express[®]





MPC8572E Block Diagram



Wide Range of Features for Multiple Target Applications

The robust feature set and advanced integration found on the MPC8572E family of processors provides an optimal communications processing solution for applications such as multi-service routing and switching, firewall/VPN, unified threat management, intrusion detection and prevention, antivirus, load balancing, content switching and application-aware networking equipment. The next-generation architecture also addresses the computationally demanding processing requirements of wireless infrastructure equipment, such as radio node controllers and WiMAX and LTE base stations.

The combination of highly efficient, highfrequency cores with a large 1 MB L2 cache makes the MPC8572E an ideal choice for control plane applications. These applications have a relatively lower level of parallelism and thus are better suited to run on processors with fewer but higher performance cores. SMP scaling efficiency drops off with additional cores due to inter-core handshaking, therefore the performance of the control plane application suffers on devices that rely on aggregating many cores together to achieve performance.

The hardware-based PME enables deep packet inspection with a performance and power level impossible with software-only solutions. DPI applications such as intrusion detection and prevention, antivirus and antispam and load balancers benefit greatly from the PME.

MPC8572E Technical Specifications

- Dual embedded e500 cores, up to 1.5 GHz
 6897 MIPS at 1500 MHz
 - (estimated Dhrystone 2.4)
- 36-bit physical addressing
- Enhanced hardware and software debug support
- Double-precision floating point unit

- Memory management unit
- L1/L2 cache
 - L1 cache—32 KB data and 32 KB instruction cache with line-locking support
 - Shared L2 cache-1 MB with ECC
 - L1 and L2 hardware coherency
 - L2 configurable as SRAM, cache and I/O transactions can be stashed into L2 cache regions
- Integrated dual 64-bit DDR memory controller with full ECC support, supporting up to 400 MHz clock rate (800 MHz data rate):
 - 1.8V SSTL, DDR2 SDRAM
 - 1.5V SSTL, DDR3 SDRAM
- Application acceleration platform
 - Advanced TLU
 - Integrated security engine supporting DES, 3DES, MD-5, SHA-1/2, AES, RSA, RNG, Kasumi F8/F9, ARC-4 encryption algorithms and XOR RAID acceleration
 - Integrated PME (Regular Expression)
 - Packet deflate engine
- Four on-chip, triple-speed Ethernet controllers supporting 10 and 100 Mbps, and 1 Gbps Ethernet/IEEE 802.3 networks with MII, RMII, GMII, SGMII, RGMII, RTBI and TBI physical interfaces and IEEE 1588
 - TCP/IP checksum acceleration and advanced Quality of Service (QoS) features
 - Lossless flow control
- 100Mb/s MII debug port
- General-purpose I/O
- Serial RapidIO and PCI Express high-speed interconnect interfaces
- On-chip network (OCeaN) switch fabric
- 150 MHz, 32-bit, 3.3V I/O, local bus with memory controller
- Dual integrated DMA controller
- Dual I²C and DUARTS
- Programmable interrupt controller
- IEEE 1149.1 JTAG test access port
- 1.1V core voltage with 3.3V/2.5V/1.8V/1.5V I/O
- 1023-pin FC-PBGA package

MPC8572E Partner Ecosystems

Operating System Support

- Enea OSE
- Green Hills INTEGRITY[®]
- Linux®
- MontaVista professional grade Linux and carrier grade Linux
- QNX Neutrino[®]
- Wind River VxWorks® and Linux

Evaluation Boards

Freescale ATX form factor

Development

- Abatron BDI3000 probe
- CodeSourcery G++ compiler
- CodeWarrior[™] Development Studio
- CodeWarrior Ethernet TAP
- CodeWarrior USB TAP
- Green Hills MULTI® IDE
- Green Hills probe
- Lauterbach TRACE32 probe
- Wind River ICE probe
- Wind River Workbench IDE

Models

- Virtutech Simics functional simulator
- Mentor Graphics Seamless co-verification
- Freescale instruction set simulator

Application Software: VortiQa™ for Enterprise

- Stateful firewall and NAT
- IPsec virtual private network (VPN)
- Intrusion prevention system (IPS) and deep packet inspection
- Antivirus/anti-spam detection and prevention (AntiX)
- · QoS and traffic management
- High Availability
- More information at www.freescale.com/vortiqa

Training Classes

- Arnewsh
- Phoenix Micro

Learn More:

For current information about Freescale products and documentation, please visit **www.freescale.com**.



Freescale and the Freescale logo are trademarks or registered trademarks of Freescale Semiconductor, Inc. in the U.S. and other countries. All other product or service names are the property of their respective owners. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org. © Freescale Semiconductor, Inc. 2009. Document Number: MPC8572FS BEV 4 rademarks or registered trademarks of Freescale Ser