Generator for PowerQUICC III

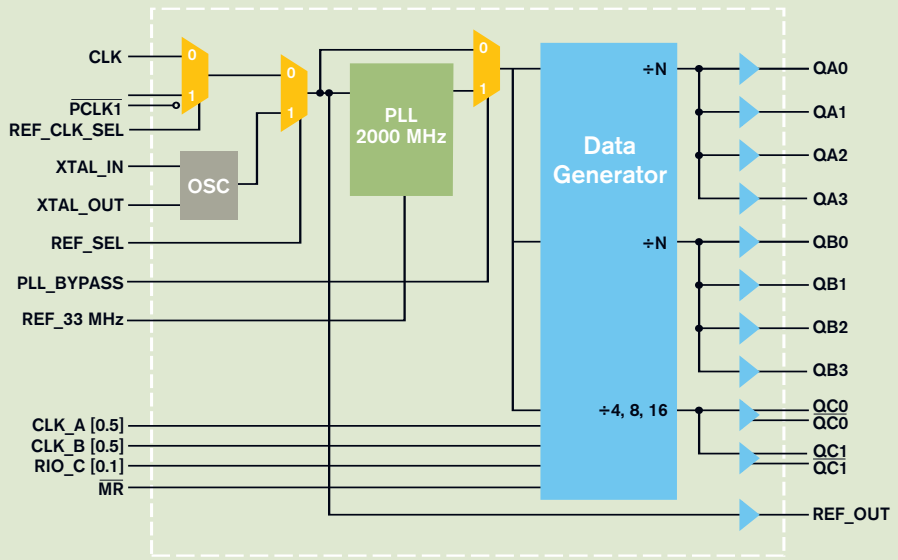
MPC9850 QUICCclock

The Freescale MPC9850 QUICCclock, a PLL based clock generator, has been specifically designed as a single-chip solution to the clock requirements for the PowerQUICC III™ processor. This device provides the microprocessor system clock, a 500 MHz RapidIO clock, as well as a Gigibit Ethernet PHY.

The reference input for the MPC9850 is supplied from a 25 or 33 MHz reference oscillator or derived from a 25 MHz crystal using the internally provided oscillator. The high frequency PLL multiplies the reference to 2000 MHz where dual programmable dividers provide two system frequencies. These two frequencies may be selected from a list of common microprocessor system frequencies ranging from 16 thru 250 MHz.

The MPC9850 offers a total of eight low skew clock outputs organized into two LVCMOS output banks. An additional bank of two LVDS outputs are RapidIO compatible and can be configured for 125, 250 or 500 MHz. In addition, the input reference frequency is buffered for use as a Gigibit Ethernet PHY clock and the extended temperature range of the MPC9850 QUICCclock supports telecommunication and networking requirements. All these high performance features are designed into a single low cost package – the 100-lead MAPBGA.

MPC9850 BLOCK DIAGRAM



Designed using Freescale's high-speed SiGe:C technology, the MPC9850 QUICCclock offers telecommunication and networking equipment designers a single chip clocking solution to support microprocessor and microcontroller applications. This device offers designers a wide range of available output frequencies to match most user microprocessor system configurations for Freescale's PowerQUICC III, as well as PowerPC™ families of microprocessors.

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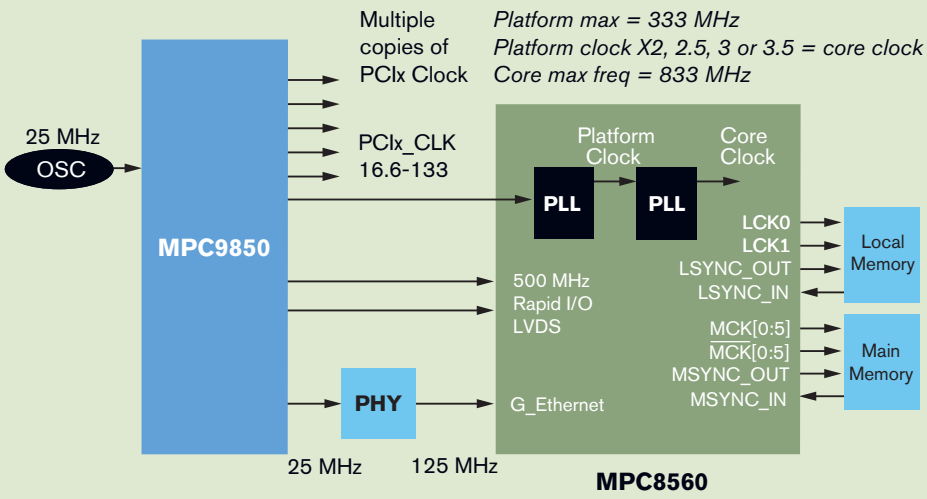
POWERQUICC™ III – MPC8560 WITH MPC9850



Clock Generator for PowerQUICC III

The high performance Freescale PowerQUICC III technology requires clock generation techniques that are based upon careful IC design and advanced technology. The MPC9850 QUICCclock provides accurate clock requirements such as low jitter and maximized clock performance.

The MPC9850 IC, designed for the PowerQUICC III processor, is a single-chip PLL based device generating a microprocessor input clock. This clock is multiplied by internal MPC8560 PLL circuitry to provide the high frequency core clocks achieving high CPU performance in the PowerQUICC III.

In addition, the MPC9850 has differential LVDS outputs used to clock the high speed RapidIO data interface at speeds up to 500 MHz. A 25 MHz reference at the QUICCclock buffered output provides the input to most Gigibit Ethernet PHY's.

For PowerQUICC III applications, memory clocks are provided through DLL (delay lock loop) circuitry on the MPC8560. However, non-PowerQUICC III applications utilize the two banks of LVCMOS outputs to provide multiple copies of the system clock for memory applications.

Key Features

> Clock generator for PowerQUICC III system and RapidIO clocks

> 25 MHz or 33 MHz reference input

> External oscillator or 25 MHz crystal

> 8 LVCMOS in two output banks

> 2 LVDS outputs for RapidIO

> VCO = 2000 MHz

> System output = 250, 200, 166, 133, 125, 111, 100, 83, 66, 50, 33, 25 or 16 MHz

> RapidIO = 500, 250 or 125 MHz LVDS

> Gigibit Ethernet PHY applications

> Low cycle-to-cycle and period jitter

> 3.3V core with 2.5 or 3.3V output supply

> Package = 100-lead MAPBGA, 1.0 mm pitch

> Ambient temp = -40° to 85° C

Learn More: For more information about Freescale products, please visit www.freescale.com

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