RapidIO™

Interconnect Architecture for Networking

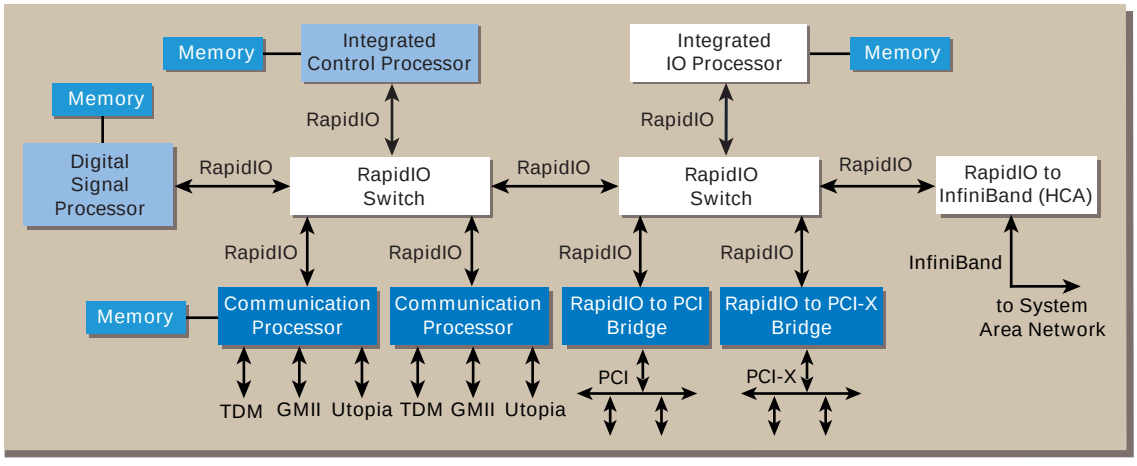
The RapidIO™ architecture is an electronic data communications standard for interconnecting chips on a circuit board and interconnecting circuit boards using a backplane. This new high-performance, packet-switched interconnect technology was designed for embedded systems, primarily for the networking and communications markets. Industry leaders in networking, communications, semiconductors, and embedded systems are founding the RapidIO Trade Association to develop and support this new open standard.

An important bottleneck in networking and communications equipment is the speed at which the various components "inside the box" communicate with each other. The RapidIO architecture eliminates this bottleneck. Current equipment is limited to hundreds of Mbits per second transfer rates using legacy bus technologies such as PCI. The new RapidIO interconnect will increase this bandwidth significantly. Many believe that increases in bandwidth have already replaced increases in microprocessor performance as the key requirement for higher-performance Internet technology.

Designed for Networking and Communications Equipment

Designed for networking and communications equipment, enterprise storage, and other high-performance embedded markets, the RapidIO architecture addresses the demand for higher performance networking equipment for use in the Internet infrastructure. Other bus technologies such as PCI, PCI-X and InfiniBand are targeted at the desktop PC and server computer markets. RapidIO architecture offers the bandwidth, software independence, fault tolerance, and low latency required in the networking market.

The RapidIO specification defines a high-performance interconnect architecture designed for passing data and control information between microprocessors, DSPs, communications and network processors, system memory, and peripheral devices within a system. It was designed to replace current processor and peripheral bus technologies such as PCI and proprietary processor buses. The initial RapidIO specification defines physical layer technology suitable for chip-to-chip and board-to-board communications across standard printed circuit board technology at throughputs exceeding 10 Gbits per second utilizing low voltage differential signaling, (LVDS) technology. Unlike other next-generation I/O technologies, RapidIO technology is transparent to application software, and does not require special device drivers. Additionally, it has no impact on operating system software. The RapidIO Interconnect can also be a bridge to other bus technologies such as PCI, PCI-X, and system area networks like InfiniBand. A rich variety of features are provided in the RapidIO interconnect including high data bandwidth capability and support for high-performance I/O devices, as well as providing globally shared memory, message passing, and software managed programming models.



Designed for Networking and Communications Equipment

A Partitioned Architecture

The RapidIO standard is a packet-switched interconnect architecture conceptually similar to internet protocol (IP). However, the RapidIO architecture is designed to be used for the processor and peripheral interface where high bandwidth and low latency are crucial. The RapidIO architecture is partitioned into a three-layer hierarchy of logical, transport, and physical specifications, which allows scalability and future enhancements while maintaining compatibility.

RapidIO Features

Higher Bandwidth

Initially, the RapidIO interconnect is designed to provide 10 Gbits per second aggregate device bandwidth using 8-bit wide input and output data ports. The LVDS technology used by the RapidIO interconnect has the capability to scale to multi-GHz speeds, and the port width can scale to 16-bits and possibly wider in the future.

Low Latency

High frequency and low packet overhead provides a much narrower interconnect that still offers better latency than bus technologies like PCI and PCI-X.

Transparent to Existing Software Base

The RapidIO architecture supports all needed microprocessor and I/O transactions. It is transparent to existing applications and operating system software, and provides a flexible method for memory mapping systems.

Error Management Support in Hardware

The RapidIO interconnect is able to recover from all single bit errors and most multi-bit errors with no software or higher-level system intervention. It can detect and notify software in the event of more severe errors in order to redirect traffic around failed devices in high reliability applications.

Small Silicon Footprint

The RapidIO interconnect was designed to have a minimum silicon footprint for low cost, full custom ASIC or FPGA based designs. The logic required to implement a RapidIO endpoint is similar in scale to a PCI-X endpoint.

Widely Available Process and I/O Technologies

The RapidIO interconnect is designed for common .25 and .18 micron CMOS technology. The LVDS drivers and receivers have been standardized in the industry through IEEE. LVDS driver technology is commonly available on standard ASIC and FPGA offerings. Full duplex communications is provided between devices. Transmission distances up to 30 inches over standard printed circuit board traces are targeted.

Multiprocessing Support

Hardware supported symmetric multiprocessing is provided through an optional distributed shared-memory extension. Distributed shared memory is used pervasively in the computer workstation and server markets, and is becoming more popular in high-performance embedded applications. Distributed shared memory is also useful for maintaining cache coherency for a single processor in systems with distributed memory controllers.

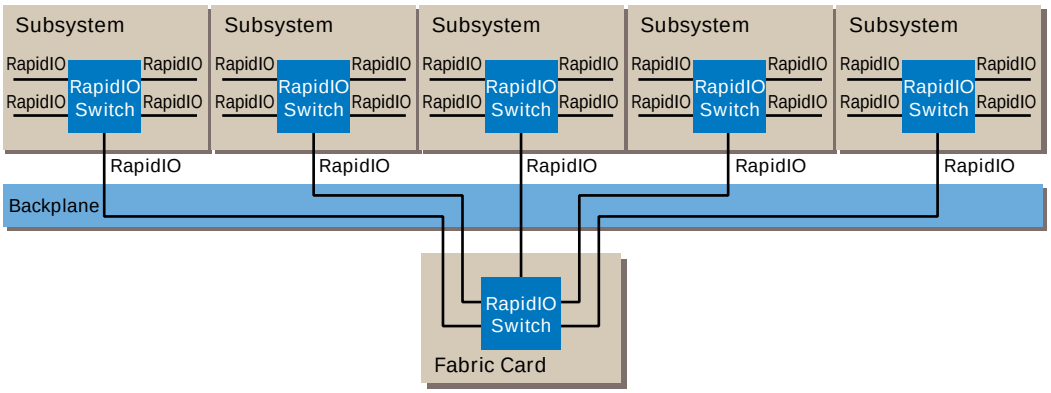
Flexible Topologies

Various topologies are supported by the RapidIO architecture such as star, linked star, and mesh.

An Open Standard

In addition to the technical requirements, the high-performance embedded market requires an open standard interconnect. Currently the market suffers from an overabundance of proprietary buses, requiring standard product and ASIC-based bridges to connect the various devices in the system. The RapidIO interconnect provides a common connection architecture for general purpose RISC processors, digital signal processors, communications processors, network processors, memory controllers, peripheral devices, and bridges to legacy buses. This efficient architecture benefits users by reducing cost, time-to-market, and complexity. The RapidIO architecture will be an open standard and will be available to any company that joins the RapidIO Trade Association. Members of the RapidIO Trade Association are expected to offer RapidIO products including various processors, bridges and switch fabric devices.

RapidIO in a Backplane Application



Contact Information

For more information on the RapidIO interconnect architecture and how to join the RapidIO Trade Association visit –

www.RapidIO.org