SPI-based LIN communication opening up new horizons

NXP® SJA1124 SPI to Quad-LIN Bridge

By decoupling MCU selection from the number of LIN channels the SJA1124 offers unprecedented cost and board space savings in multi-channel LIN applications.

GENERAL DESCRIPTION

The SJA1124 is an SPI to Quad-LIN Bridge incorporating four LIN master channels. Each LIN master channel contains a LIN controller and LIN transceiver with master termination.

LIN data communication is accomplished via SPI. The SJA1124 converts the transmit data stream received on the SPI input into LIN master frames on the LIN bus. The data stream received on the LIN bus can be read via SPI. The SPI replaces the UART-related TXD and RXD pins on the MCU. A complete LIN frame can be transmitted in a one single SPI operation.

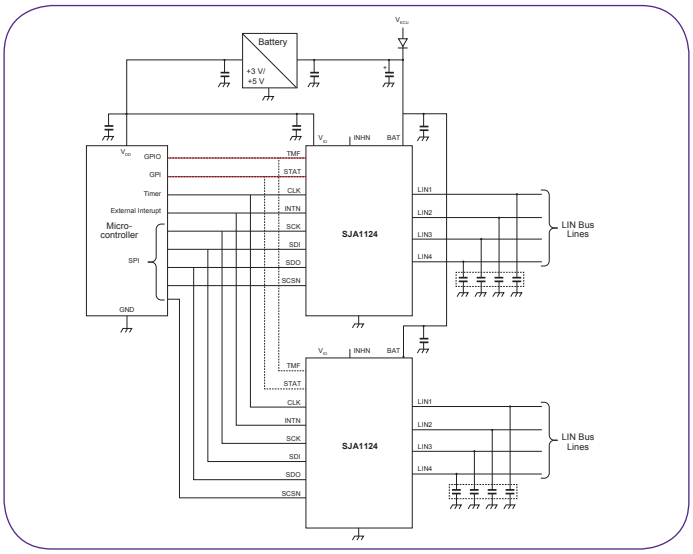
The on-chip LIN controllers allow the use of smaller, mainstream low-pin-count MCUs. Performance becomes the primary selection criteria, rather than the number of LIN communication channels. Decoupling the MCU from the channel count not only allows it to be tailored to performance requirements, it also enhances scalability. Adding four additional LIN channels with a second SJA1124 requires only an additional chip select pin on the MCU.

The SJA1124 is ideally suited to multi-LIN master applications, such as body control and ambient mood lighting. The integrated master termination further reduces the BOM and board space requirements.

APPLICATIONS

- Body control
- HVAC
- Ambient mood lighting
- Park assist

SJA1124 APPLICATION DIAGRAM



KEY FEATURES

General

- ISO 17987 (LIN2.x)/SAE J2602 compliant LIN master controller and LIN transceiver
- Serial Peripheral Interface (SPI) for LIN data transfer, configuration, control and diagnosis
- Synchronous LIN frame transmission across multiple SJA1124 devices
- Interrupt output with configurable interrupt sources
- Leadless DHVQFN24 package (3.5 x 5.5 mm)

LIN master controller

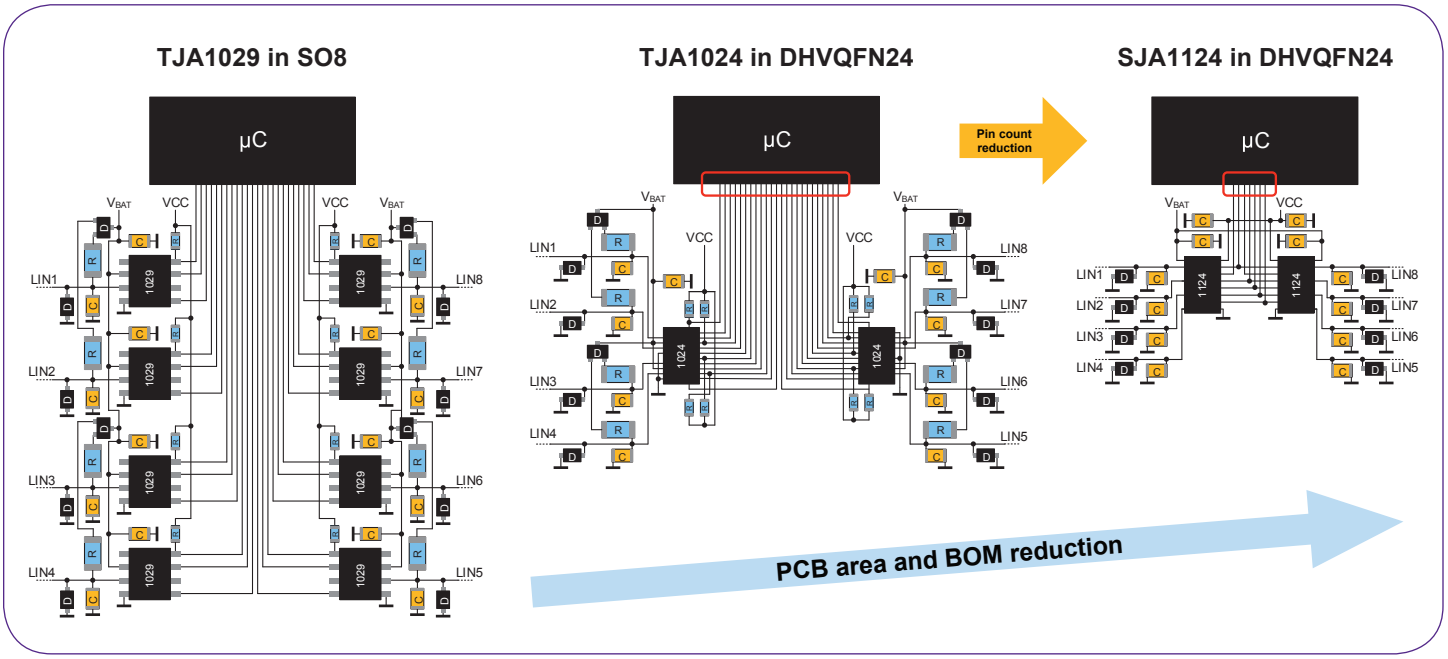
- AUTOSAR compatible
- Baud rate, operating mode, status and interrupt processing configurable per LIN channel
- Complete LIN message handling
- One interrupt per LIN message

An overview of NXP's multi-LIN transceiver portfolio is given in the table below.

NXP MULTI-LIN TRANSCEIVER PORTFOLIO

Function / Feature	TJA1022	TJA1024	TJA1124	SJA1124
# LIN channels	2	4	4	4
ISO 17897 (LIN 2.x) / SAE-J2602 compliancy	✓	✓	✓	✓
Master termination (resistor + diode)	x	x	✓	✓
SPI to LIN bridge (replacing TxD / RxD pins)	x	x	x	✓
High-speed LIN	x	x	x	100 kBd
Microcontroller interface	3V3 and 5 V	3V3 and 5 V	3V3 and 5 V	3V3 and 5 V
INHN	x	x	✓	✓
TxD dominant time-out function	✓	✓	✓	✓
Wake-up source recognition	✓	✓	✓	✓
Battery supply voltage range	5 V - 18 V	5 V - 18 V	5 V - 28 V	5 V - 28 V
Max. voltage pins BAT and LIN	+ 42 V	+ 42 V	+ 43 V	+ 43 V
ESD (pin LIN)				
Human Body Model	± 8 kV	± 8 kV	± 6 kV	± 6 kV
According to IEC61000-4-2	± 6 kV	± 6 kV	± 6 kV	± 6 kV
Package (supporting AOI)	HVSON14 (3.0 mm x 4.5 mm) SO14 (3.9 mm x 8.65 mm)	DHVQFN24 (3.5 mm x 5.5 mm)	DHVQFN24 (3.5 mm x 5.5 mm)	DHVQFN24 (3.5 mm x 5.5 mm)

SJA1124 – WHEN SIZE REALLY MATTERS



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