NXP Semiconductors
Application Notes

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i.MXRT1060 Product Lifetime Usage Estimates

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1. Introduction

This document describes the estimated product lifetimes for the i.MX RT1060 applications processor based on the criteria used in the qualification process.

The product lifetimes described here are estimates and do not represent a guaranteed lifetime of the processor.

The i.MX RT series consists of an extensive number of processors that deliver a wide range of processing and multimedia capabilities across various qualification levels.

This document is intended to provide users with guidance on how to interpret the different i.MX RT1060 qualification levels in terms of the target operating frequency of the device, the maximum supported junction temperature (Tj) of the processor, and how this relates to the lifetime of the device.

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Each qualification level supported (Commercial and Industrial) defines a number of power-on hours (PoH) available to the processor under a given set of conditions, such as:

- The target frequency for the application (commercial and industrial).
  a) The target frequency is determined by the input voltage to the processor's core complex (VDD_SOC_IN).
  b) The use of the DCDC-enabled or DCDC-bypass mode.
     – When using the DCDC-bypass mode, the target voltage should not be set to the minimum specified in the datasheet. All power management ICs have allowable tolerances. The target voltage must be set higher than the minimum specified voltage to account for the tolerance of the PMIC. The tolerance assumed in the calculations in this document is +/-25mV.
     – The DCDC-enabled mode uses the DCDC module to generate power supply for the core logic on the i.MX RT series. These DCDC module is well characterized and can be set to output the exact minimum specified voltage. Longer power-on-hours can be achieved using the DCDC-enabled mode.
- The percentage of active use compare to standby.
  a) Active use means that the processor is running in an active performance mode.
     – For the commercial and industrial tiers, there are two performance modes available: 600 MHz and 528 MHz.
  b) In the DSM mode the datasheet defines lower operating conditions for VDD_SOC_IN, reducing the power consumption and junction temperature. In this mode, the voltage and temperature are set low enough so that the effect on the lifetime calculations is negligible and treated as if the device was powered off.
- The junction temperature (Tj) of the processor.
  a) The maximum junction temperature of the device is different for each tier of the product, e.g. 95oC for commercial and 105oC for industrial. This maximum temperature is guaranteed by final test.
  b) Users must ensure that their device is appropriately thermally managed such that the maximum junction temperature is not exceeded.

NOTE

All data provided within this document are estimates for PoH that are based on extensive qualification experience and testing with the i.MX RT series. These statistically derived estimates should not be viewed as a limit on an individual device's lifetime, nor should they be construed as a guarantee by NXP as to the actual lifetime of the device. Sales and warranty terms and conditions still apply.

2. Device qualification level and available PoH

Commercial qualification

Table 1 provides the number of PoH for the typical use conditions for the commercial device.

Table 1. **Commercial qualification lifetime estimates**

	ARM Core Speed (MHz)	Power-on Hours [PoH] (Hrs)	ARM Core Operating Voltage (V)	Junction Temperature [T_j] (^oC)
Case C1: DCDC Enabled	600	28,098	1.25	95
Case C2: DCDC Enabled	528	76,379	1.15	95
Case C3: DCDC Bypassed	600	21,883	1.275	95
Case C4: DCDC Bypassed	528	59,484	1.175	95

Figure 1 and Figure 2 establish the guidelines for estimating PoH as a function of CPU frequency and junction temperature. PoH can be read directly off the charts below to determine the necessary trade-offs to be made to CPU frequency and junction temperature to increase the estimated PoH of the device.

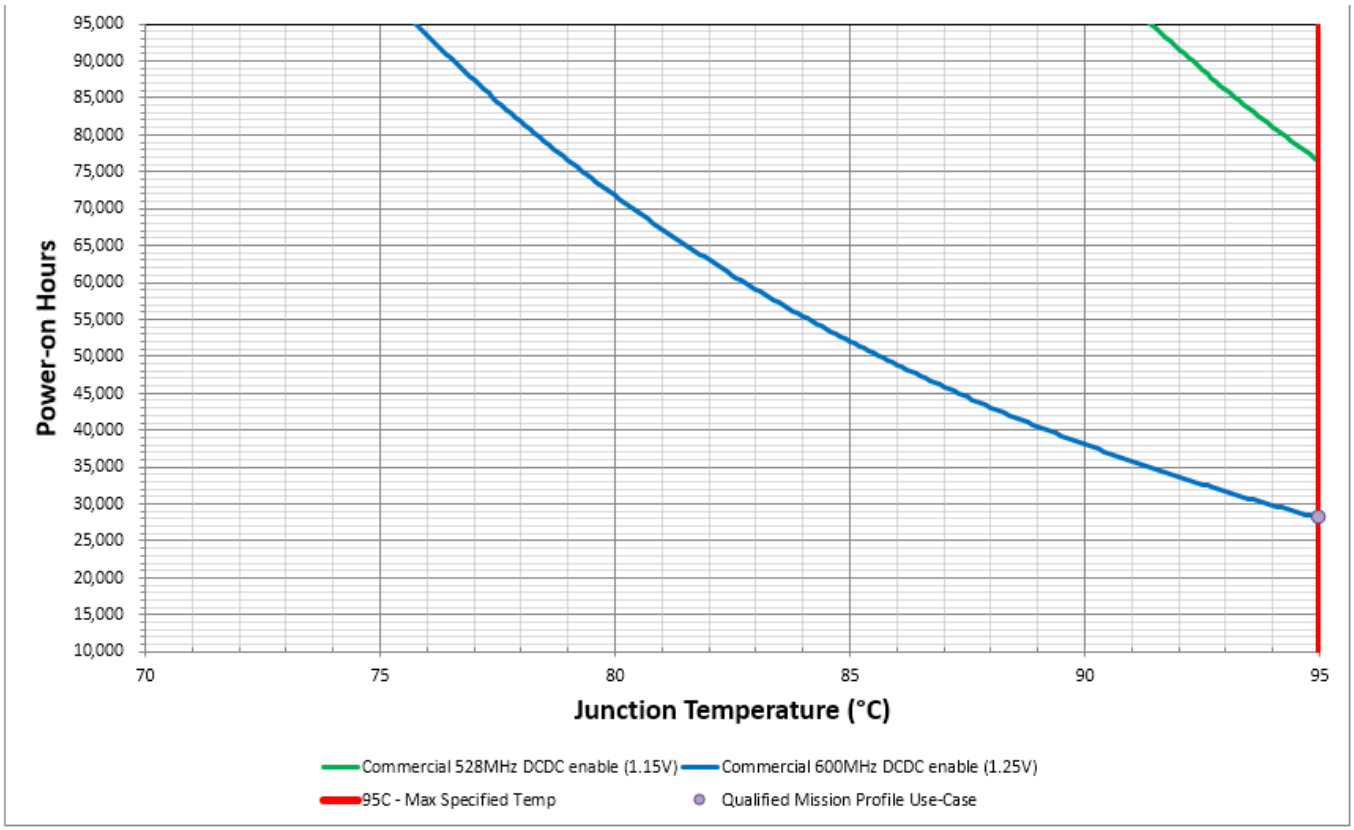

Figure 1. . i.MXRT1060 commercial lifetime estimates DCDC-enabled mode

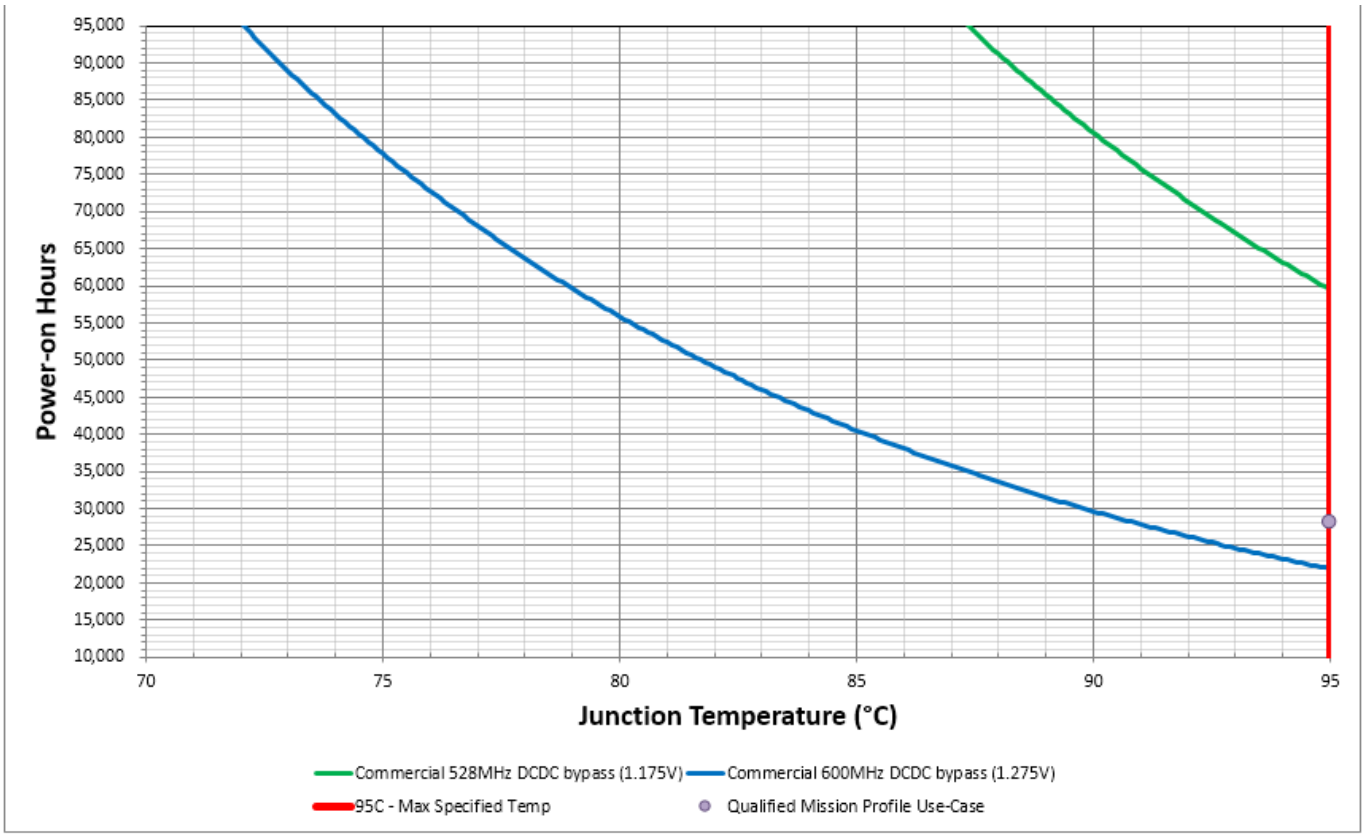

Figure 2. i.MXRT1060 commercial lifetime estimates DCDC-bypass mode

Industrial qualification

Table 2 provides the number of PoH for the typical use conditions for the industrial device.

Table 2. **Industrial qualification lifetime estimates**

	ARM® Core Speed (MHz)	Power-on Hours [PoH] (Hrs)	ARM Core Operating Voltage (V)	Junction Temperature [T_j] (^oC)
Case I1: DCDC Enabled	528	88,407	1.15	105
Case I2: DCDC Bypassed	528	68,851	1.175	105

Figure 3 and Figure 4 establish the guidelines for estimating the PoH as a function of CPU frequency and junction temperature. PoH can be read directly off of the charts below to determine the necessary trade-offs to be made to CPU frequency and junction temperature to increase the estimated PoH of the device.

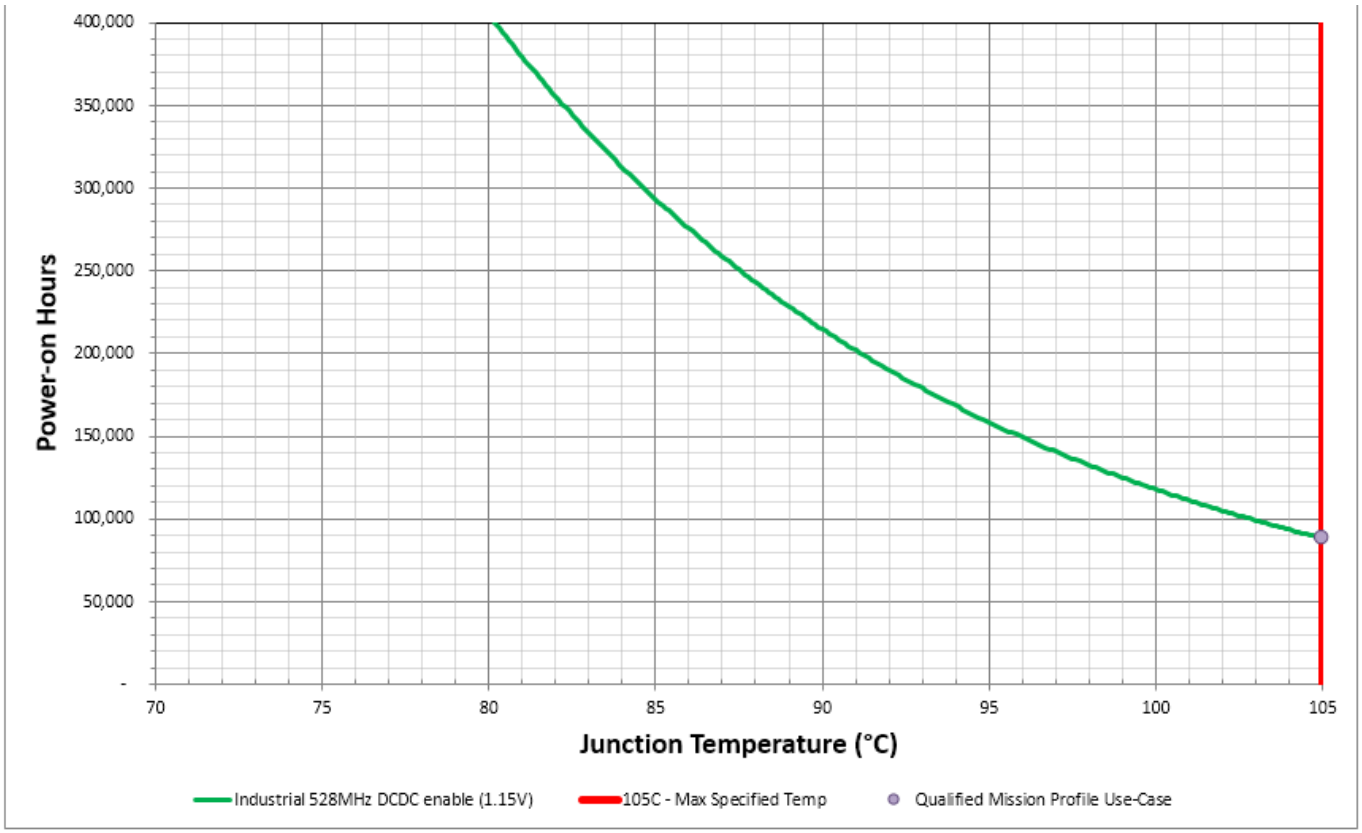

Figure 3. i.MXRT1060 Industrial lifetime estimates DCDC-enabled mode

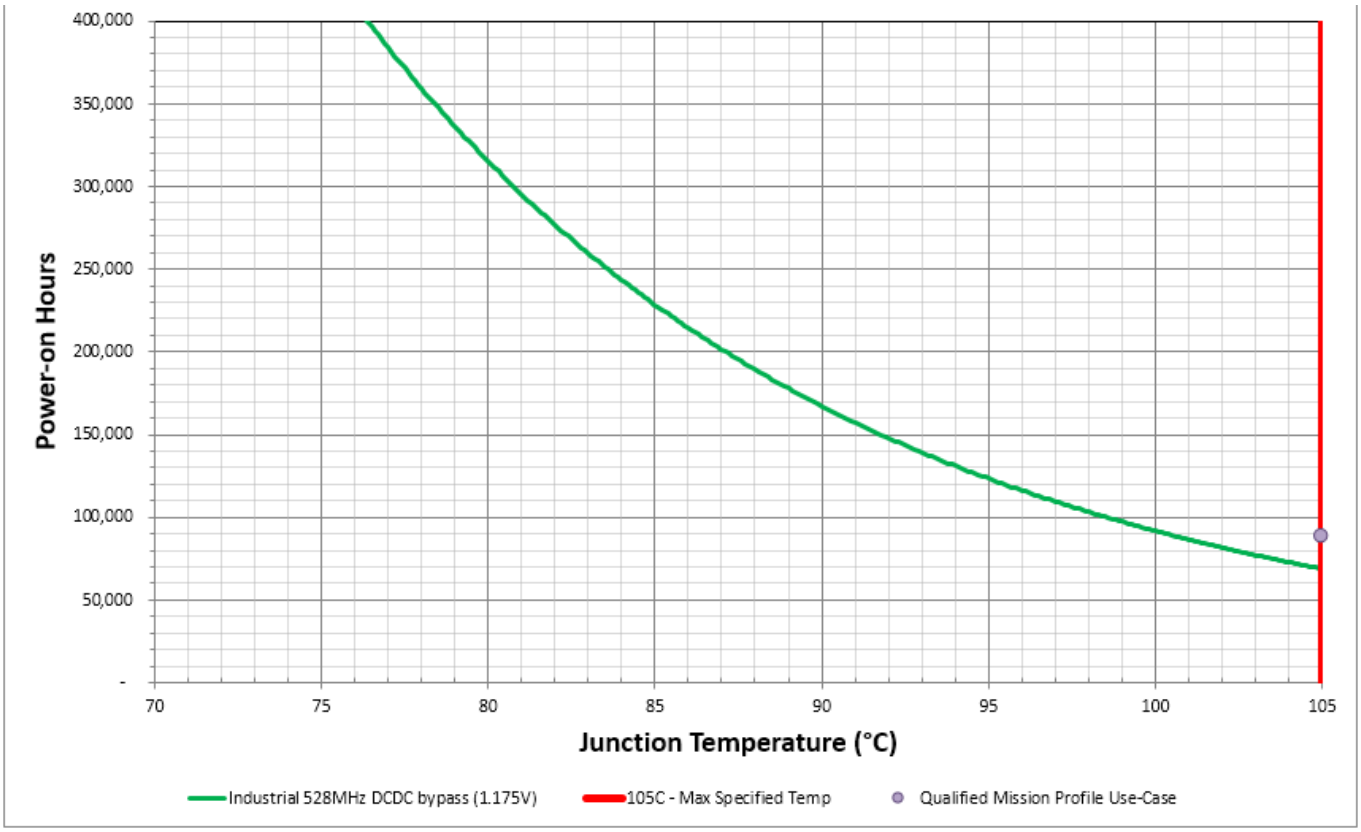

Figure 4. i.MXRT1060 Industrial lifetime estimates DCDC-bypass mode

3. Combining use cases

In some applications a constant operating use case cannot deliver the target PoH. In this case, it is advantageous to use multiple operating conditions. This method provides some of the lifetime benefits of running at a lower performance use case, while keeping the ability of the system to use the highest performance state dictated by the application's demands.

Scenario 1: Switching between two power states with different voltages.

In this scenario, the system is using the 600 MHz full power state, and the 528 MHz reduced power state. It is assumed for these calculations that the temperature stays constant in either mode. If the system spends 50% of its power-on-time at 600 MHz and 50% of its power-on-time at 528 MHz, the two POH (read from Figure 5) can be combined with using those percentages: 31,698 x 0.5 + 86,165 x

0.5 = 58,931 PoH.

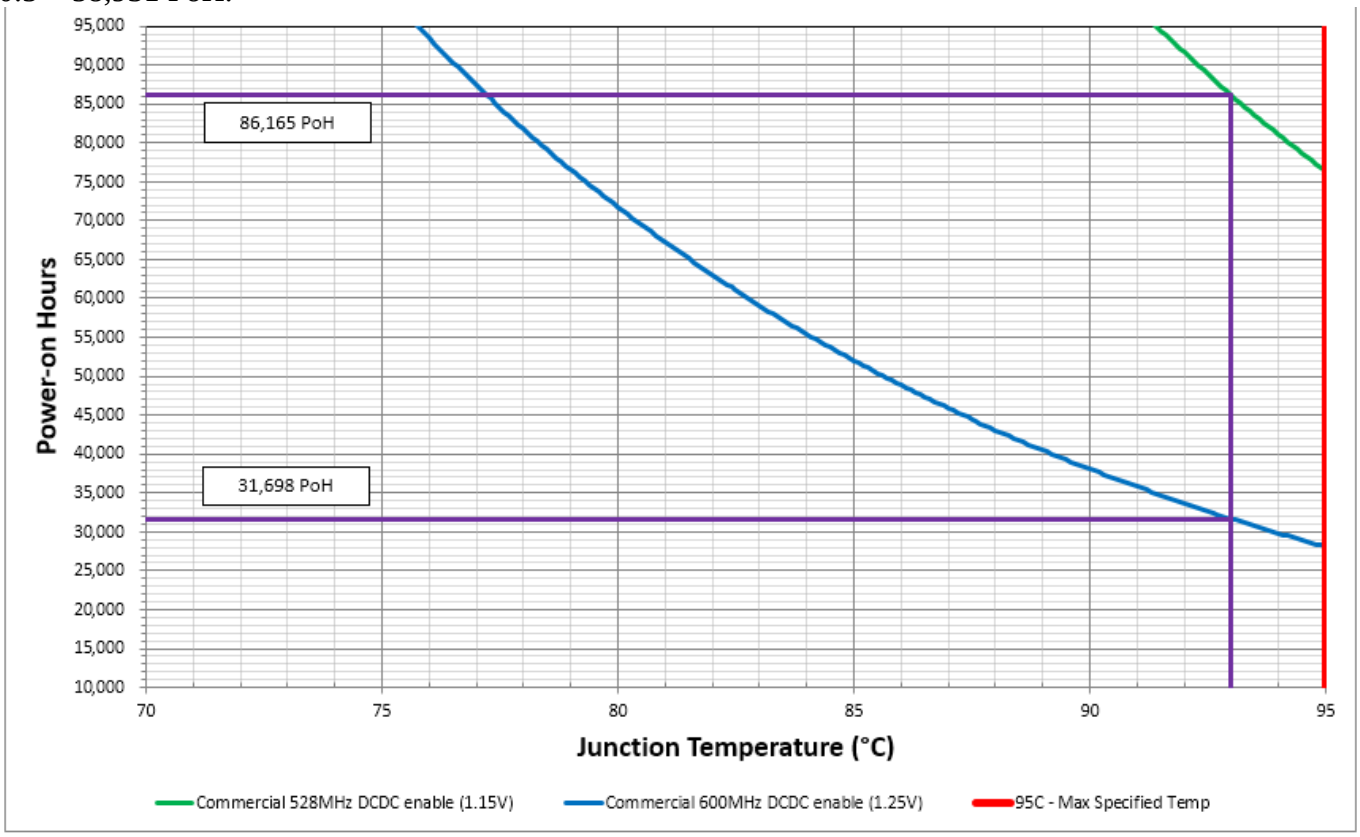

Figure 5. Multiple power state use case

Scenario 2: Switching between two power states with different temperatures

This scenario assumes that the system can achieve a drop in temperature by throttling back the performance while still maintaining a constant voltage. This temperature change may be able to be achieved by changing the frequency or by simply scaling back the loading on the Arm cores or processing units. This use case is particularly useful for customers who need to take advantage of the full commercial temperature range of the i.MXRT series.

In this scenario, the system spends 30% of its PoH at 93^{O}C and 70% of its power-on hours at 85^{O}C (as read off the chart in Figure 6). The two POH can be combined as follows: 31,698 x 0.3 + 52,038 x 0.7 = 45,932 PoH.

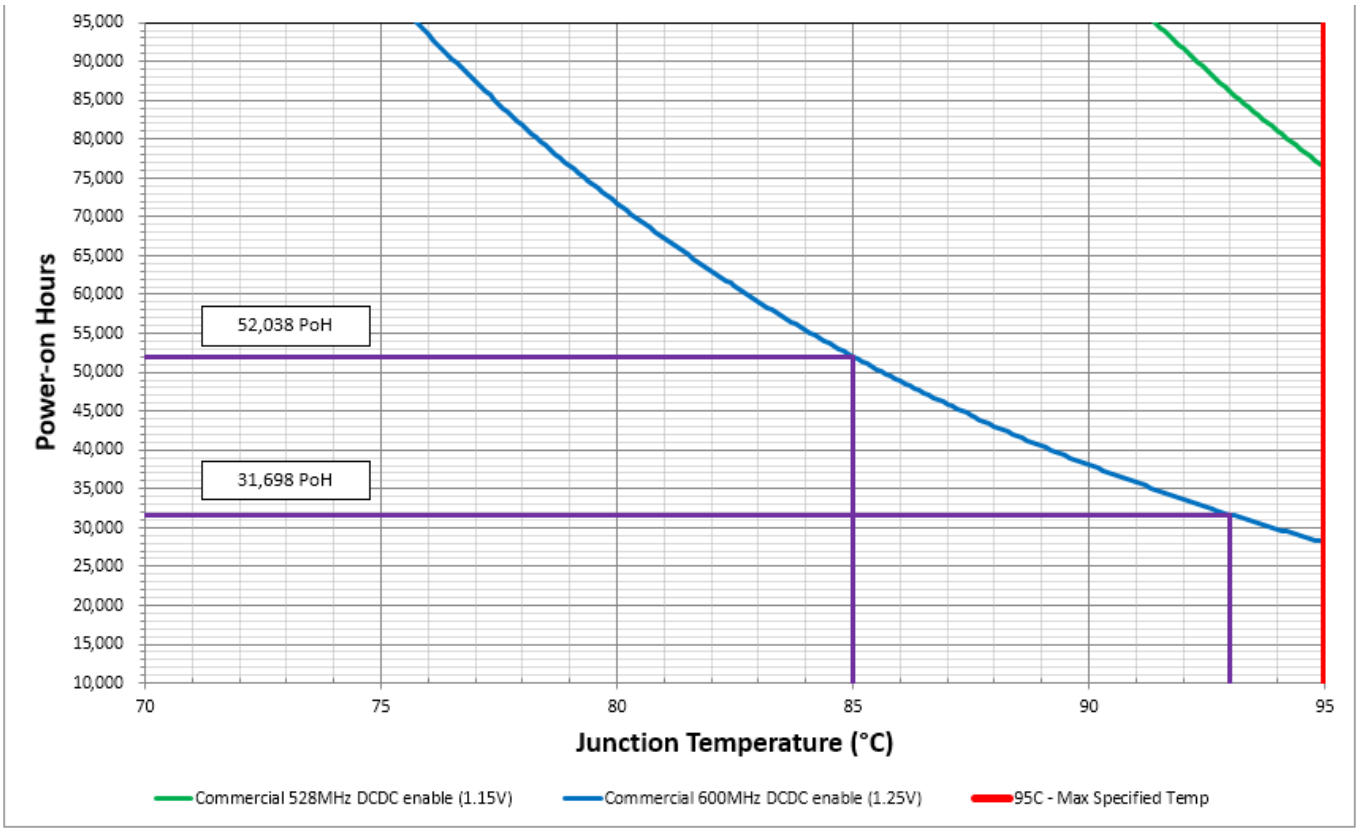

Figure 6. Multiple temperature use case

Scenario 3: Using three or more power states.

This scenario shows how this strategy how extend to more than two power states. While this example only has three power states, there is no limit to the actual number of the power states that can be combined. The power states that are being used in this scenario are 528 MHz (at 93^{O}C) and 600 MHz (at 85 ^{O}C and 93^{O}C). Each state is used equally one third of the time. These power states can be combined as follows: 86,165 x 0.34 + 52,038 x 0.33 + 31,298 x 0.33 = 56,796 PoH.

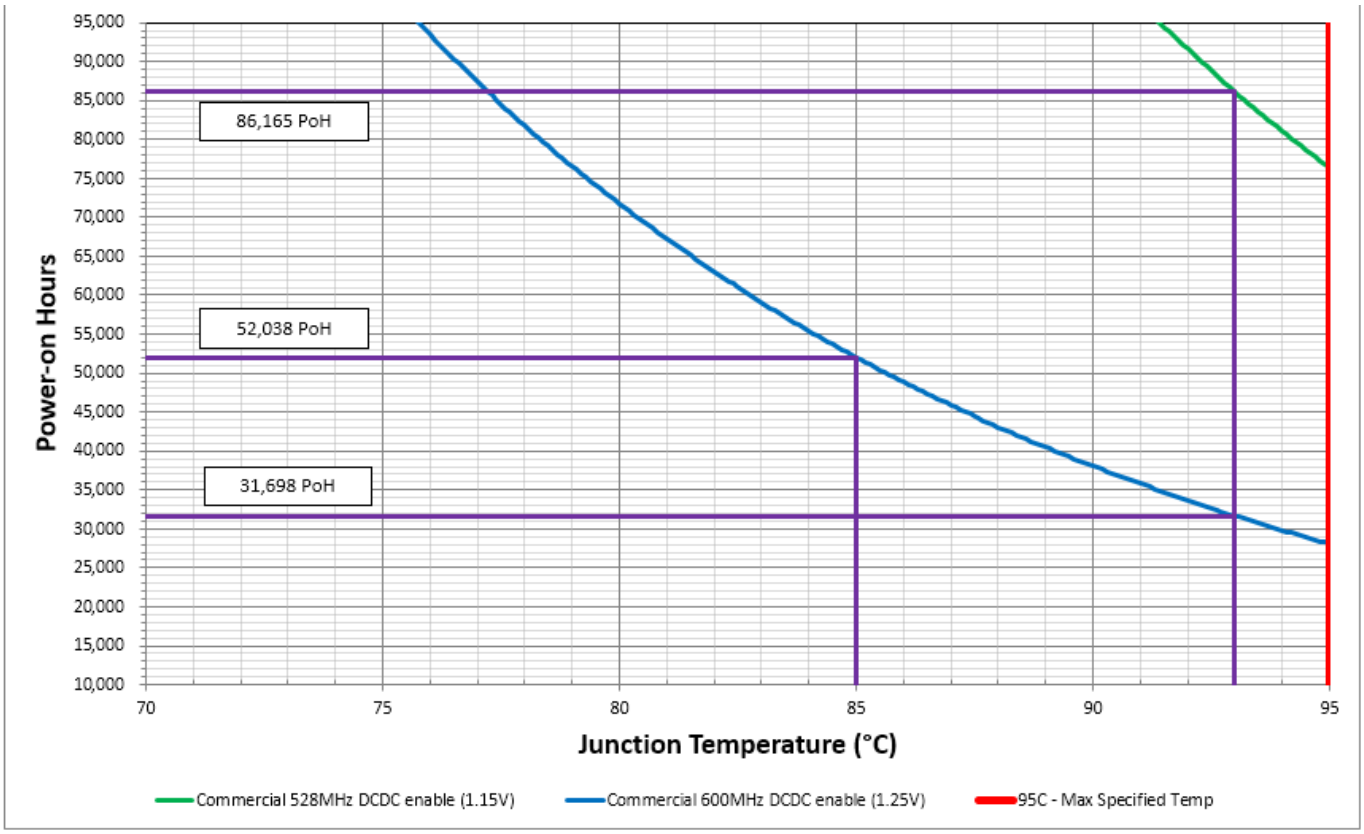

Figure 7. . Various use cases

4. Revision history

Revision	Change description
0	Initial release

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