AN13540

LPC553x/LPC55S3x High-Speed Comparator - Evaluation of Basic Features

Rev. 1 — 20 May 2022 Application Note

Contents

1 Introduction

This application note describes various design criteria that system designers should consider when implementing HSCMP designs with the LPC553x/LPC55S3x family of microprocessors. This application note describes the critical parts of an HSCMP sub-system and its interconnections with related MCU peripheral modules, particularly those related to fast system protection (overcurrent or overvoltage protection).

This application note deals with basic comparator features of the LPC553x/LPC55S3x device. It presents possibilities to set up and evaluate the HSCMP module for real-time control applications.

This document is useful for engineers who want to discover internal peripheral interconnection possibilities and use cases of the HSCMP module. The software package with the example is in the NXP MCUXpresso IDE. FreeMASTER real-time debugger is used for application monitoring and control. The examples in this application note are implemented on the LPCxpresso55S36 EVK.

1.1 Introduction to HSCMP

The High-Speed Comparator (HSCMP) module provides a circuit to compare two analog input voltages. It includes a comparator (CMP), comparator input selectors, 8-bit DAC, and an analog mux for each comparator input.

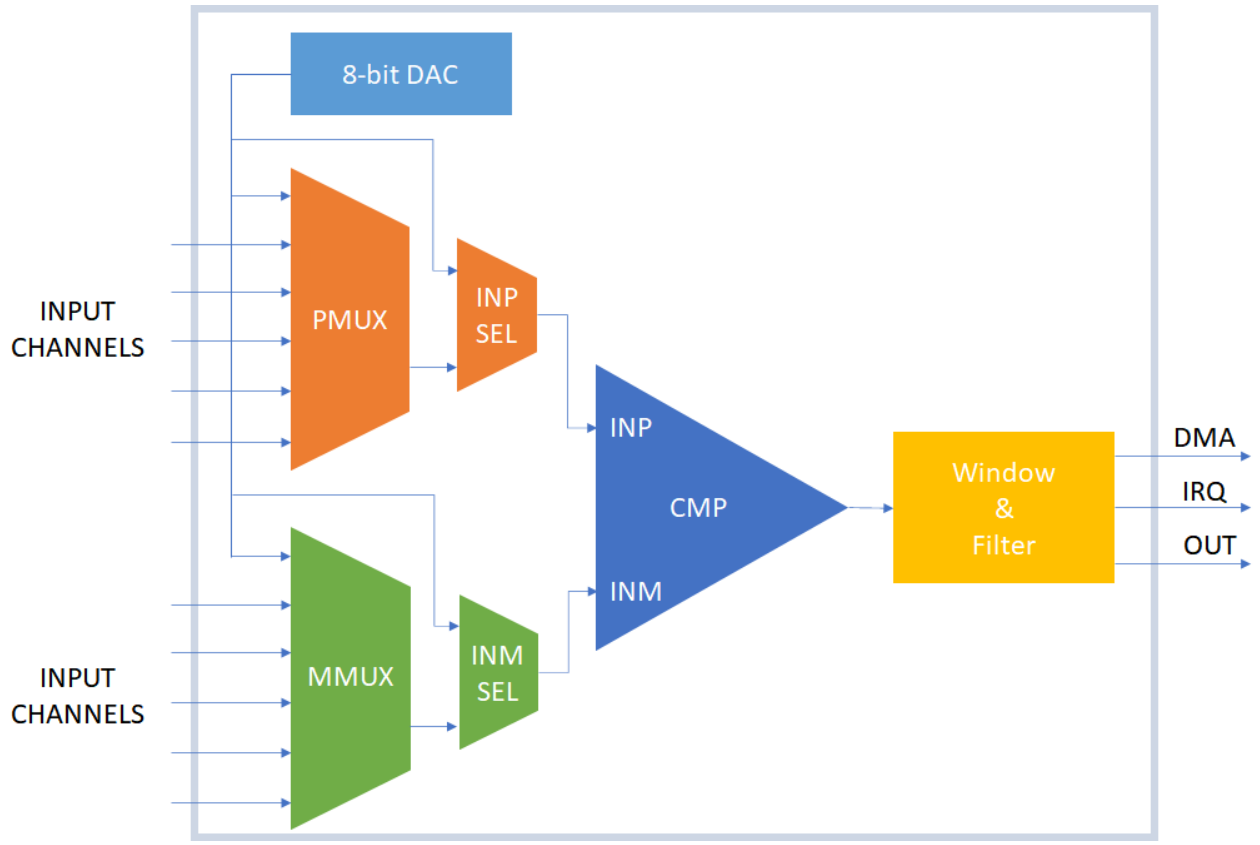

Figure 1. HSCMP block diagram

The CMP can operate across the full range of the supply voltage, which is known as a rail-to-rail operation. The DAC is a 256-tap resistor ladder network that provides a selectable voltage reference for applications that require a voltage reference. The 256-tap resistor ladder network divides the supply reference (Vin) into 256 voltage levels. An 8-bit digital signal input selects the output voltage level, which varies from Vin to Vin/256. Vin can be selected from two voltage sources, vrefh0 and vrefh1. The HSCMP's internal DAC output is available as an on-chip internal signal only. It is not available for an external device pin. An internal 8-bit DAC is connected to both input muxes and to the comparator input selector, which allows to select between the input mux or DAC directly. It is also possible to connect a 12-bit DAC, which is available on specific input channels (see the following sections).

1.2 HSCMP features

The features of the HSCMP module include the following:

- Two MUXes to select input signal from 8 channels
- Multiple operation modes to produce a wide range of outputs, such as:
  - Sampled
  - Windowed, which is ideal for certain PWM zero-crossing-detection applications
  - Digitally filtered
- Advanced feature for window and sample:
  - WINDOW/SAMPLE signal can be inverted
  - Window can be closed by COUT rising, falling, or both edges
  - User can define COUT level when window is closed
- Selectable performance levels: nano-power mode, low-power (speed) mode, high-power (speed) mode

- Programmable hysteresis control
- Selectable inversion on comparator output
- External hysteresis can be used at the same time as the output filter is used for internal functions
- Interrupt and DMA support
- Trigger mode
- Includes 8-bit resolution DAC
- Selectable supply reference source for DAC
- Configurable low- or high-power mode for DAC

HSCMP is intended for real-time control applications and fast-response use cases, such as overcurrent detection. It is possible to propagate a hardware compare event to disable the PWM, so the HSCMP acts as a hardware overcurrent protection. It could also be used for level-crossing detection of signals in various applications, such as power converters. The HSCMP compare event can also restart the PWM.

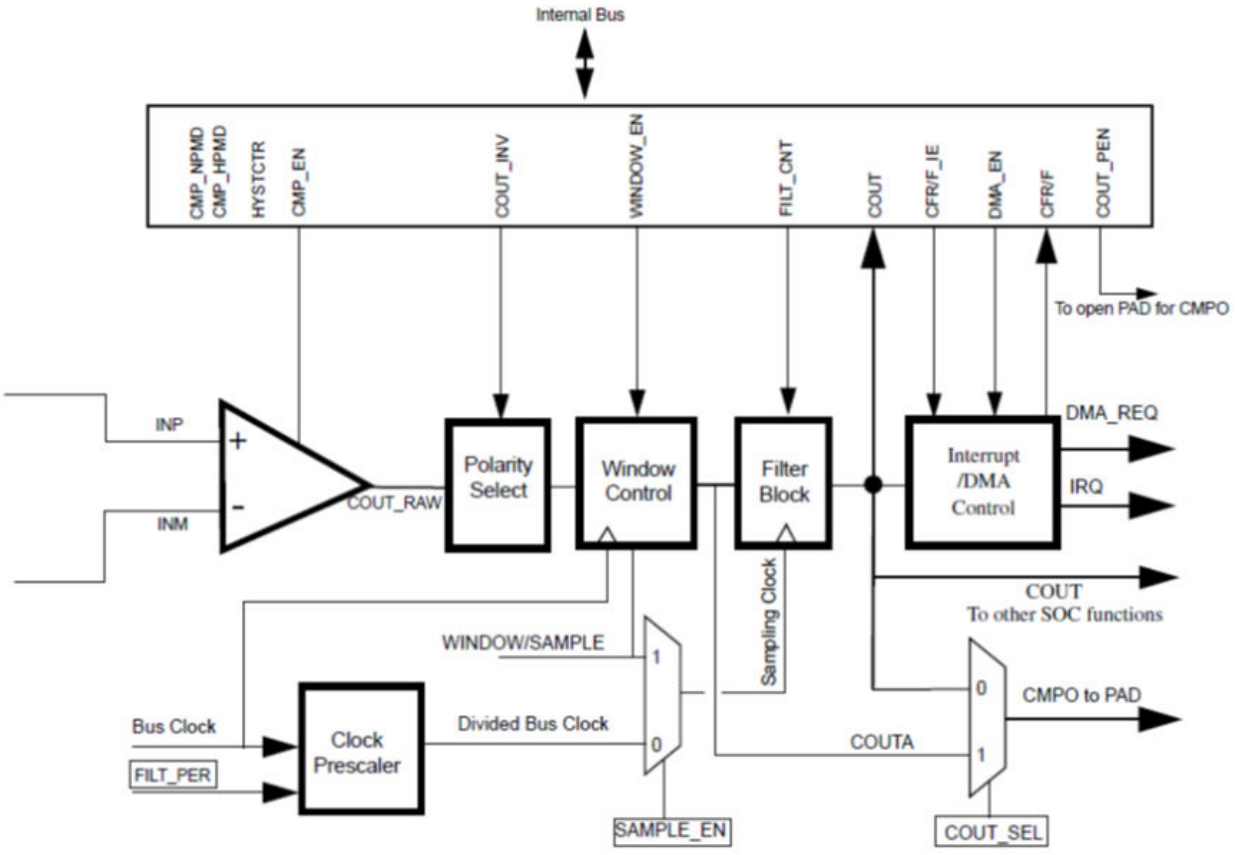

Figure 2. HSCMP block diagram

2 Pin configuration

The analog mode of the HSCMP multiplexer input pins must be set. For more details, see the "I/O Pin Configuration (IOCON)" chapter in the reference manual (pin multiplexing and IOCON register description) and the low-level software examples below. Table 1 summarizes all HSCMP pins on the LPC553x/LPC55S3x device and their availability on the HSCMP input mux. Inputs and indexes are identical on both positive and negative muxes and registers HSCMP_CCR2_MSEL and HSCMP_CCR2_PSEL.

Table 1. HSCMP inputs

Input MUX index	HSCMP0	HSCMP1	HSCMP2
0	HSCMP0_IN0 PIO0_24	HSCMP1_IN0 PIO0_7	HSCMP2_IN0 PIO0_17
1	HSCMP0_IN1 PIO1_12	HSCMP1_IN1 DAC0_OUT PIO1_22	HSCMP2_IN1 PIO1_23
2	Unconnected	Unconnected	Unconnected
3	HSCMP0_IN3 PIO1_5	HSCMP1_IN3 PIO1_10	Unconnected
4	HSCMP0_IN4 OPAMP0_OUT PIO1_9	OPAMP1_OUT	OPAMP2_OUT
5	DAC0_OUT PIO1_22	HSCMP1_IN5 DAC1_OUT PIO1_19	DAC2_OUT
6	Reserved	Reserved	Reserved
7	HSCMP0 DAC	HSCMP1 DAC	HSCMP2 DAC

2.1 Comparator evaluation

This application note and evaluation software describes basic functionality. The example demonstrates a comparison of two signals: the sawtooth generated by the 12-bit DAC and the constant voltage reference generated by the HSCMP internal 8-bit DAC. The result of the HSCMP comparison can be observed on the output pin. You can invert the output logic and set different threshold values (internal 8-bit DAC, external 12-bit DAC, or MCU input pins signals according to Table 1). MCUXpresso, LPC553x/LPC55S3x SDK package, and the FreeMASTER tool must be installed.

To run the SDK HSCMP example, perform the following steps:

1. Unzip the example to your hard drive location.
2. Import the example into the MCUXpresso IDE.
3. Build the example.
4. Flash the example.
5. Start the FreeMASTER HSCMP project.
6. Click the "Run" button.
7. Set the variables (especially the threshold value) in the runtime using the FreeMASTER real-time debugger. The result can be monitored using an oscilloscope.

The oscilloscope can be connected to J10-11 on LPCXpresso55S36 to monitor the 12-bit DAC output and a second probe can be connected to J10-9 to observe the comparator output (see Figure 3). External signal connected to J9-9 (HSCMP0_IN3) could be connected instead of the 12-bit DAC output. When evaluating the software example, the expected default waveforms should look like the signals in Figure 3.

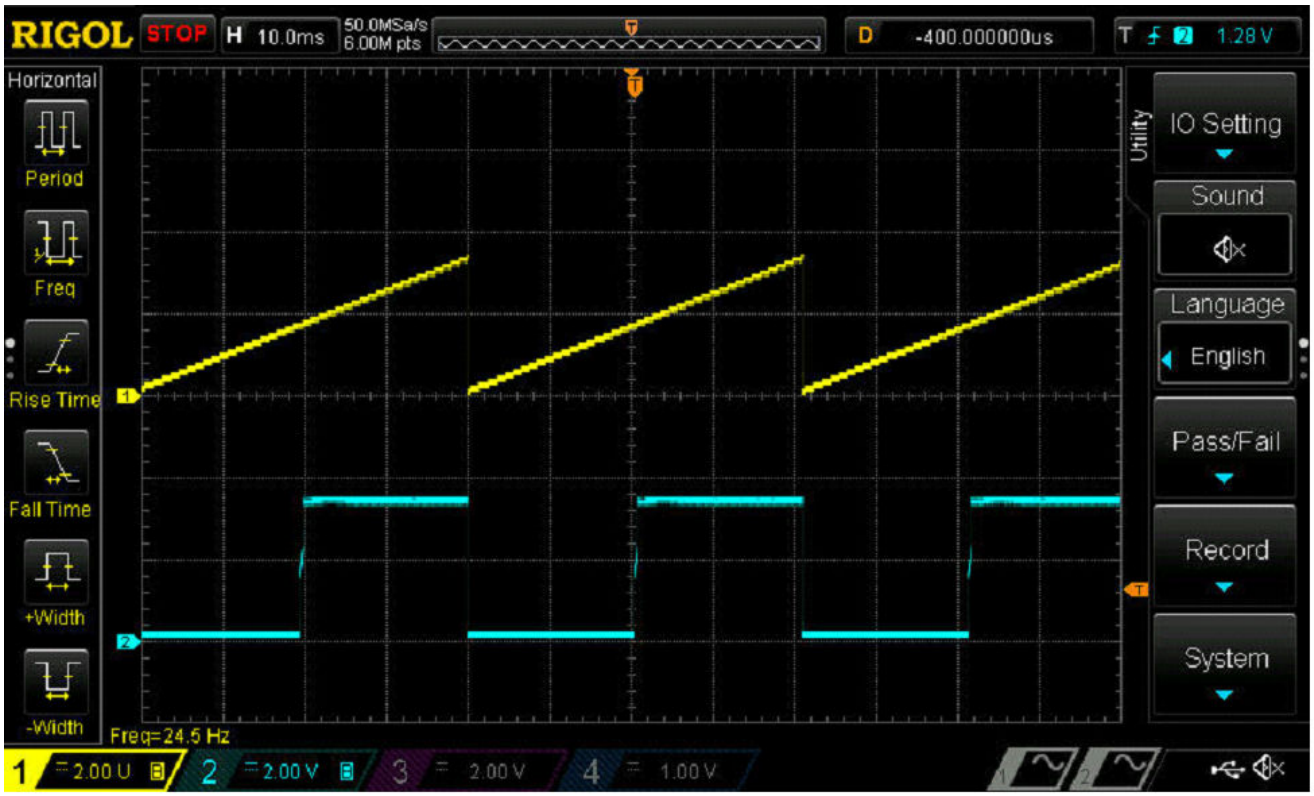

Figure 3. Expected waveforms

3 Using the HSCMPs for overcurrent protection

The following schematics show a typical 3-shunt configuration for motor-control applications. $R_{sh\_<x>}$ is a shunt resistor in a low-side current-sensing configuration. The voltage drop across this resistor is amplified by the internal variable-gain OPAMP. R_1 and R_2 are part of the internal resistor network and their values are, along with the positive reference voltage (PREF) source, configurable via the OPAMP_CTR register.

The OPAMP output signal (OPAMP<x>_OUT) is internally wired to ADCs, HSCMPs, and output pins. Depending on the particular OPAMP<x>_OUT – HSCMP<y> input combination, an analog switch may require to be closed by setting the respective ASW0 or ASW1 bits in the IOCON module PIO registers. See the corresponding table in the reference manual.

The HSCMP positive and negative input signals are configurable via the HSCMP CCR2 register.

The HSCMP output signal is routed via the INPUTMUX module to the fault input of the related eFlexPWM submodule (see the PWM0_FAULT0 – PWM0_FAULT3 registers of the INPUTPUX).

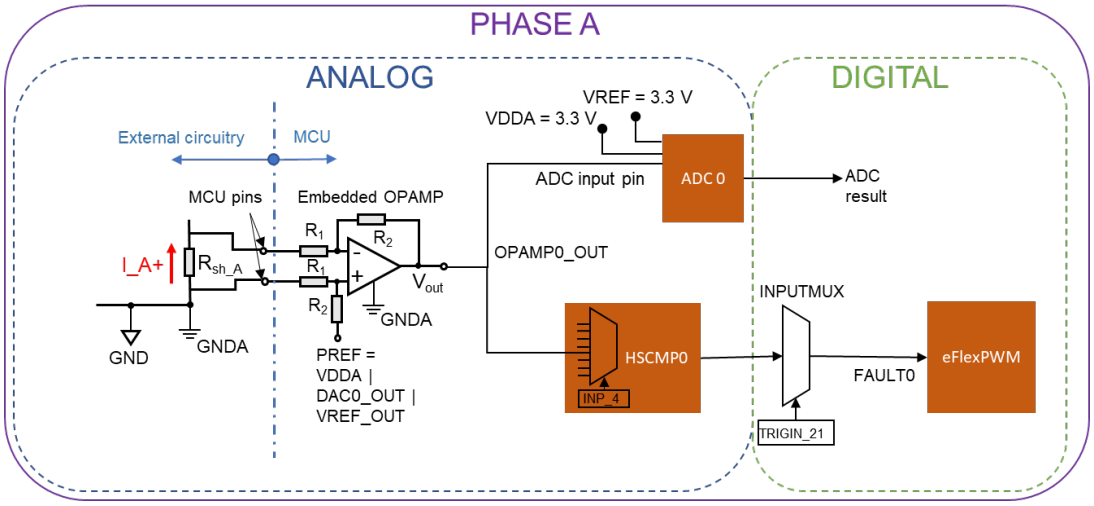

Figure 4. Overcurrent protection block diagram (phase A)

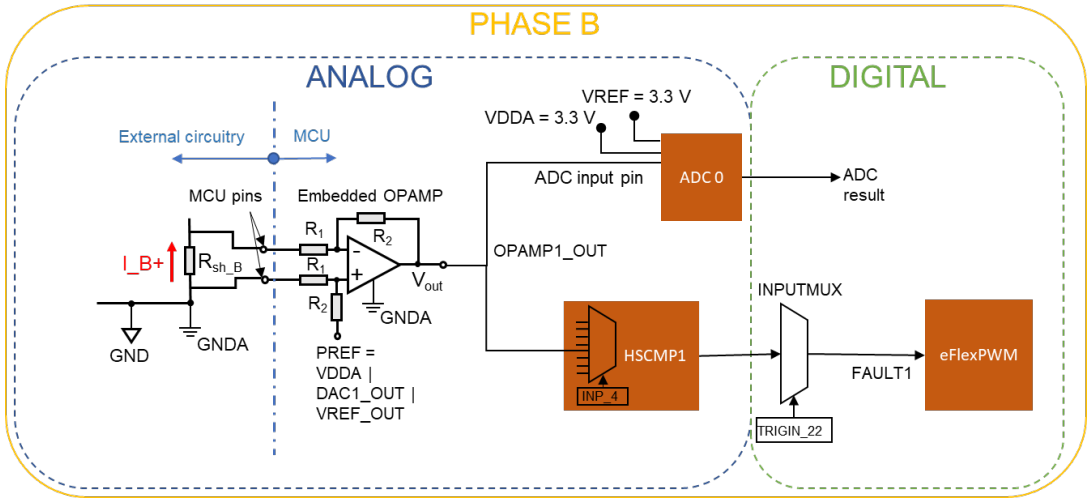

Figure 5. Overcurrent protection block diagram (phase B)

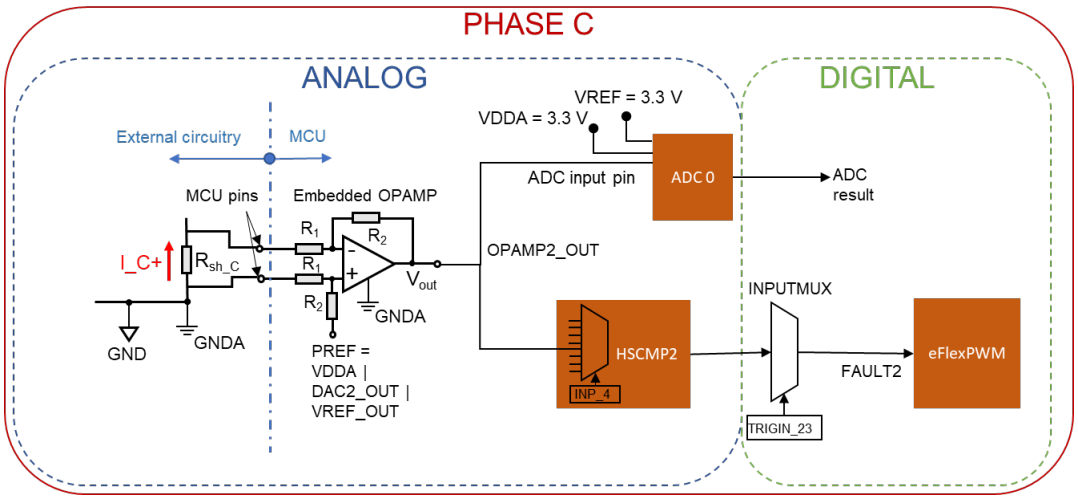

Figure 6. Overcurrent protection block diagram (phase C)

3.1 Overcurrent protection design guideline

The OPAMPn_OUT$_{max}$ voltage corresponding to the maximal current could be determined using the following formula:

$$OPAMPnOUT_{max} = (I_{max} * R_{sh} * GAIN) + PREF \qquad [V]$$

Please note that in the depicted scenario, the current direction convention is such that the overcurrent flowing from the DC-Bus to the GND generates a negative voltage drop across the shunt resistor, therefore OPAMPnOUT$_{max}$ < PREF.

This calculated value presents the comparator reference voltage, which may be generated by the internal 8-bit DAC of the HSCMP. Alternatively, an external 12-bit DAC could be set as the reference source. The comparator reference voltage should then be routed to the INM input of the comparator. The OPAMPn_OUT signal should be connected to the INP input pin. The HSCMP configuration example (using the internal DAC) is as follows:

```
/* Port 2, pin 14 (OPAMP1_OUT) to HSCMP1_IN4 - close the analog switch */
IOCON_PinMuxSet(IOCON, 2, 14, IOCON_FUNC0 | IOCON_ANALOG_EN | (1U << 10 ));
/* Power up the CMP bias circuitry */
POWER_DisablePD(kPDRUNCFG_PD_CMPBIAS);
/* Power up the HSCMP and its internal DAC */
 POWER_DisablePD(kPDRUNCFG_PD_HSCMP1);
 POWER_DisablePD(kPDRUNCFG_PD_HSCMP1_DAC);
HSCMP1->CCR1 = (1U << 5) | /* Enable comparator output*/
(1U << 4);
/* Use COUTA (unfiltered comparator output) */
HSCMP1->CCR2 = (0U << 28) | /* INM - 8-bit DAC */
(1U << 24) | /* INP - Analog 8-1 mux */
(7U << 20) | /* MSEL - 8-bit DAC */
(4U << 16) | /* PSEL - OPAMP1_OUT */
(1U << 0);
/* High power mode */
/* Set DAC_OUT to 1.225V (2.5A current through 0.020 Ohm shunt) */
HSCMP1->DCR = (94U << 16) | /* (3.3V / 256) * (94 + 1) = 1.224 V */
(1U << 15) | /* DAC output enable */
(1U << 1) | /* High power mode enabled */
(1U << 0);
/* DAC enable */
/* HSCMP enable */
HSCMP1->CCR0 = 1U;
```

The output of the HSCMP should be routed (via the INPUTMUX module) to the respective FAULT input of the PWM submodule responsible for generating the corresponding phase PWM signals. The INPUTMUX configuration example is as follows:

```
/* Separate fault per each OPAMP */
INPUTMUX->PWM0_FAULT[0] = 21U;
/* PWM0 fault 0 = HSCMP0 */
INPUTMUX->PWM0_FAULT[1] = 22U;
/* PWM0 fault 1 = HSCMP1 */
INPUTMUX->PWM0_FAULT[2] = 23U;
/* PWM0 fault 2 = HSCMP2 */
```

The FAULT signal is edge-sensitive and its polarity is configurable. The PWM must be configured to detect the fault signal and react appropriately. The FlexPWM fault-handling configuration example is as follows:

```
/* Separate fault per each OPAMP */
PWM0->SM[0].DISMAP[0] = 0xF777U;
PWM0->SM[1].DISMAP[0] = 0xF777U;
PWM0->SM[2].DISMAP[0] = 0xF777U;
PWM0->SM[3].DISMAP[0] = 0xF777U;
/* PWM fault filter - 3 Fast periph. clocks sample rate, 5 agreeing samples to activate */
PWM0->FFILT |= PWM_FFILT_FILT_PER(2);
PWM0->FFILT |= PWM_FFILT_FILT_CNT(2);
/* All interrupts disabled, safe manual fault clearing */
PWM0->FCTRL &= ~(PWM_FCTRL_FLVL_MASK | PWM_FCTRL_FAUTO_MASK | PWM_FCTRL_FSAFE_MASK |
PWM_FCTRL_FIE_MASK);
/* Clear FCTRL register prior further settings */
PWM0->FCTRL |= PWM_FCTRL_FIE(0U);
/* FAULT 0 & FAULT 1 - Interrupt disable */
/* Internal OPAMP fault signals are active low. */
PWM0->FCTRL |= PWM_FCTRL_FLVL(0x0U);
PWM0->FCTRL |= PWM_FCTRL_FAUTO(0U);
PWM0->FCTRL |= PWM_FCTRL_FSAFE(0xFU);
```

4 Revision history

Table 2. Revision history

Revision number	Date	Substantive changes
0	27 January 2022	Initial release
1	20 May 2022	Replaced LPC55S36 with LPC553x/ LPC55S3x

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