The TEA9026T is a controller IC for resonant power supplies with a wide input voltage range. To compensate the frequency variation and the input voltage change, it incorporates a new mains input compensation curve. To reach a high efficiency at all power levels, it introduces a new operating mode: low-power mode. This mode operates in the power region between continuous switching (now called high-power mode) and burst mode. Most LLC resonant converter controllers regulate the output power by adjusting the operating frequency. The TEA9026T regulates the output power by adjusting the voltage across the primary resonant capacitor for accurate state control and a linear power control. External presets can adjust the mains compensation curve and the operating modes. This feature provides flexibility and ease of design for optimizing controller properties to wide input range LLC resonant designs.
## Revision history

<table>
<thead>
<tr>
<th>Rev</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>v.1</td>
<td>20220614</td>
<td>Initial version</td>
</tr>
</tbody>
</table>
1 Introduction

The TEA9026T is a fully digital controller for high-efficiency resonant power supplies with a wide input voltage range. Together with the TEA2095T dual SR controller, a complete resonant power supply can be built, which is easy to design and has a very low component count. This power supply meets the efficiency regulations of Energy Star, the Department of Energy (DoE), the Eco-design directive of the European Union, the European Code of Conduct and other guidelines. So, an additional power supply for standby supply is not required.

The TEA9026T is a derivative product of the TEA19161. The functions and external presets of the TEA9026T are optimized for wide input voltage range. This application note describes the related functions and external presets. The "TEA19161 and TEA19162 controller ICs" application note describes the common functions and information for the TEA19161 (Ref. 1).

This document is set up in such a way, that a chapter or paragraph of a specific topic can be read as a standalone description. A minimum number of cross-references to other document parts of the TEA9026T data sheet is used. This document setup leads to repetition of some information within the application note and to descriptions or figures that are similar to the ones published in the data sheet. To enhance readability, only typical values are given in most cases.

1.1 Related products

NXP Semiconductors products that are related to the TEA9026T are:

- **TEA19161:**
  This product is the core product of TEA9026T. For designing applications, the recommendation is to use the TEA19161 with the TEA19162. The TEA19162 is a DCM/QR PFC controller IC.

- **TEA2095T:**
  The newest synchronous rectification controller for resonant converters with dual gate drivers in an SO8 package. This product is optimized for the TEA9026T operating modes.

- **TEA1708:**
  An X-capacitor discharge IC.
2 TEA9026T highlights and features

2.1 Resonant conversion for wide input voltage range

The market of today demands high-quality, reliable, small, light-weight, and efficient power supplies.

A resonant DC-to-DC converter produces sinusoidal currents with low switching losses. It provides the possibility of operating at higher frequencies with excellent efficiency at high power levels.

In recent years, LLC resonant converters have become more popular because of the high efficiency at medium and high output load. The latest generation of resonant controllers that support burst-mode operation have enabled good efficiency from low load to high load. It also enables a good low power consumption in standby, minimizing the losses at no-load operation.

Resonant converters are difficult to design in combination with wide input voltage range. So, they are typically designed with a PFC prestage. Due to the characteristic of a resonant converter, a high input voltage range also implies a wide frequency range. As the output power depends on the input voltage and the frequency, it causes a high variation on the mode transition levels and the overpower protection level.

The TEA9026T incorporates the mains compensation function which compensates not only mains input voltage, but also the frequency variation. This new compensation can achieve more constant operation-mode transition levels and overpower protection levels over mains input voltages.

2.2 TEA9026T key features

- Wide input voltage range
- Integrated high-voltage start-up
- Integrated high-voltage level shifter (LS)
- Fast start-up (< 500 ms)
- Continuous $V_{SUPIC}$ regulation via the SUPHV pin during start-up and protection, allowing minimum SUPIC capacitor values
- Operating frequencies are outside the audible area in all operating modes
- Integrated soft start

2.3 TEA9026T green features

- High efficiency from low load to medium load
- Excellent no-load input power
- Regulated low optocurrent, enabling low no-load power consumption
- Very low supply current during non-switching state in burst mode
- Transitions between modes and power levels adjustable with external presets
- Externally adjustable low-power mode to burst mode transition level
- Adaptive non-overlap time
2.4 TEA9026T protection features

- Safe-restart mode for whole system fault conditions
- Accurate output overvoltage protection (OVP)
- Open-loop protection (OLP)
- Internal overtemperature protection (OTP)
- Supply undervoltage protection (UVP)
- Overpower protection (OPP)
- Capacitive mode protection (CMR)
- Maximum low-side and high-side LLC on-time protection
- Overcurrent protection (OCP)
- Disable input

2.5 TEA9026T typical applications

- TV application
- Printers
- E-bike chargers
3 Application diagram

The application diagram shows LLC resonant converter design with wide input voltage range.

Figure 1. TEA9026T application diagram
4 Wide input voltage range LLC design and TEA9026T functions

4.1 Wide range input LLC design

The input power of an LLC resonant converter can be calculated with Equation 1.

\[ P_{in} = \frac{P_{out}}{\eta} = V_{in} \times \Delta V \times C_r \times f_{sw} \]  

Equation 1 shows that the output power is related to the input voltage \( V_{in} \). As the input voltage changes, the frequency varies as well. To compensate this input voltage influence, a controller IC must compensate the input voltage and the frequency variation.

Typically, the application which requires LLC resonant design with wide input voltage is separated to the low mains input range (for example, 85 V (AC) to 135 V (AC)) or the high mains input range (for example, 150 V (AC) to 264 V (AC)). Although there is a large capacitor after the bridge rectifier, the minimum LLC input voltage is lower than the peak level of a minimum AC input voltage because of the voltage ripple on the capacitor. So, the LLC input voltage range depends on the system AC mains voltage range and the input capacitor design. In addition, the frequency variation is related to resonant tank design. To satisfy various system requirements, the TEA9026T offers extended input voltage compensation setting options.

4.2 Mains input voltage compensation of the TEA9026T

The TEA9026T incorporates mains input voltage compensation. The SNSBOOST pin, which is connected to the input capacitor with an external resistor divider, detects the input voltage \( V_{SNSBOOST} \). The \( f(SNSBOOST) \) is an internal compensation related to \( V_{SNSBOOST} \). The \( f(SNSBOOST) \) also compensates for the switching frequency, which depends on the input voltage.

Since the \( f(SNSBOOST) \) compensates the input voltage and the switching frequency, the internal Ctrl_P signal is only related to the output power. The OPP level and the mode transition levels are derived from the Ctrl_P.

Figure 2 shows the relation between Ctrl_P, \( f(SNSBOOST) \), and \( \Delta V_{SNSCAP} \).

To support various design requirements, the TEA9026T has several compensation options. Figure 3 shows \( f(SNSBOOST) \) versus \( V_{SNSBOOST} \) for different options.

\[ \Delta V_{Cr} = \frac{P_{out}}{\eta V_{in} C_r f_{sw}} \]  

\[ \Delta V_{SNSCAP} = Ctrl_P \times f(SNSBOOST) \]
Figure 2. Relation between Ctrl_P, f(SNSBOOST), and ΔV_{SNSCAP}

Figure 3. Mains compensation curves versus SNSBOOST pin voltage

(1) Compensation curve 1
(2) Compensation curve 2
(3) Compensation curve 3
(4) Compensation curve 4
Example with compensation curve 4:

- SNSBOOST voltage range: 1.4 V to 2.6 V
- f(SNSBOOST) at $V_{\text{SNSBOOST}} = 1.4$ V with compensation curve 4: 2.3
- f(SNSBOOST) at $V_{\text{SNSBOOST}} = 2.6$ V with compensation curve 4: 0.45
- Ratio of $V_{\text{SNSBOOST}}$ variation: 2.6 V / 1.4 V = 1.86
- Ratio of f(SNSBOOST) variation: 2.3 / 0.45 = 5.11
- Compensation amount for frequency change: 5.11 / 1.86 = 2.75

### 4.3 $V_{\text{SNSCAP}}$ levels for different power levels

When calculating the output power levels for OPP or HP-LP transition, the $\Delta V_{\text{SNSCAP}}$ value is required. Equation 4 shows the relationship between the $\Delta V_{\text{SNSCAP}}$ level, f(SNSBOOST), and the power level.

$$\Delta V_{\text{SNSCAP}} = 1.2 \, V \times \frac{P_{\text{out}}[\%]}{125 \%} \times f\left(\text{SNSBOOST}\right)$$  \hspace{1cm} (4)

The SNSCAP pin is internally biased to 2.5 V. $V_{\text{hs(SNSCAP)}}$ and $V_{\text{ls(SNSCAP)}}$ can be calculated with Equation 5 and Equation 6. Where, $V_{\text{hs(SNSCAP)}}$ is an internal threshold which turns off the high-side gate and $V_{\text{ls(SNSCAP)}}$ is an internal threshold which turns off the low-side gate.

$$V_{\text{hs(SNSCAP)}} = 2.5 \, V + 0.6 \, V \times \frac{P_{\text{out}}[\%]}{125 \%} \times f\left(\text{SNSBOOST}\right)$$  \hspace{1cm} (5)

$$V_{\text{ls(SNSCAP)}} = 2.5 \, V - 0.6 \, V \times \frac{P_{\text{out}}[\%]}{125 \%} \times f\left(\text{SNSBOOST}\right)$$  \hspace{1cm} (6)

$P_{\text{out}}$ is a percentage of the nominal output power. The $P_{\text{out}}$ levels of the overpower protection and the power limit are 125 % and 150 %. The maximum $\Delta V_{\text{SNSCAP}}$ level ($\Delta V_{\text{th(max)}\text{SNSCAP}}$) is 3 V. Although the result of Equation 4 is a higher value than the $\Delta V_{\text{th(max)SNSCAP}}$, the $\Delta V_{\text{SNSCAP}}$ value is clamped to 3 V.

Figure 4 shows the $\Delta V_{\text{SNSCAP}}$ curves of the overpower protection (OPP) versus $V_{\text{SNSBOOST}}$ for the different compensation options. It is derived from Equation 4 with f(SNSBOOST) information. Equation 4, Equation 5, and Equation 6 and the information of Figure 4 are valid without a voltage offset to the SNSCAP. When applying a voltage offset to the SNSCAP, the calculated levels change. Section 5.5 gives a more detailed explanation of adding an offset to the SNSCAP.
If ΔV_{SNSCAP} must be calculated at different V_{SNSBOOST} levels, f(SNSBOOST) information is required. Table 1 shows the f(SNSBOOST) levels for the different options.

Table 1. f(SNSBOOST) value at V_{SNSBOOST} for different compensation options

<table>
<thead>
<tr>
<th>V_{SNSBOOST} condition</th>
<th>f(SNSBOOST)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compensation 1</td>
<td></td>
</tr>
<tr>
<td>V_{SNSBOOST} &gt; 1.85 V</td>
<td>2.582 – 0.682 × V_{SNSBOOST} × [1 / V]</td>
</tr>
<tr>
<td>1.85 V &gt; V_{SNSBOOST} &gt; 1.67 V</td>
<td>5.226 – 2.111 × V_{SNSBOOST} × [1 / V]</td>
</tr>
<tr>
<td>1.85 V &gt; V_{SNSBOOST} &gt; 1.67 V</td>
<td>9.178 – 4.478 × V_{SNSBOOST} × [1 / V]</td>
</tr>
<tr>
<td>Compensation 2</td>
<td></td>
</tr>
<tr>
<td>V_{SNSBOOST} &gt; 1.95 V</td>
<td>2.389 – 0.656 × V_{SNSBOOST} × [1 / V]</td>
</tr>
<tr>
<td>1.95 V &gt; V_{SNSBOOST} &gt; 1.48 V</td>
<td>5.217 – 2.106 × V_{SNSBOOST} × [1 / V]</td>
</tr>
<tr>
<td>V_{SNSBOOST} &gt; 1.48 V</td>
<td>8.678 – 4.444 × V_{SNSBOOST} × [1 / V]</td>
</tr>
<tr>
<td>Compensation 3</td>
<td></td>
</tr>
<tr>
<td>V_{SNSBOOST} &gt; 1.96 V</td>
<td>2.464 – 0.725 × V_{SNSBOOST} × [1 / V]</td>
</tr>
<tr>
<td>1.96 V &gt; V_{SNSBOOST} &gt; 1.42 V</td>
<td>5.472 – 2.259 × V_{SNSBOOST} × [1 / V]</td>
</tr>
<tr>
<td>V_{SNSBOOST} &gt; 1.42 V</td>
<td>7.870 – 3.948 × V_{SNSBOOST} × [1 / V]</td>
</tr>
<tr>
<td>Compensation 4</td>
<td></td>
</tr>
<tr>
<td>V_{SNSBOOST} &gt; 2.06 V</td>
<td>2.236 – 0.688 × V_{SNSBOOST} × [1 / V]</td>
</tr>
<tr>
<td>2.06 V &gt; V_{SNSBOOST} &gt; 1.19 V</td>
<td>5.366 – 2.207 × V_{SNSBOOST} × [1 / V]</td>
</tr>
<tr>
<td>V_{SNSBOOST} &gt; 1.19 V</td>
<td>7.500 – 4.000 × V_{SNSBOOST} × [1 / V]</td>
</tr>
</tbody>
</table>

Figure 4. ΔV_{SNSCAP} curves versus SNSBOOST pin voltage for OPP (125 %)
4.3.1 Time delay $V_{SNSCAP}$-to-HB transition

The level of transition depends on an internal SNSCAP target level and a time delay until the HB transition. The time delay includes:

- Time between the moment SNSCAP reaches the target level (A) and the moment the GATE switches off (B). This time is internally fixed: 150 ns.
- Time between the moment the GATE switches off (B) and the moment HB reaches half of its maximum value (C). This time depends on the application properties. In this document, 300 ns is assumed.

The time delay leads to a difference in power level between the control of mode transition level and reality. This difference can lead to a substantial difference in (mode transition) power levels. When the application-depending delay (B-C) is different from the 300 ns used in this document, the estimated power levels are different as well.

![Diagram of Time delay $V_{SNSCAP}$-to-HB transition](image)

To measure $\Delta V_{SNSCAP}$ without the application-depending delay (B-C), $V_{SNSCAP}$ must be measured at the starting of falling edges of the GateLS pin voltage and the GateHS pin voltage. However, the measured $\Delta V_{SNSCAP}$ can be higher than the internal threshold levels of the IC, because of the IC propagation delay (A-B).
4.4 SNSBOOST voltage levels and SNSBOOST pin design guideline

The SNSBOOST pin has two threshold levels, the start level ($V_{\text{start(SNSBOOST)}}$) and the undervoltage protection level ($V_{\text{uvp(SNSBOOST)}}$). When the $V_{\text{SNSBOOST}}$ exceeds $V_{\text{start(SNSBOOST)}}$ (1.4 V) with satisfying other start-up conditions ($V_{\text{SUPIC}} > V_{\text{start(SUPIC)}}$ and $V_{\text{SUPREG}} > V_{\text{uvp(SUPREG)}}$ and success of readout settings), the TEA9026T starts switching. When $V_{\text{SNSBOOST}}$ drops to below $V_{\text{uvp(SNSBOOST)}}$ the TEA9026T stops switching. The external resistor divider on the SNSBOOST pin can be designed based on the brownin requirements.

Example of SNSBOOST resistor calculation:

- AC mains voltage range: 150 V (AC) to 264 V (AC)
  - Maximum LLC input voltage at 150 V (AC): $150\sqrt{2} = 212$ V
  - Minimum LLC input voltage at 150 V (AC) with a 94 μF input capacitor: 141 V
- Target brownin level: 140 V (AC)
- The selected upper side resistor on SNSBOOST pin: 6 MΩ
- The calculated lower side resistor on SNSBOOST pin: $\frac{6 \text{ MΩ}}{140 \sqrt{2} - 1} = 43 \text{ kΩ}$

- Check that the minimum $V_{\text{SNSBOOST}}$ at 150 V (AC) exceeds $V_{\text{uvp(SNSBOOST)}}$ (0.8 V):
  $$141 \text{ V} \times \frac{43 \text{ kΩ}}{6 \text{ MΩ} + 43 \text{ kΩ}} = 1 \text{ V}$$

For real-time compensation over the input voltage, use a capacitor on the SNSBOOST pin of < 1 nF.
5 Presetting TEA9026T functionality for wide range input voltage

Before the system starts operation, it reads the external settings. Several internal settings can be defined with specific values for resistors at GATELS, SNSSET, and SNSOUT. These settings cannot be changed during operation. They are refreshed at each start or restart. The resistors are:

- GATELS resistor ($R_{\text{GATELS}}$)
- SNSSET resistor ($R_1$)
- SNSSET resistor ($R_2$)
- SNSOUT resistor ($R_{\text{SNSOUT}}$)

![Diagram of TEA9026T](image)

Figure 6. Presetting TEA9026T using values of four resistors

5.1 Setting the soft start power level (RGATELS)

To limit the power in each cycle at start-up, the $V_{\text{SNSCP}}$ control switching levels are given an offset. During start-up, the slope compensation makes a sweep of 12 ms. The maximum start-up time is 12 ms. However, under normal conditions, the start-up time is much shorter. The compensation that is used at start-up can be optimized with the value of resistor $R_{\text{GATELS}}$. The range of values for resistor $R_{\text{GATELS}}$ is: $100 \text{ k}\Omega \leq R_{\text{GATELS}} \leq 300 \text{ k}\Omega$. 
Any value within this range can be applied. The value is sampled in 255 steps accuracy which approaches an analog setting. At 100 kΩ, the energy in the first cycle is lowest. At 300 kΩ, it is highest.

This optimization function depends on the application converter properties and behavior. So, when the behavior of the primary current and the output voltage increase is monitored, experimenting must determine the value. A typical value is 180 kΩ.

During the start-up slope, functions that are also active during normal operation can influence the behavior:

- SNSBOOST pin: Compensation for lower input voltage
- Symmetry regulation to keep the duty cycle close to 50%
- SNSFB: Start regulation when the nominal output voltage is reached

5.2 SNSSET resistor R1

The value of resistor R1 on the SNSSET pin presets the mains compensation curve and the burst frequency. Table 2 shows the $R_{\text{SNSSET1}}$ values and options.

<table>
<thead>
<tr>
<th>$R_{\text{SNSSET1}}$</th>
<th>Mains compensation curve</th>
<th>Burst frequency (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 10</td>
<td>No start-up</td>
<td></td>
</tr>
<tr>
<td>53.6</td>
<td>1</td>
<td>800</td>
</tr>
<tr>
<td>61.9</td>
<td>2</td>
<td>800</td>
</tr>
<tr>
<td>71.5</td>
<td>3</td>
<td>800</td>
</tr>
<tr>
<td>82.5</td>
<td>4</td>
<td>800</td>
</tr>
<tr>
<td>95.3</td>
<td>1</td>
<td>1600</td>
</tr>
<tr>
<td>110</td>
<td>2</td>
<td>1600</td>
</tr>
<tr>
<td>127</td>
<td>3</td>
<td>1600</td>
</tr>
<tr>
<td>147</td>
<td>4</td>
<td>1600</td>
</tr>
</tbody>
</table>

The TEA9026T incorporates the four mains compensation curves. Figure 3 shows the compensation versus the SNSBOOST voltage for different curve options. The compensation curve can be selected based on the overpower protection performance. Related to the selected compensation curve, the HP-LP transition power and the LP-BM transition power are compensated as well. The sections below introduce options for the HP-LP transition level and the LP-BM transition level.

5.3 SNSSET resistor R2 and SNSOUT resistor

The SNSSET resistor R2 and the SNSOUT resistor preset the following option:

- $R_{\text{SNSSET2}}$:
  - HP-LP transition level. The possible options are 20 % and 30 %
  - $R_{\text{SNSSET2}}$:
    - LP-BM transition level at $V_{\text{SNSBOOST}} = 2.5$ V
- $R_{\text{SNSOUT1}}$:
  - LP-BM transition level at $V_{\text{SNSBOOST}} = 1.3$ V

The HP-LP transition level has two options, 20 % and 30 %. This transition level is constant as the input voltage.

At lower load conditions, the internal Ctrl_P signal becomes less accurate because the frequency as function of the input voltage is different with higher load condition. In...
addition, the delays are more significant at lower loads. So, as the input voltage changes, the LP-BM transition level changes as well.

The TEA9026T can adjust the LP-BM transition levels as function of the input voltage. The SNSSET resistor R2 determines the HP-LP transition level at $V_{\text{SNSBOOST}} = 2.5$ V. The LP-BM transition level at $V_{\text{SNSBOOST}} = 1.3$ V can be selected via another preset resistor, $R_{\text{SNSOUT1}}$. Figure 7 shows the overall LP-BM transition curve to one selected setting.

**Table 3. Settings of SNSSET resistor R2**

<table>
<thead>
<tr>
<th>$R_{\text{SNSSET2}}$ (kΩ)</th>
<th>LP-BM transition level at $V_{\text{SNSBOOST}} = 2.5$ V (%)</th>
<th>HP-LP transition level (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5</td>
<td>30</td>
</tr>
<tr>
<td>6.8</td>
<td>7.5</td>
<td>30</td>
</tr>
<tr>
<td>15</td>
<td>10</td>
<td>30</td>
</tr>
<tr>
<td>27</td>
<td>12.5</td>
<td>30</td>
</tr>
<tr>
<td>47</td>
<td>5</td>
<td>20</td>
</tr>
<tr>
<td>82</td>
<td>7.5</td>
<td>20</td>
</tr>
<tr>
<td>180</td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>open</td>
<td></td>
<td>12.5</td>
</tr>
</tbody>
</table>

**Table 4. Mains compensation curve and burst frequency settings**

<table>
<thead>
<tr>
<th>$R_{\text{SNSOUT1}}$ (kΩ)</th>
<th>LP-BM transition level at $V_{\text{SNSBOOST}} = 1.3$ V (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.8</td>
<td>12.5</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>15</td>
<td>7.5</td>
</tr>
<tr>
<td>22</td>
<td>5</td>
</tr>
</tbody>
</table>

The $R_{\text{SNSOUT1}}$ resistor value is used for internal calibration as well. An accurate resistor of 1 % required (see Table 4). The output overvoltage protection level can be adjusted using the upper-side resistor ($R_{\text{SNSOUT2}}$).
Figure 7. LP-BM transition curve versus SNSBOOST pin voltage

White-filled circles: Possible LP-BM transition selections
Orange-filled circles: Selected transition level. 5 % at \( V_{\text{SNSBOOST}} = 1.3 \) V via \( R_{\text{SNSOUT1}} \) and 7.5 % at \( V_{\text{SNSBOOST}} = 2.5 \) V via \( R_{\text{SNSSET2}} \)

5.4 Capacitor value selection for the SNSSET pin

To measure the values for resistors R1 and R2 on the SNSSET pin, a capacitor is used in series with resistor R2. For reliable measurement, the value of this capacitor must be a value shown in Table 5.

Table 5. SNSSET capacitor (\( C_{\text{SNSSET}} \) (nF)) value versus resistor values

<table>
<thead>
<tr>
<th>R1 (kΩ)</th>
<th>1</th>
<th>6.8</th>
<th>15</th>
<th>27.0</th>
<th>47</th>
<th>82.0</th>
<th>180</th>
<th>open</th>
<th>R2 (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>46.4</td>
<td>33</td>
<td>33</td>
<td>33</td>
<td>33</td>
<td>33</td>
<td>22</td>
<td>12</td>
<td>n.c.</td>
<td></td>
</tr>
<tr>
<td>53.6</td>
<td>33</td>
<td>33</td>
<td>33</td>
<td>33</td>
<td>33</td>
<td>22</td>
<td>12</td>
<td>n.c.</td>
<td></td>
</tr>
<tr>
<td>61.9</td>
<td>33</td>
<td>33</td>
<td>33</td>
<td>33</td>
<td>33</td>
<td>22</td>
<td>12</td>
<td>n.c.</td>
<td></td>
</tr>
<tr>
<td>71.5</td>
<td>33</td>
<td>33</td>
<td>33</td>
<td>33</td>
<td>22</td>
<td>22</td>
<td>12</td>
<td>n.c.</td>
<td></td>
</tr>
<tr>
<td>82.5</td>
<td>33</td>
<td>33</td>
<td>33</td>
<td>22</td>
<td>22</td>
<td>22</td>
<td>12</td>
<td>n.c.</td>
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</tr>
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<td>95.3</td>
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<td>22</td>
<td>12</td>
<td>12</td>
<td>n.c.</td>
<td></td>
</tr>
<tr>
<td>110</td>
<td>22</td>
<td>22</td>
<td>22</td>
<td>22</td>
<td>22</td>
<td>12</td>
<td>12</td>
<td>n.c.</td>
<td></td>
</tr>
<tr>
<td>127</td>
<td>22</td>
<td>22</td>
<td>22</td>
<td>22</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>n.c.</td>
<td></td>
</tr>
<tr>
<td>147</td>
<td>22</td>
<td>22</td>
<td>22</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>n.c.</td>
<td></td>
</tr>
</tbody>
</table>
5.5 Transition power level modification by adding an offset to the SNSCAP signal

Normally, $R_{\text{SNSSET2}}$ and $R_{\text{SNSOUT1}}$ are chosen to set the mode transition levels. However, in some cases, the options in the table do not meet the requirements. For example, when transitions must be set at a very low power level. When a voltage offset is added to SNSCAP, the values can be changed to meet the requirements. This offset shifts the total power range. However, it has a greater effect on the lower power region (near LP-to-BM transition) than on the higher power region (100 % level).

The SNSCAP pin can be connected to the voltage on the auxiliary winding using resistor $R_{\text{OFFSET}}$ and capacitor $C_{\text{OFFSET}}$. It adds a voltage to the SNSCAP signal for both polarities of the SNSCAP signal. The winding direction of the auxiliary winding determines if an offset is added or subtracted.

The value of the auxiliary voltage and the value of $R_{\text{OFFSET}}$ determine the amount of offset on SNSCAP. Capacitor $C_{\text{OFFSET}}$ provides the AC coupling of the offset signal. The value of $C_{\text{OFFSET}}$ must allow correct timing for the function.

Although it has less effect on the higher power region, the overpower level must be double-checked after adding an offset.

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![Figure 8. Addition an offset on SNSCAP to modify mode transition power levels](image-url)
6 Presetting optimization example

6.1 Mains compensation curve design example

The mains compensation curve is selected based on overpower protection requirement. Figure 9 shows a practical design example for overpower protection level. Where the overpower protection curve with the compensation curve 3 must still improve the compensation, compensation curve 4 can achieve a better overpower protection curve versus the mains input voltage.

![Graph showing mains compensation curves](image)

Figure 9. Practical example of overpower protection level with different curves

Figure 10 shows the influence of the mode transition levels (HP-LP transition and LP-BM transition) on different mains compensation curves. Regarding the overpower protection compensation result, curve 4 is the more compensated option for mode transition levels.
6.2 LP-BM transition optimization example

Section 6.1 shows that a compensation curve option compensates the LP-BM transition level. If the compensated LP-BM transition level must still optimize for less input voltage influence, the transition level can be adjusted with \( R_{\text{SNSOUT1}} \) and \( R_{\text{SNSSET2}} \). Figure 11 shows LP-BM transition level example with different options. The option which is 7.5% at \( V_{\text{SNSBOOST}} = 1.3 \text{ V} \) and 5% at \( V_{\text{SNSBOOST}} = 2.5 \text{ V} \) shows the most optimized LP-BM transition level curve. When selecting an LP-BM transition level, the standby power consumption and the audible noise in burst mode must be considered as well.
The LP-BM transition power level is closely related to standby power consumption. Figure 12 shows a practical example where the standby power consumption is improved with different LP-BM transition options. The 22 kΩ value of $R_{SNSOUT1}$ sets a 5 % LP-BM transition level at $V_{SNSBOOST} = 1.3$ V. The practical LP-BM transition power level at 150 V (AC) is much lower than 1 W. So, the standby power consumption at 150 V (AC) is much higher than other mains input conditions. After the LP-BM transition level at $V_{SNSBOOST} = 1.3$ V is increased to 7.5 % with $R_{SNSOUT1} = 15$ kΩ, the standby power consumption is improved.
6.3 Audible noise

The LLC transformer is the main source of audible noise. Audible noise does not happen in high-power mode because the switching frequency well exceeds the audible frequency. However, in burst mode, the repetition frequency of the bursts is in the audible frequency range. The TEA9026T can be set to a steady repetition frequency of 1600 Hz or 800 Hz. This operation can generate audible noise.

The LP mode enables the system to keep switching above the audible frequency even at low output power levels. Since the minimum low-power mode repetition frequency is 28 kHz, this frequency value does not generate audible noise. However, unstable low-power repetition frequency because of jumping between a different number of peaks can generate audible noise.
The wide input voltage range results in a longer turn-on time at lower input voltages. It increases the magnetizing current and so the level of audible noise in burst mode and low-power mode.

The sections below introduce possible improvements in burst mode and LP mode. However, improvement for audible noise often results in more power consumption at low output power and higher output voltage ripple. Sometimes, a compromise for acceptable performance on related subjects must be found. The TEA9026T offers many options to optimize mode operation transitions that can help to achieve the best performance-combination in all working conditions.

6.3.1 Audible noise improvement in burst mode

When audible noise occurs in burst mode, several possible improvements can be considered.

Lowering the LP-BM transition level reduces the energy level in each burst-mode cycle, which improves audible noise. Resistors $R_{SNSOUT1}$ and $R_{SNSSET2}$ adjust the LP-BM transition level (see Section 6.2). If the options on $R_{SNSOUT1}$ and $R_{SNSSET2}$ are not sufficient to optimize audible noise (see Section 5.5), the adding offset level on SNSCAP can adjust the LP-BM transition level more accurately. Typically, the $R_{OFFSET}$ value decides the level of offset. Using this method, the LP-BM transition values that are best suited for the application to be designed can be created.

The main mechanism for producing noise is the interruption of magnetization current sequences (bursts), which leads to a mechanical force. The core of the resonant transformer is especially susceptible and starts acting like a loudspeaker. The noise amplitude is highest at the (mechanical) resonant frequency of the transformer. Normally, the resonant frequency of the transformer is a higher frequency than the burst repetition frequency.

Harmonics of the burst repetition frequency produce the audible noise. A lower repetition burst frequency reduces the energy in the harmonics at the resonant frequency of the transformer. So, the lower burst repetition frequency improves the audible noise. Throughout $R_{SNSSET1}$, 800 Hz or 1600 Hz burst frequency can be selected.

6.3.2 Audible noise improvement in low-power mode

When the LP repetition frequency is unstable in combination with higher magnetizing current, audible noise happens in low-power mode. Likewise, in burst mode, audible noise is the most critical at the lowest input voltage level. A reduction of input voltage requirement can improve audible noise.

Lowering the HP-LP mode transition level and reducing the LP operation power range can improve audible noise. $R_{SNSSET2}$ presets the HP-LP transition level between 30 % and 20 %. If the 20 % HP-LP mode transition level option is not sufficient, adding an offset level on SNSCAP can adjust the HP-LP transition level.
7 Abbreviations

Table 6. Abbreviations

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>MOSFET</td>
<td>metal-oxide semiconductor field-effect transistor</td>
</tr>
<tr>
<td>PCB</td>
<td>printed-circuit board</td>
</tr>
<tr>
<td>PFC</td>
<td>power factor correction</td>
</tr>
<tr>
<td>THD</td>
<td>total harmonic distortion</td>
</tr>
<tr>
<td>UVLO</td>
<td>undervoltage lockout</td>
</tr>
</tbody>
</table>

8 References

[1] AN11801 application note — TEA19161 and TEA19162 controller ICs, revision 2.1; 2021, NXP Semiconductors
[2] TEA9026T data sheet — Digital LLC controller for power supplies providing wide input voltage range and low standby; 2022, NXP Semiconductors
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