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<tr>
<td>Keywords</td>
<td>QN908x, errata</td>
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## Revision history

<table>
<thead>
<tr>
<th>Rev</th>
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<tbody>
<tr>
<td>00.01</td>
<td>20160809</td>
<td>Initial draft</td>
</tr>
<tr>
<td>00.02</td>
<td>20160901</td>
<td>Reviewed internally and updated</td>
</tr>
<tr>
<td>00.03</td>
<td>20161125</td>
<td>Removed some issue after Metal fix</td>
</tr>
<tr>
<td>00.04</td>
<td>20170307</td>
<td>Change document name and version</td>
</tr>
<tr>
<td>00.06</td>
<td>20170427</td>
<td>Update from v00.04, add RTC in errata, change TSC name into CS</td>
</tr>
<tr>
<td>1.0</td>
<td>20170601</td>
<td>Change document revision number to 1.0</td>
</tr>
<tr>
<td>1.1</td>
<td>20180223</td>
<td>ESD issue fixed</td>
</tr>
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</table>

## Contact information

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For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)
1. Introduction

This document describes QN908x errata which should be referred by customer while application development.

2. Product Identification

The QN9080 HVQFN package has the following top-side marking:
- Line A: “9080” for QN9080
- Line B1: xxxxxx
- Line B2: xxxx
- Line C: xxYYWW[R]
  - WW: week code.
  - R = Chip revision.

The QN9083 WLCSP package has the following top-side marking:
- Line A: “9083” for QN9083
- Line B1: xxxxxx

![HVQFN48 package marking](image1)

![WLCSP47 package marking](image2)
• Line B2: xxWW
  – WW: week code.
• Line C: YY[R]x
  – R = Chip revision.

Table 1. Revision overview table

<table>
<thead>
<tr>
<th>Revision identifier</th>
<th>Revision description</th>
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</thead>
<tbody>
<tr>
<td>’A’</td>
<td>Initial device revision</td>
</tr>
<tr>
<td>’B’</td>
<td>First metal fix revision</td>
</tr>
<tr>
<td>’C’</td>
<td>Second metal fix revision</td>
</tr>
<tr>
<td>’D’</td>
<td>ESD problem fixed</td>
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3. Errata Overview

Table 2. Errata summary table

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<thead>
<tr>
<th>Erratum ID</th>
<th>Short description</th>
<th>Product version(s)</th>
<th>Detailed description</th>
</tr>
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<tbody>
<tr>
<td>FSP.1</td>
<td>FIR coefficient can only be saved in low 64K SRAM</td>
<td>‘A’, ‘B’, ‘C’, and ‘D’</td>
<td>Section 4.1</td>
</tr>
<tr>
<td>FC.1</td>
<td>Flexcomm (0~3) interrupt can’t be wakeup source in sleep mode if SLEEPDEEP bit of</td>
<td>‘A’, ‘B’, ‘C’, and ‘D’</td>
<td>Section 4.2</td>
</tr>
<tr>
<td></td>
<td>Cortex-M4 SCR register is 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>COMPARATOR.1</td>
<td>Comparator can’t work correctly under some condition</td>
<td>‘A’, ‘B’, ‘C’, and ‘D’</td>
<td>Section 4.4</td>
</tr>
<tr>
<td>COMPARATOR.2</td>
<td>Comparator can’t work correctly under some condition</td>
<td>‘A’, ‘B’, ‘C’, and ‘D’</td>
<td>Section 4.5</td>
</tr>
<tr>
<td>CS.1</td>
<td>SCAN_INTEN register cannot be read</td>
<td>‘A’, ‘B’, ‘C’, and ‘D’</td>
<td>Section 4.6</td>
</tr>
<tr>
<td>RTC.1</td>
<td>SEC, CNT_VAL and CNT2 register reading may return invalid values when happens at</td>
<td>‘A’, ‘B’, ‘C’, and ‘D’</td>
<td>Section 4.7</td>
</tr>
<tr>
<td></td>
<td>32k clock positive edge</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESD.1</td>
<td>DCDC does not meet the required 2 kV ESD HBM specification</td>
<td>‘A’, ‘B’, and ‘C’</td>
<td>Section 4.8</td>
</tr>
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4. Errata Details

4.1 FSP.1: FIR coefficients can only be stored in low 64K SRAM

Introduction:
FIR coefficients can be stored anywhere in the 128K SRAM, and FIR engine will read it for computation.

Problem:
The FIR coefficient base address register (FIR.CH<x>_COEF_BASE, x = 0-8) is only 16 bit, which means only 64K SRAM is accessible. If the FIR coefficient is saved in high 64K, FIR can’t fetch it.

Work-arounds:
Coefficient can only be stored in low 64K SRAM.

4.2 FC.1: Flexcomm (0~3) interrupt can’t be wakeup source in sleep mode if SLEEPDEEP bit of Cortex-M4 SCR register is 1

Introduction:
Flexcomm (0~3) interrupt should be a wakeup source in sleep mode, no matter what value the SLEEPDEEP bit of Cortex-M4 System Control Register (SCR) is.

Problem:
Flexcomm (0-3) can’t wake up MCU from sleep mode if the SLEEPDEEP bit in SCR is 1.

Work-arounds:
If Flexcomm are used as wakeup source, set SLEEPDEEP bit as 0 in sleep mode. The power saving from SLEEPDEEP=1 is negligible.

4.3 FC.2: TXIDLE bit error in USART synchronous slave mode

Introduction:
TXIDLE bit in USART Status register (STAT) should be 1 after transmit is finished in synchronous slave mode.

Problem:
When USART works in synchronous slave mode, TXIDLE bit in USART Status register (STAT) is set one cycle after transmit completes. The TXIDLE signal is not asserted correctly if the synchronous CLK from USART master doesn’t provide that extra clock cycle.

Work-arounds:
Ignore the TXIDLE bit in synchronous slave mode. Use the buffer status as the indication of transmit completion.

4.4 COMPARATOR.1: Comparator cannot work correctly under some condition

Introduction:
Comparator should work well when internal reference is VCC*(15/16).

Problem:
When $VCC \leq 1.8V$ and one of the analog comparator input is selected as internal reference=$VCC \times (15/16)$, the analog comparator does not function correctly. The analog comparator result does not change to logic “1” even if another input is $> VCC \times (15/16)$.

**Work-arounds:**

No work-arounds.

### 4.5 COMPARATOR.2: Comparator cannot work correctly under some condition

**Introduction:**

Comparator should work well when internal reference is $(1/16) \times VCC$.

**Problem:**

When $VCC \leq 1.8V$ and one of the analog comparator input is selected as internal reference=$VCC \times (1/16)$, the analog comparator does not function correctly. The analog comparator result does not change to logic “1” even if another input is $> VCC \times (1/16)$.

**Work-arounds:**

No work-arounds.

### 4.6 CS.1: SCAN_INTEN register cannot be read back correctly

**Introduction:**

SCAN_INTEN register, bit 3 in address $0x4000780C$ should be RMW correctly.

**Problem:**

SCAN_INTEN register, bit 3 in address $0x4000780C$ can’t be read by MCU. This bit will always read back 0. If read-modify-write is used to modify this register, this bit will be written as 0.

**Work-arounds:**

Software should keep track of this register value. Always modify on the software saved value rather than read-back value when changing this register.

### 4.7 RTC.1: SEC, CNT_VAL, CNT2 register read return invalid value

**Introduction:**

Reading SEC, CNT_VAL and CNT2 registers, may return invalid values when it happens at the edge of 32K clock.

**Problem:**

These registers are 32k domain register, and they are mapping to APB clock domain. There is only a stage of synchronization of these registers. So when the reading operation happens at the edge of the 32K clock, the reading back value may be invalid.

**Work-arounds:**

Software need to read more times, when get 2 same value. It should be the correct one.
4.8 ESD.1: DCDC does not meet the required 2 kV ESD HBM specification

Introduction:
The chip is rated for 2 kV ESD HBM. ESD HBM stressed as highlighted a weakness in the DCDC IP.

Problem:
DCDC IP is passing ESD-HBM stress at 500V and failing above. When stressing the device with a level above 500V, DCDC IP will be damaged but the device is fully functional when the DCDC is using external power supplies.

Work-arounds:
This problem is fixed in Rev. D.
For the earlier reversions, it is not recommended to enable the DCDC. In such case, make sure to connect the VCC/VVD1/VDD2/VDD3 pins all together.
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