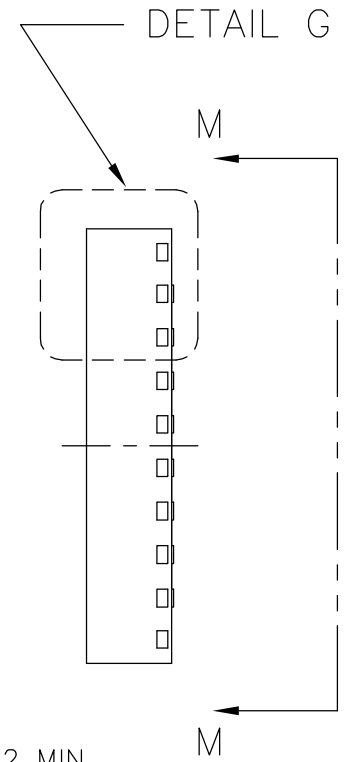
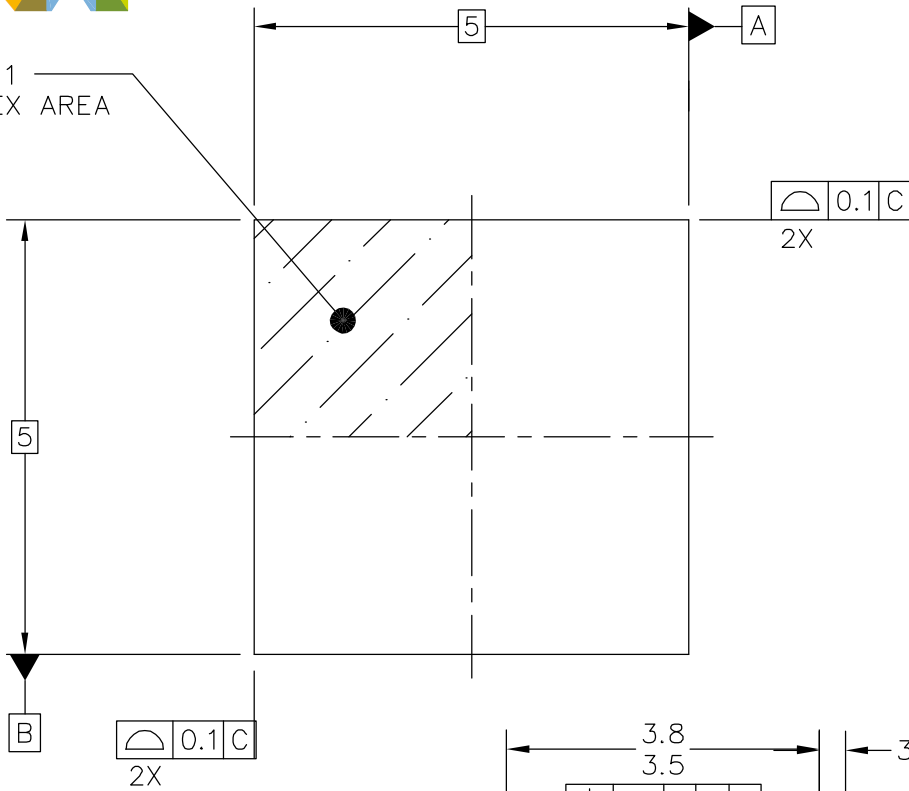
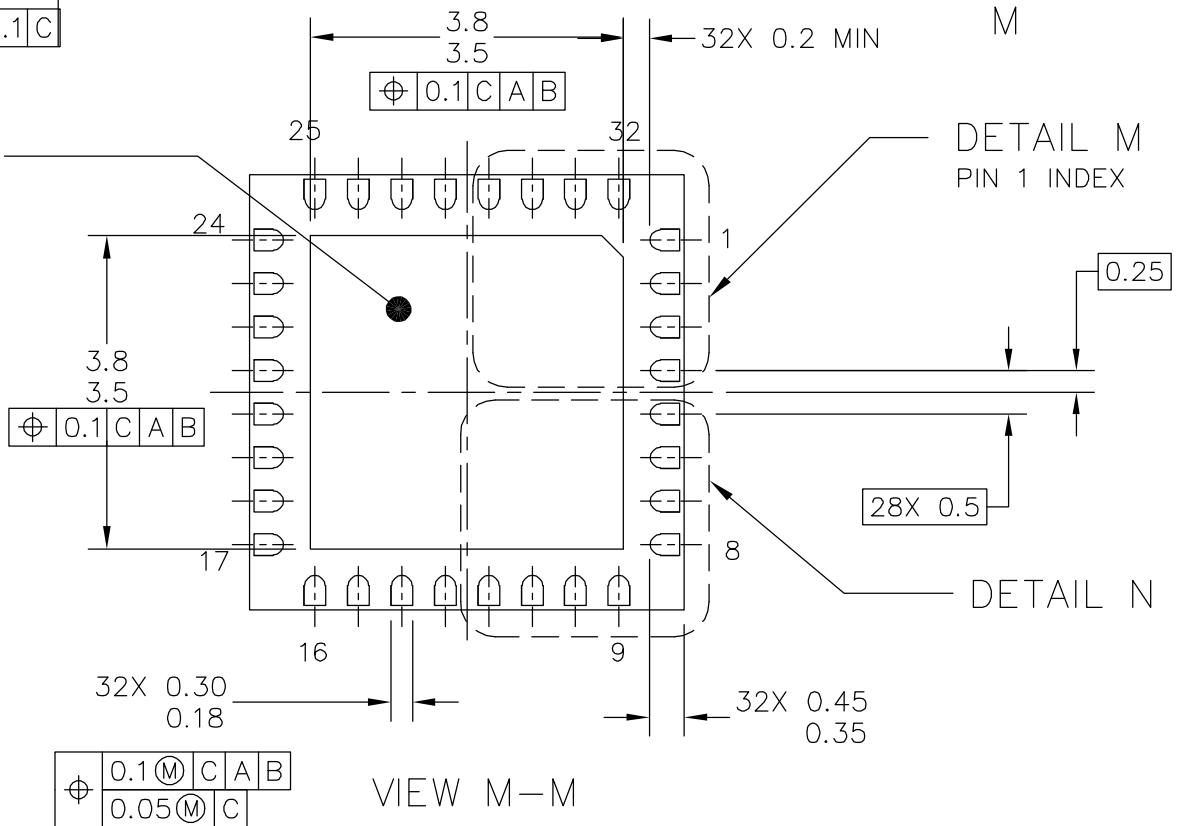




PIN 1 INDEX AREA

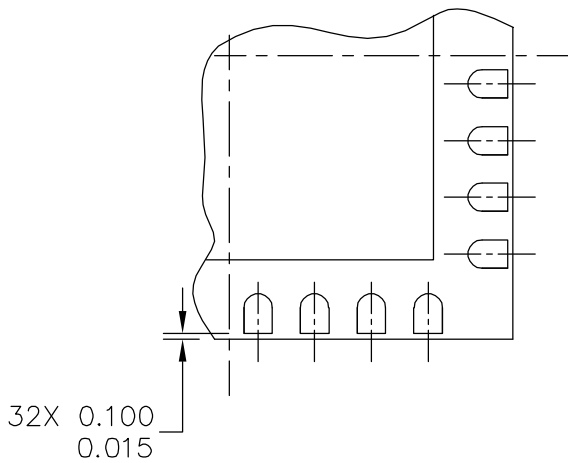


EXPOSED DIE ATTACH PAD

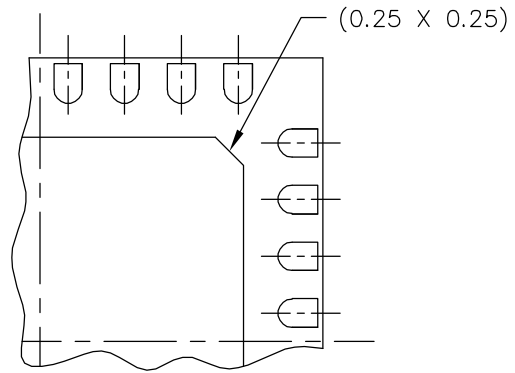


VIEW M-M

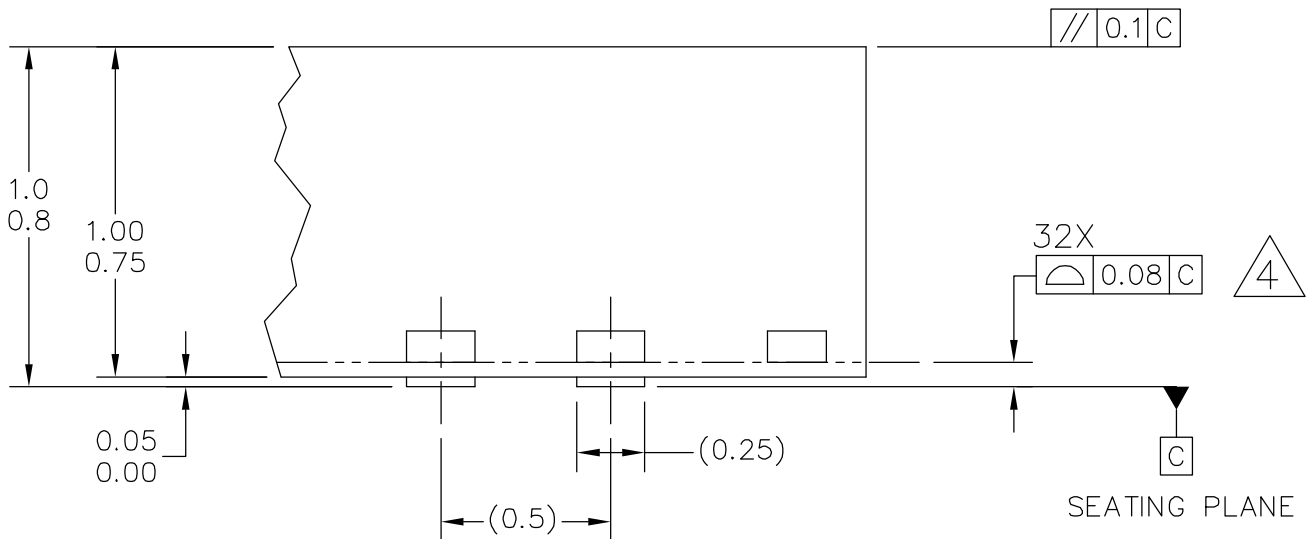
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<p>TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 32 TERMINAL, 0.5 PITCH (5 X 5 X 1) 3.6 X 3.6 EP, CASE OUTLINE</p>	<p>DOCUMENT NO: 98ARE10566D REV: D</p>	
	<p>STANDARD: JEDEC MO-220 VHHD-4</p>	
	<p>SOT617-14</p>	<p>01 FEB 2016</p>



DETAIL N
PREFERRED CORNER CONFIGURATION



DETAIL M
PREFERRED BACKSIDE PIN 1 INDEX




DETAIL G
VIEW ROTATED 90° CW

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		STANDARD: JEDEC MO-220 VHHD-4	
		SOT617-14	01 FEB 2016



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFN.
4.  COPLANARITY APPLIES TO LEADS, AND DIE ATTACH PAD.
5. MINIMUM METAL GAP SHOULD BE 0.2 MM.

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	SOT617-14	01 FEB 2016