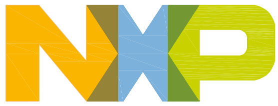


PIN 1 INDEX AREA

9

A

0.1 C

2X

DETAIL G

M

9

B

0.1 C

2X

M

7.25
6.95

0.1 C A B

(4)

(3.7)

DETAIL M
PIN1 INDEX

49 64

48 1

EXPOSED PAD

0.25

7.25
6.95

0.1 C A B

(6.2)

(6.5)

60X 0.5

33 16

DETAIL N

64X 0.30
0.18

32 17

0.1 Ⓜ C A B
0.05 Ⓜ C

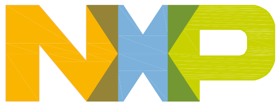
64X 0.5
0.3

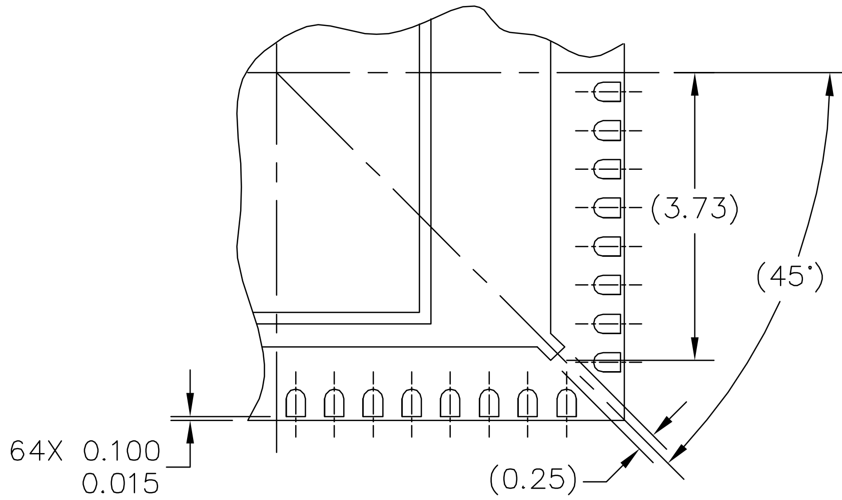
VIEW M–M

© NXP SEMICONDUCTORS N.V.
ALL RIGHTS RESERVED

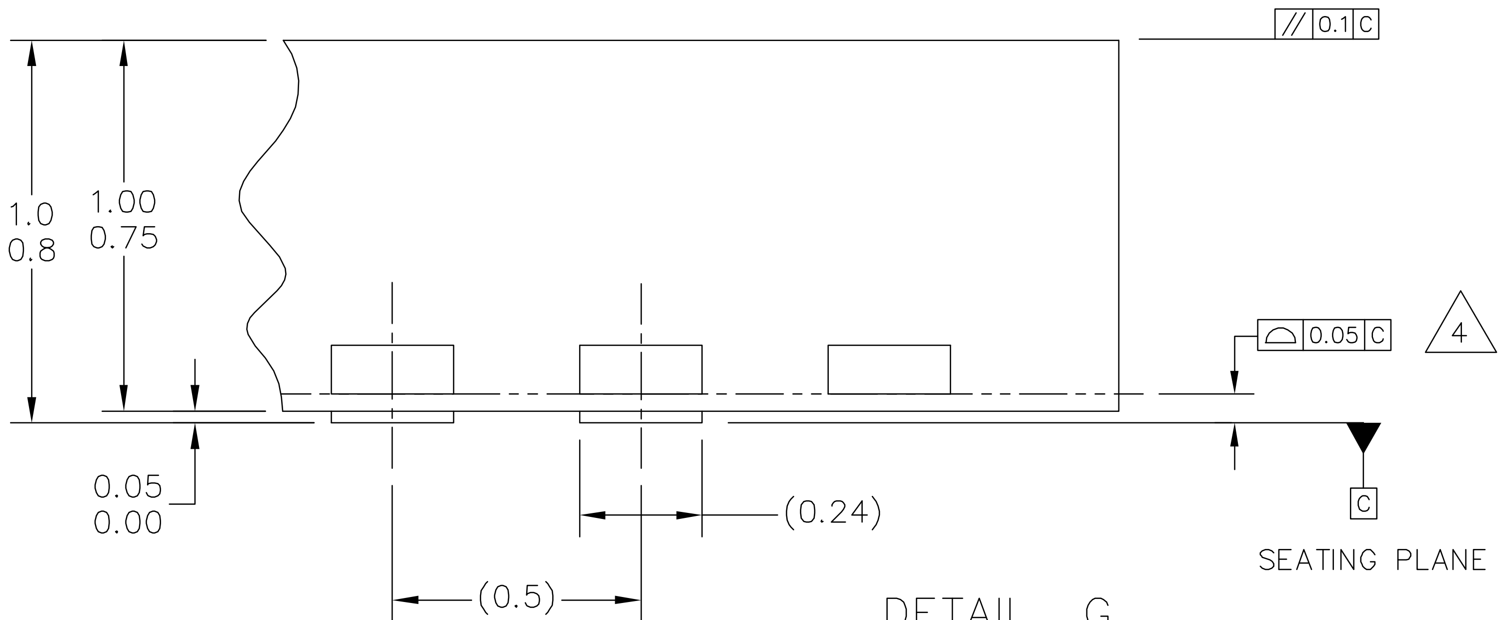
MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)	DOCUMENT NO: 98ARE10599D REV: B
	STANDARD: NON–JEDEC
	SOT804–6 01 FEB 2016



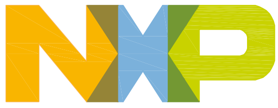


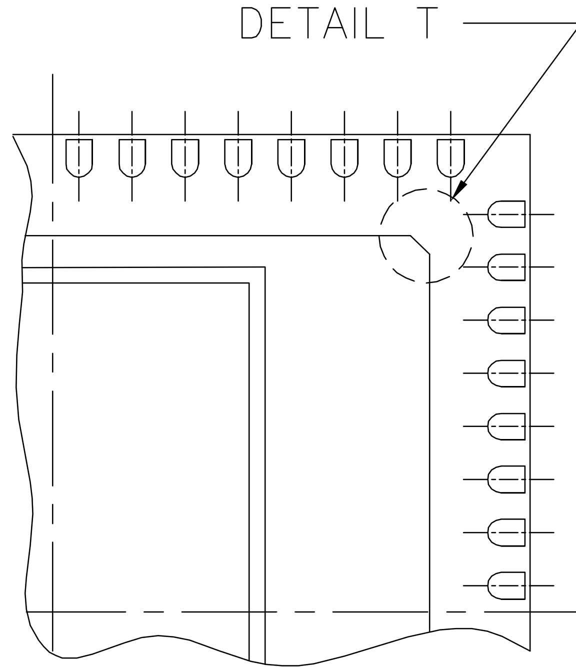
DETAIL N
CORNER CONFIGURATION



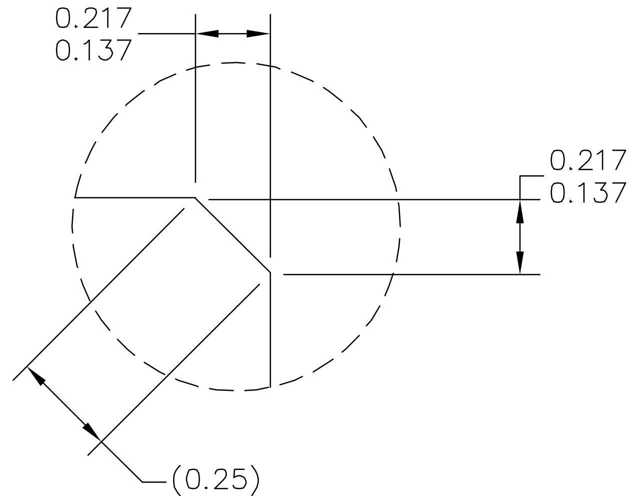
DETAIL G
VIEW ROTATED 90° CW

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)	DOCUMENT NO: 98ARE10599D	REV: B
	STANDARD: NON-JEDEC	
	SOT804-6	01 FEB 2016





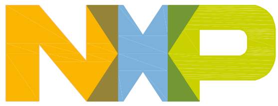
DETAIL M
PIN 1 BACKSIDE IDENTIFIER

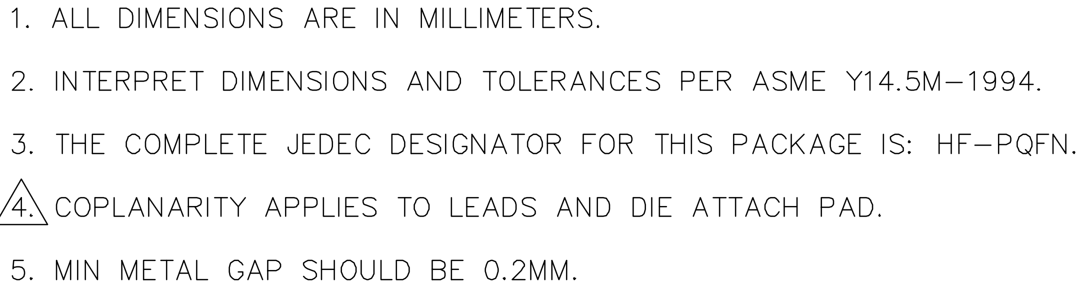


DETAIL T
PIN 1 BACKSIDE IDENTIFIER

© NXP SEMICONDUCTORS N.V.
ALL RIGHTS RESERVED

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)	DOCUMENT NO: 98ARE10599D REV: B
	STANDARD: NON-JEDEC
	SOT804-6 01 FEB 2016





NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. (△) COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)	DOCUMENT NO: 98ARE10599D	REV: B
	STANDARD: NON–JEDEC	
	SOT804–6	01 FEB 2016