

# OL-PCA9410

wafer level chip-scale package; 9 bumps; 1.24 x 1.24 x 0.525 mm (backside coating included)

8 February 2016

Package information

## 1. Package summary

<b>Terminal position code</b>	B (bottom)
<b>Package type descriptive code</b>	WLCSP
<b>Package type industry code</b>	WLCSP9
<b>Package style descriptive code</b>	UC (uncased chip)
<b>Package style suffix code</b>	NA (not applicable)
<b>Package body material type</b>	P (plastic)
<b>Mounting method type</b>	S (surface mount)
<b>Issue date</b>	23-7-2015

Table 1. Package summary

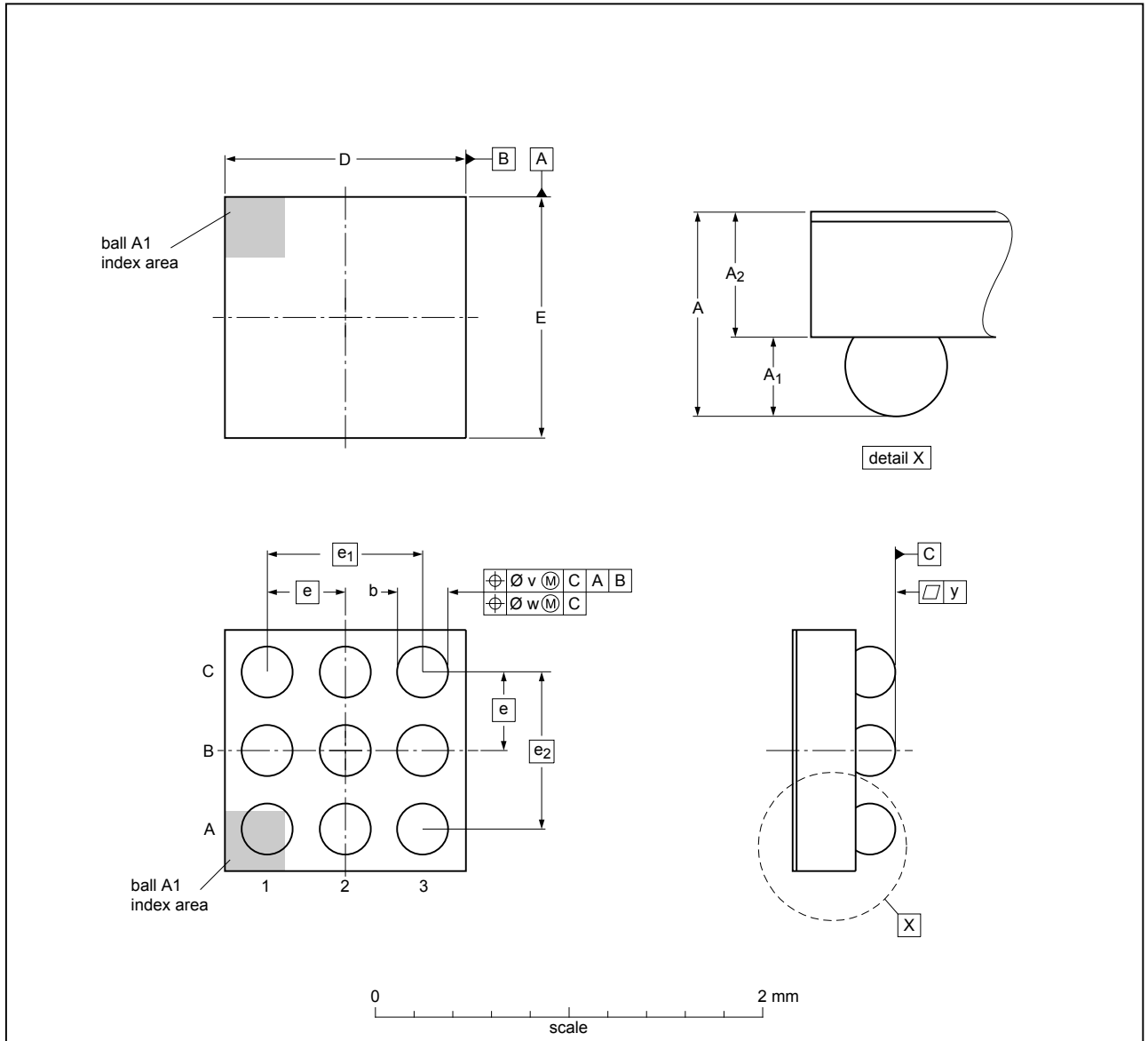
Symbol	Parameter	Min	Typ	Nom	Max	Unit
D	package length	1.21	-	1.24	1.27	mm
E	package width	1.21	-	1.24	1.27	mm
A	seated height	0.485	-	0.525	0.565	mm
A <sub>2</sub>	package height	0.3	-	0.325	0.35	mm
e	nominal pitch	-	-	0.4	-	mm
n <sub>2</sub>	actual quantity of termination	-	-	9	-	



wafer level chip-scale package; 9 bumps; 1.24 x 1.24 x 0.525 mm (backside coating included)

## 2. Package outline

WLCSP9: wafer level chip-scale package; 9 bumps; 1.24 x 1.24 x 0.525 mm (backside coating included) PCA9410



Dimensions (mm are the original dimensions)

Unit	A	A <sub>1</sub>	A <sub>2</sub>	b	D	E	e	e <sub>1</sub>	e <sub>2</sub>	v	w	y
max	0.565	0.23	0.350	0.29	1.27	1.27						
nom	0.525	0.20	0.325	0.26	1.24	1.24	0.4	0.8	0.8	0.15	0.05	0.05
min	0.485	0.17	0.300	0.23	1.21	1.21						

Note: Backside coating 25 µm

wlcs9\_pca9410\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
PCA9410					-14-09-01- 15-07-23

Fig. 1. Package outline WLCSP9 (OL-PCA9410)

wafer level chip-scale package; 9 bumps; 1.24 x  
1.24 x 0.525 mm (backside coating included)

### 3. Legal information

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