

# OL-TFA9897B

wafer level chip-scale package; 30 bumps; 2.06 x 2.72 x 0.525 mm (backside coating included)

8 February 2016

Package information

## 1. Package summary

|                                       |                     |
|---------------------------------------|---------------------|
| <b>Terminal position code</b>         | B (bottom)          |
| <b>Package type descriptive code</b>  | WLCSP               |
| <b>Package type industry code</b>     | WLCSP30             |
| <b>Package style descriptive code</b> | UC (uncased chip)   |
| <b>Package style suffix code</b>      | NA (not applicable) |
| <b>Package body material type</b>     | P (plastic)         |
| <b>Mounting method type</b>           | S (surface mount)   |
| <b>Issue date</b>                     | 13-3-2015           |

Table 1. Package summary

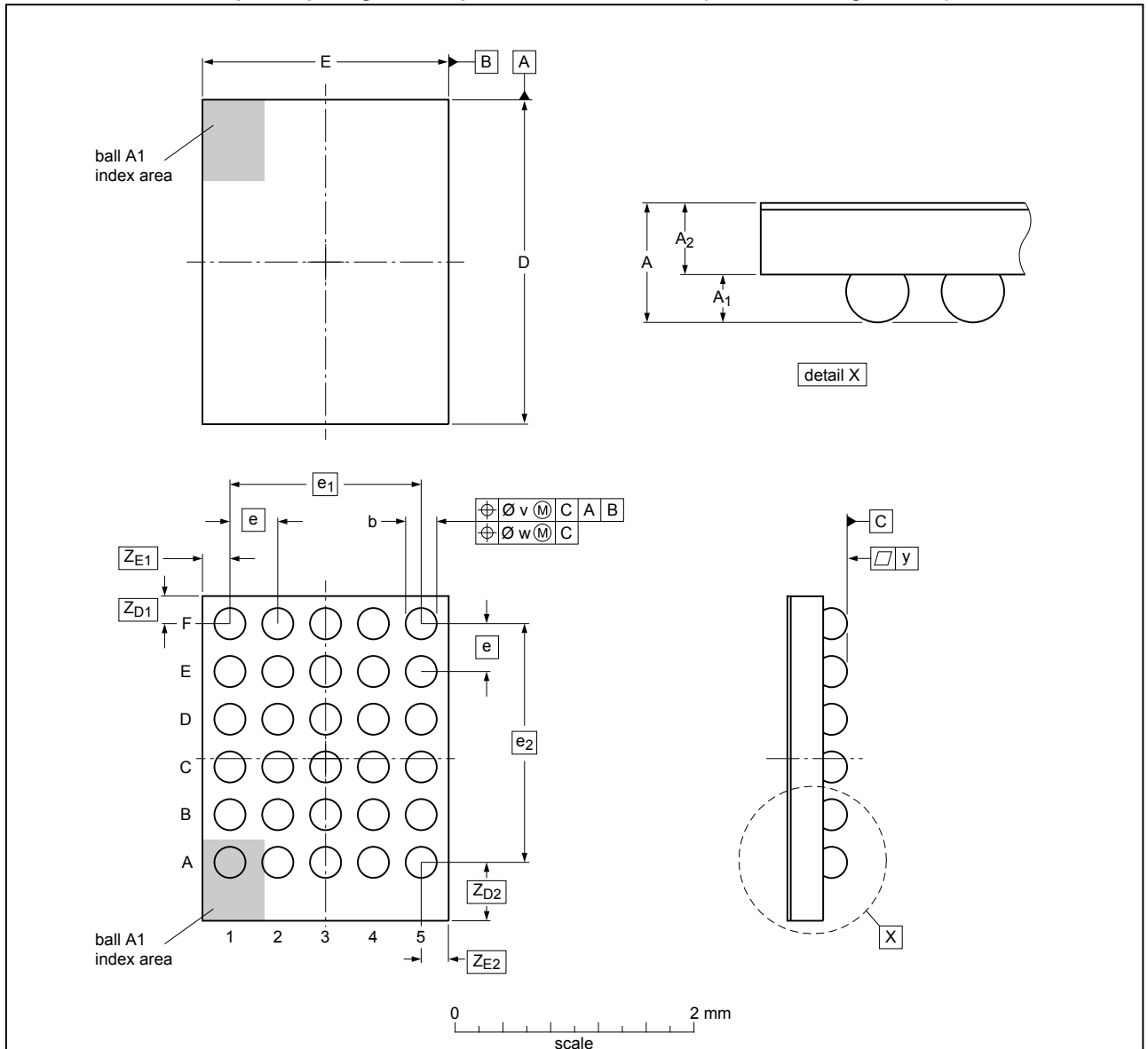
| Symbol         | Parameter                      | Min   | Typ | Nom   | Max   | Unit |
|----------------|--------------------------------|-------|-----|-------|-------|------|
| D              | package length                 | 2.69  | -   | 2.72  | 2.75  | mm   |
| E              | package width                  | 2.03  | -   | 2.06  | 2.09  | mm   |
| A              | seated height                  | 0.485 | -   | 0.525 | 0.565 | mm   |
| A <sub>2</sub> | package height                 | -     | -   | 0.33  | -     | mm   |
| e              | nominal pitch                  | -     | -   | 0.4   | -     | mm   |
| n <sub>2</sub> | actual quantity of termination | -     | -   | 30    | -     |      |



wafer level chip-scale package; 30 bumps; 2.06 x 2.72 x 0.525 mm (backside coating included)

## 2. Package outline

WLCSP30: wafer level chip-scale package; 30 bumps; 2.06 x 2.72 x 0.525 mm (backside coating included) TFA9897B



Dimensions (mm are the original dimensions)

| Unit   | A     | A <sub>1</sub> | A <sub>2</sub> | b    | D    | E    | e   | e <sub>1</sub> | e <sub>2</sub> | Z <sub>D1</sub> | Z <sub>D2</sub> | Z <sub>E1</sub> | Z <sub>E2</sub> | v    | w    | y    |
|--------|-------|----------------|----------------|------|------|------|-----|----------------|----------------|-----------------|-----------------|-----------------|-----------------|------|------|------|
| max    | 0.565 |                |                |      | 2.75 | 2.09 |     |                |                |                 |                 |                 |                 |      |      |      |
| mm nom | 0.525 | 0.20           | 0.33           | 0.26 | 2.72 | 2.06 | 0.4 | 1.6            | 2.0            | 0.23            | 0.49            | 0.23            | 0.23            | 0.05 | 0.02 | 0.03 |
| min    | 0.485 |                |                |      | 2.69 | 2.03 |     |                |                |                 |                 |                 |                 |      |      |      |

Note: Backside coating 25 µm

wlcs30\_tfa9897b\_po

| Outline version | References |       |       | European projection | Issue date           |
|-----------------|------------|-------|-------|---------------------|----------------------|
|                 | IEC        | JEDEC | JEITA |                     |                      |
| TFA9897B        |            |       |       |                     | 15-02-13<br>15-03-13 |

Fig. 1. Package outline WLCSP30 (OL-TFA9897B)

wafer level chip-scale package; 30 bumps; 2.06 x  
2.72 x 0.525 mm (backside coating included)

### 3. Legal information

#### Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

wafer level chip-scale package; 30 bumps; 2.06 x 2.72 x 0.525 mm (backside coating included)

## 4. Contents

---

|                           |   |
|---------------------------|---|
| 1. Package summary.....   | 1 |
| 2. Package outline.....   | 2 |
| 3. Legal information..... | 3 |

---

© NXP Semiconductors N.V. 2016. All rights reserved

For more information, please visit: <http://www.nxp.com>  
For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)  
Date of release: 8 February 2016

---