

# SOT1375-4

WLCSP4, wafer level chip-scale package, 4 terminals, 1.03 mm x 0.94 mm x 0.5 mm body

20 September 2017

Package information

## 1. Package summary

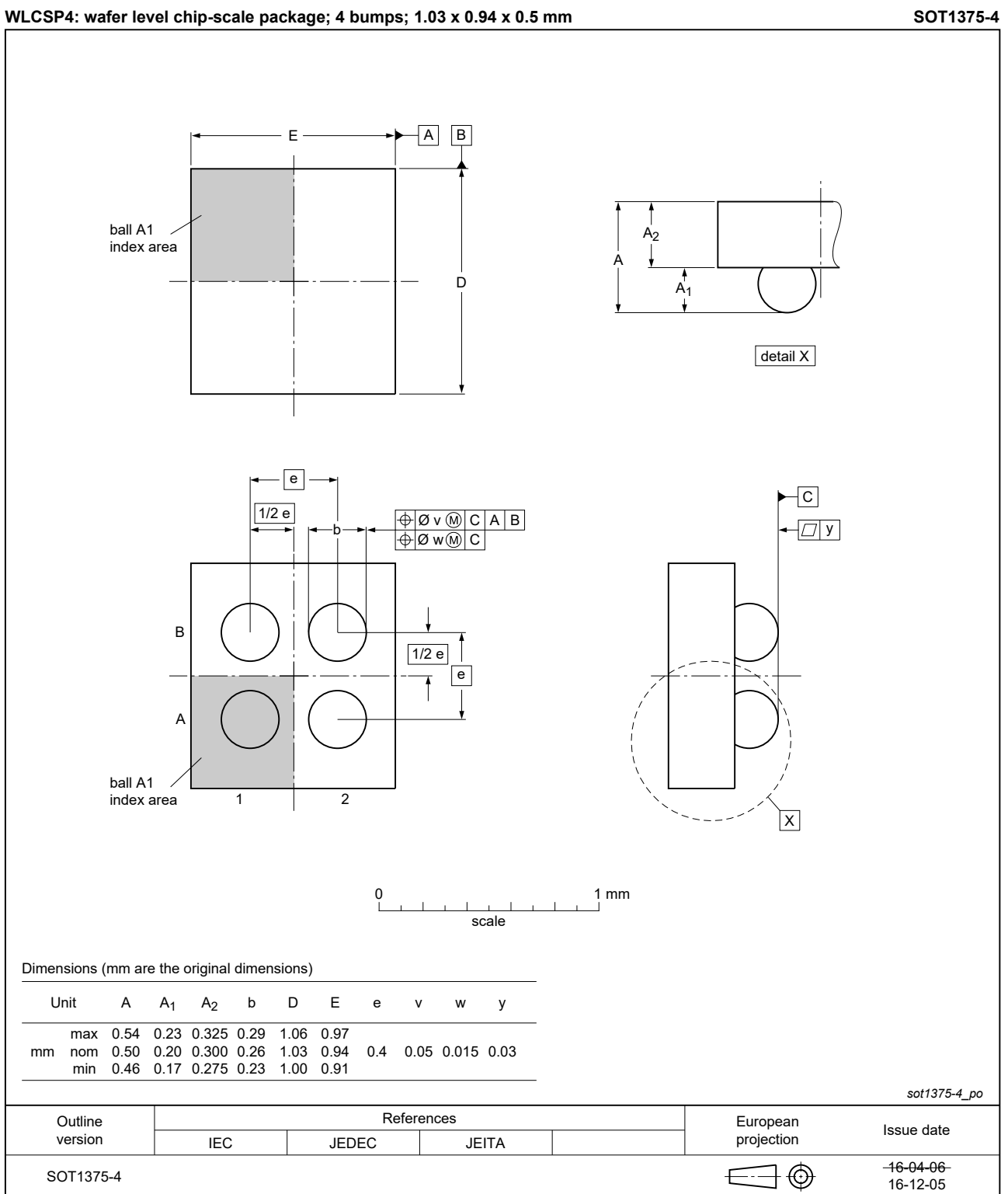
<b>Terminal position code</b>	B (bottom)
<b>Package type descriptive code</b>	WLCSP4
<b>Package type industry code</b>	WLCSP4
<b>Package style descriptive code</b>	WLCSP (wafer level chip-size package)
<b>Mounting method type</b>	S (surface mount)
<b>Issue date</b>	26-4-2016
<b>Manufacturer package code</b>	SOT1375-4

Table 1. Package summary

Symbol	Parameter	Min	Typ	Nom	Max	Unit
D	package length	1	-	1.03	1.06	mm
E	package width	0.91	-	0.94	0.97	mm
A	seated height	0.46	-	0.5	0.54	mm
A <sub>2</sub>	package height	0.275	-	0.3	0.325	mm
e	nominal pitch	-	-	0.4	-	mm
n <sub>2</sub>	actual quantity of termination	-	-	4	-	A/A

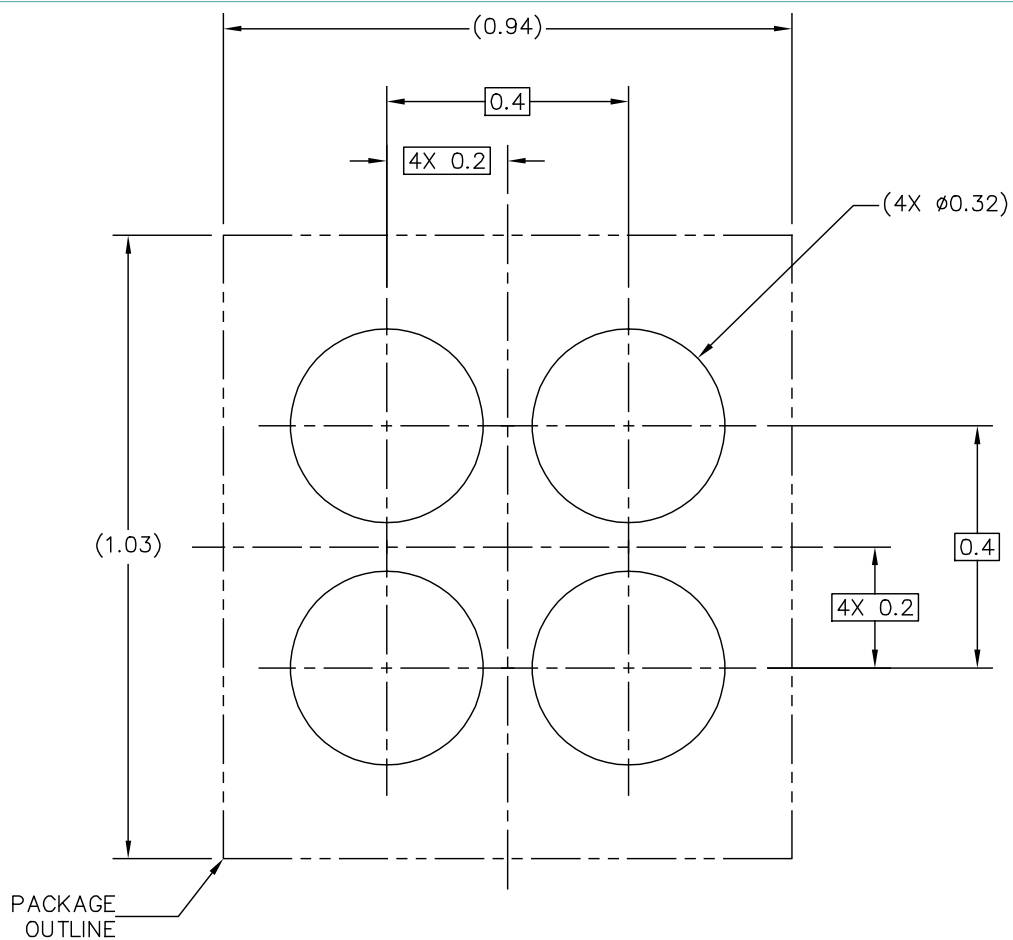


## 2. Package outline



**Fig. 1. Package outline WLCSP4 (SOT1375-4)**

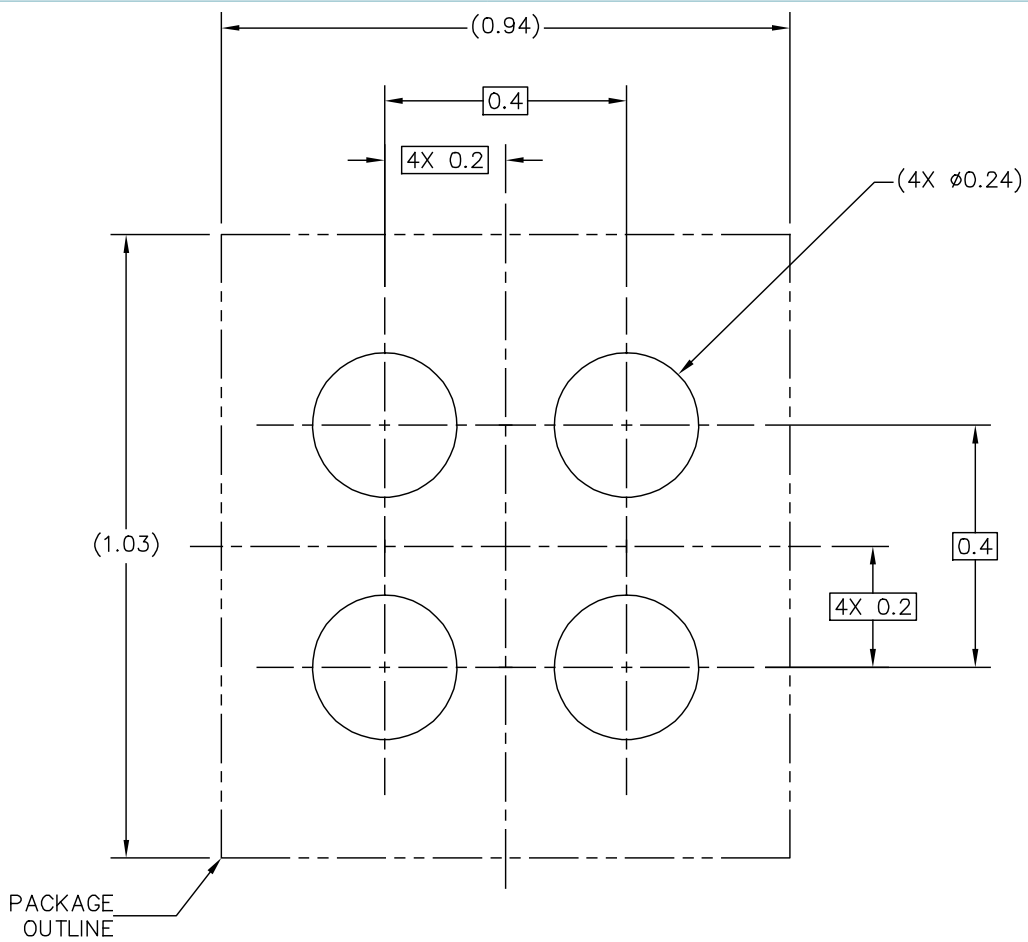
### 3. Soldering



#### PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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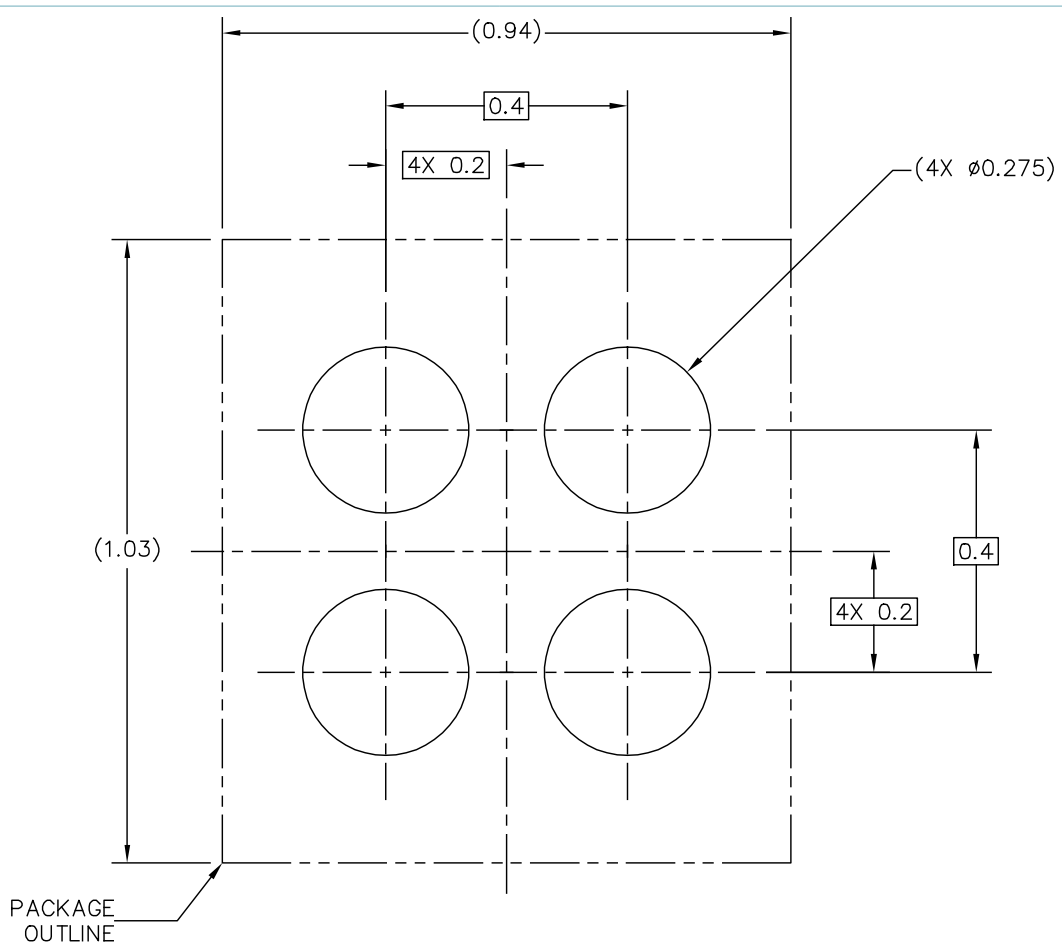
**Fig. 2. Reflow soldering footprint for WLCSP4 (SOT1375-4)**



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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**Fig. 3. Reflow soldering footprint part2 for WLCSP4 (SOT1375-4)**



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Fig. 4. Reflow soldering footprint part3 for WLCSP4 (SOT1375-4)

## 4. Legal information

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