

# SOT1375-6

WLCSP4, wafer level chip-scale package, 4 terminals, 0.4 mm pitch, 0.91 mm x 0.855 mm x 0.455 mm body (backside coating included)

5 August 2022

Package information

## 1 Package summary

<b>Terminal position code</b>	B (bottom)
<b>Package type descriptive code</b>	WLCSP4
<b>Package style descriptive code</b>	WLCSP (wafer level chip-size package)
<b>Package body material type</b>	P (plastic)
<b>Mounting method type</b>	S (surface mount)
<b>Issue date</b>	15-07-2022
<b>Manufacturer package code</b>	98ASA01775D

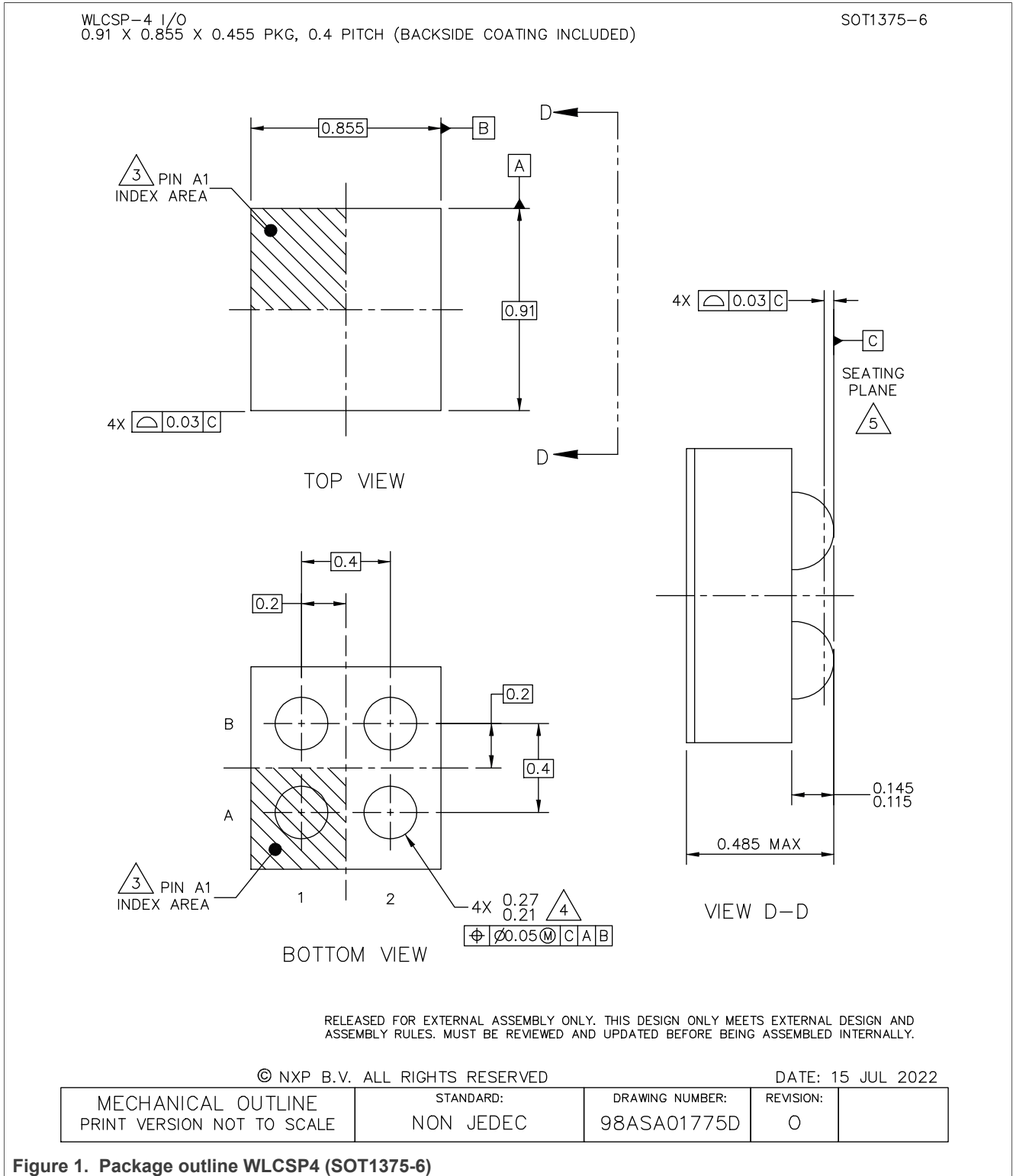
Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	0.91	-	mm
package width	-	0.855	-	mm
seated height	-	0.455	0.485	mm
nominal pitch	-	0.4	-	mm



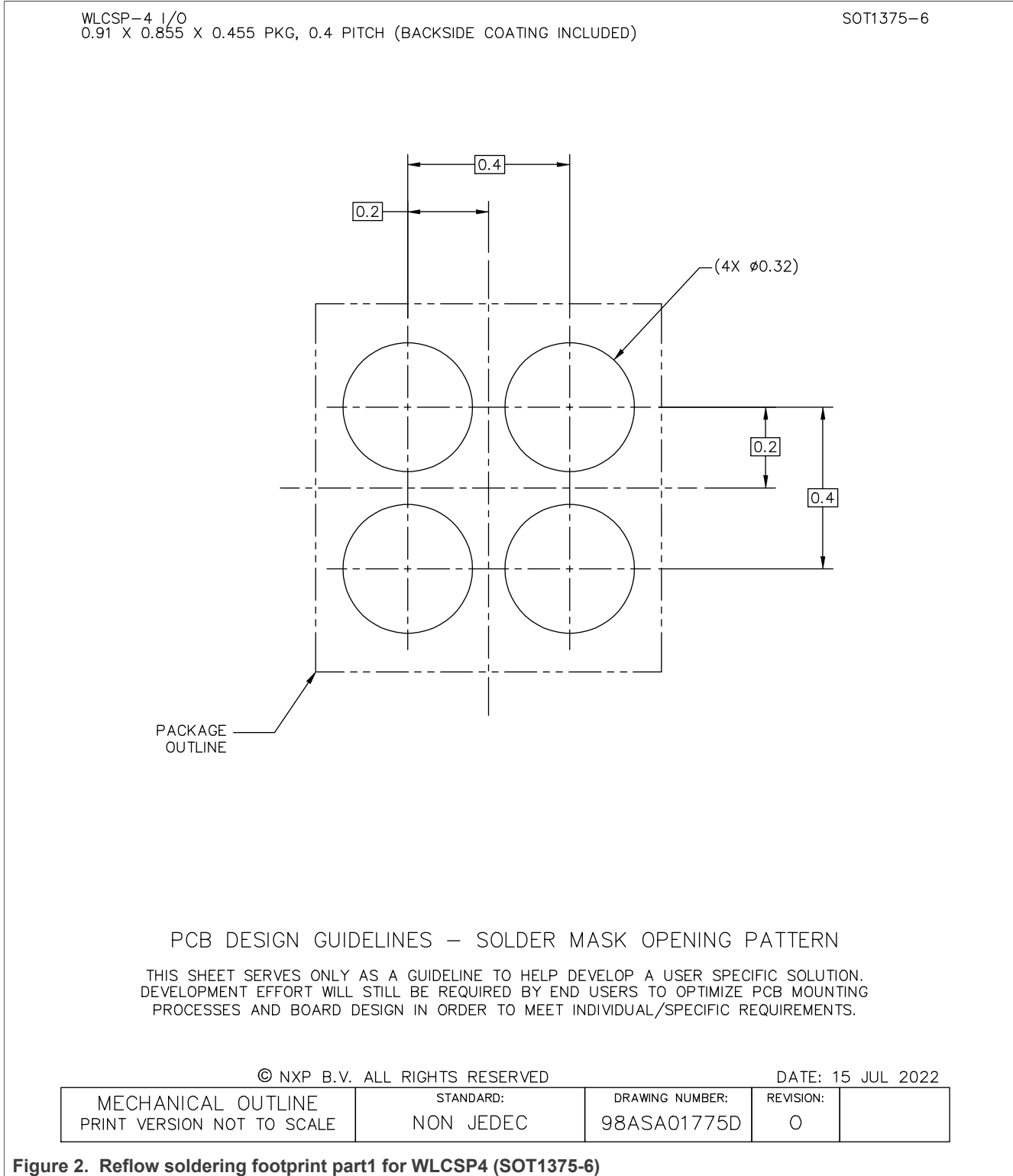
WLCSP4, wafer level chip-scale package, 4 terminals, 0.4 mm pitch, 0.91 mm x 0.855 mm x 0.455 mm body (backside coating included)

2 Package outline



WLCSP4, wafer level chip-scale package, 4 terminals, 0.4 mm pitch, 0.91 mm x 0.855 mm x 0.455 mm body (backside coating included)

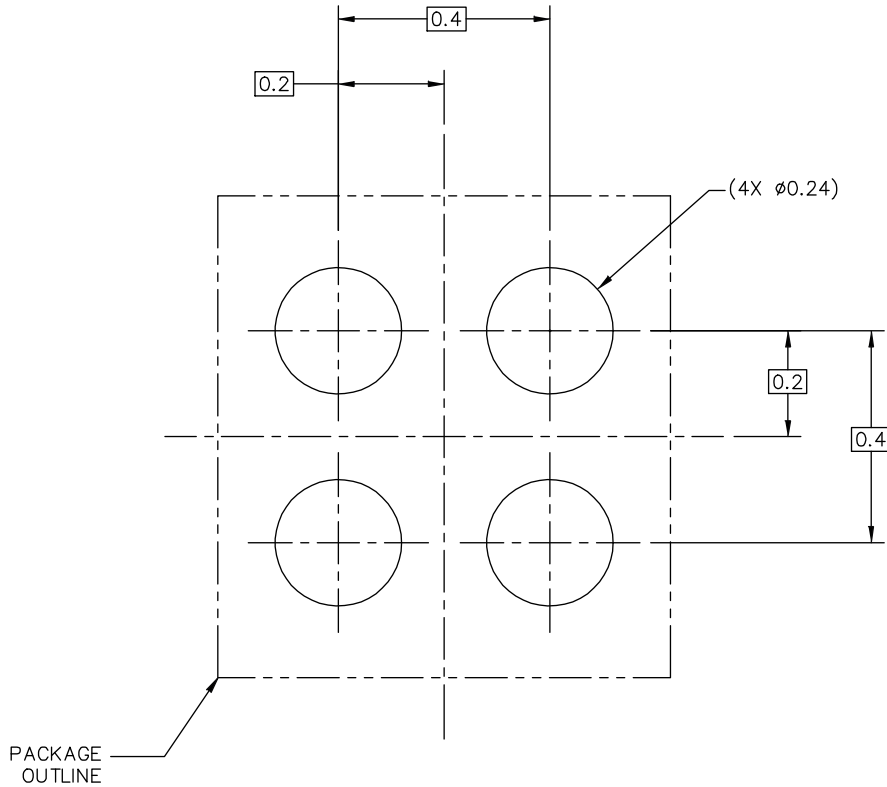
3 Soldering



WLCSP4, wafer level chip-scale package, 4 terminals, 0.4 mm pitch, 0.91 mm x 0.855 mm x 0.455 mm body (backside coating included)

WLCSP-4 I/O  
0.91 X 0.855 X 0.455 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1375-6



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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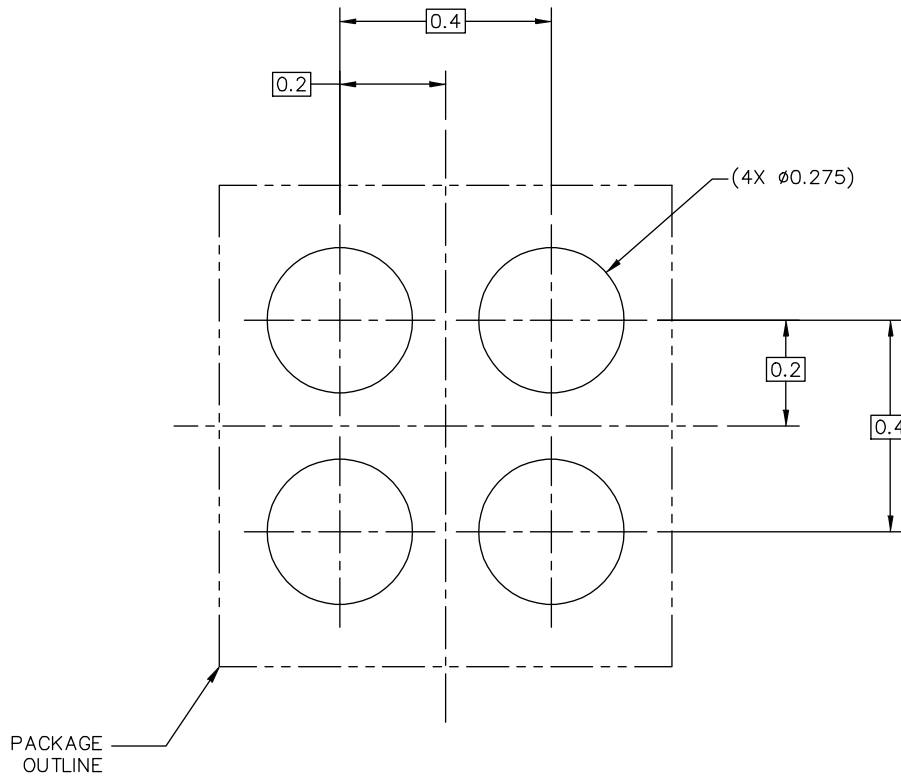
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01775D	REVISION: 0	
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Figure 3. Reflow soldering footprint part2 for WLCSP4 (SOT1375-6)

WLCSP4, wafer level chip-scale package, 4 terminals, 0.4 mm pitch, 0.91 mm x 0.855 mm x 0.455 mm body (backside coating included)

WLCSP-4 I/O  
0.91 X 0.855 X 0.455 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1375-6



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 4. Reflow soldering footprint part3 for WLCSP4 (SOT1375-6)

WLCSP4, wafer level chip-scale package, 4 terminals, 0.4 mm pitch, 0.91 mm x 0.855 mm x 0.455 mm body (backside coating included)

WLCSP-4 I/O  
0.91 X 0.855 X 0.455 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1375-6

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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Figure 5. Package outline note WLCSP4 (SOT1375-6)

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WLCSP4, wafer level chip-scale package, 4 terminals, 0.4 mm pitch, 0.91 mm x 0.855 mm x 0.455 mm  
body (backside coating included)

## 4 Legal information

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body (backside coating included)

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