

SOT1444-11

WLCSP49, wafer level chip-scale package; 49 bumps; 3.3 mm x 3.3 mm x 0.525 mm body (Backside coating included)

4 February 2019

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP49
Package type industry code	WLCSP49
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	22-08-2018
Manufacturer package code	98ASA01205D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	3.3	-	mm
package width	-	3.3	-	mm
package height	-	0.525	-	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	49	-	



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2 Package outline

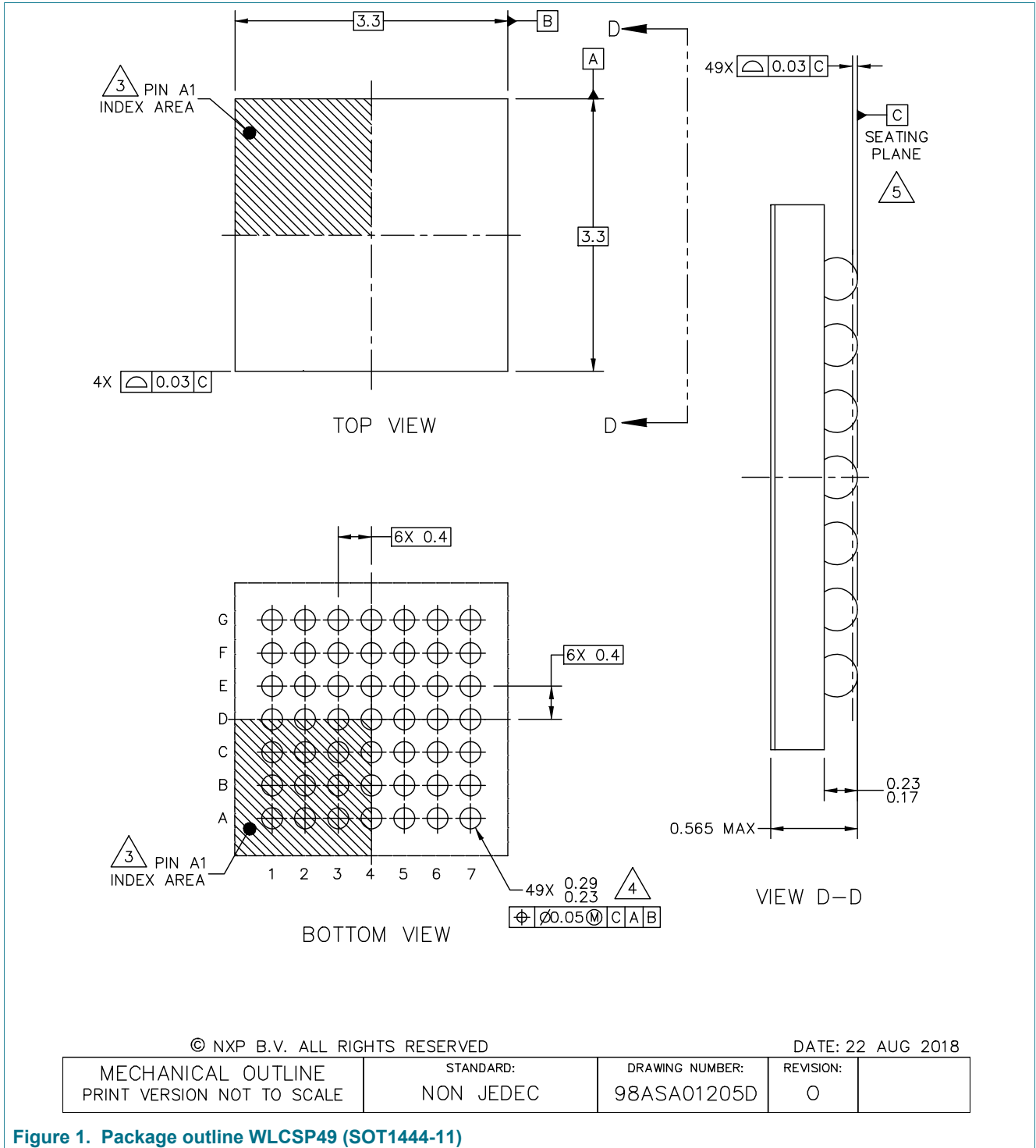


Figure 1. Package outline WLCSP49 (SOT1444-11)

WLCSP49, wafer level chip-scale package; 49 bumps; 3.3 mm x 3.3 mm x 0.525 mm body (Backside coating included)

3 Soldering

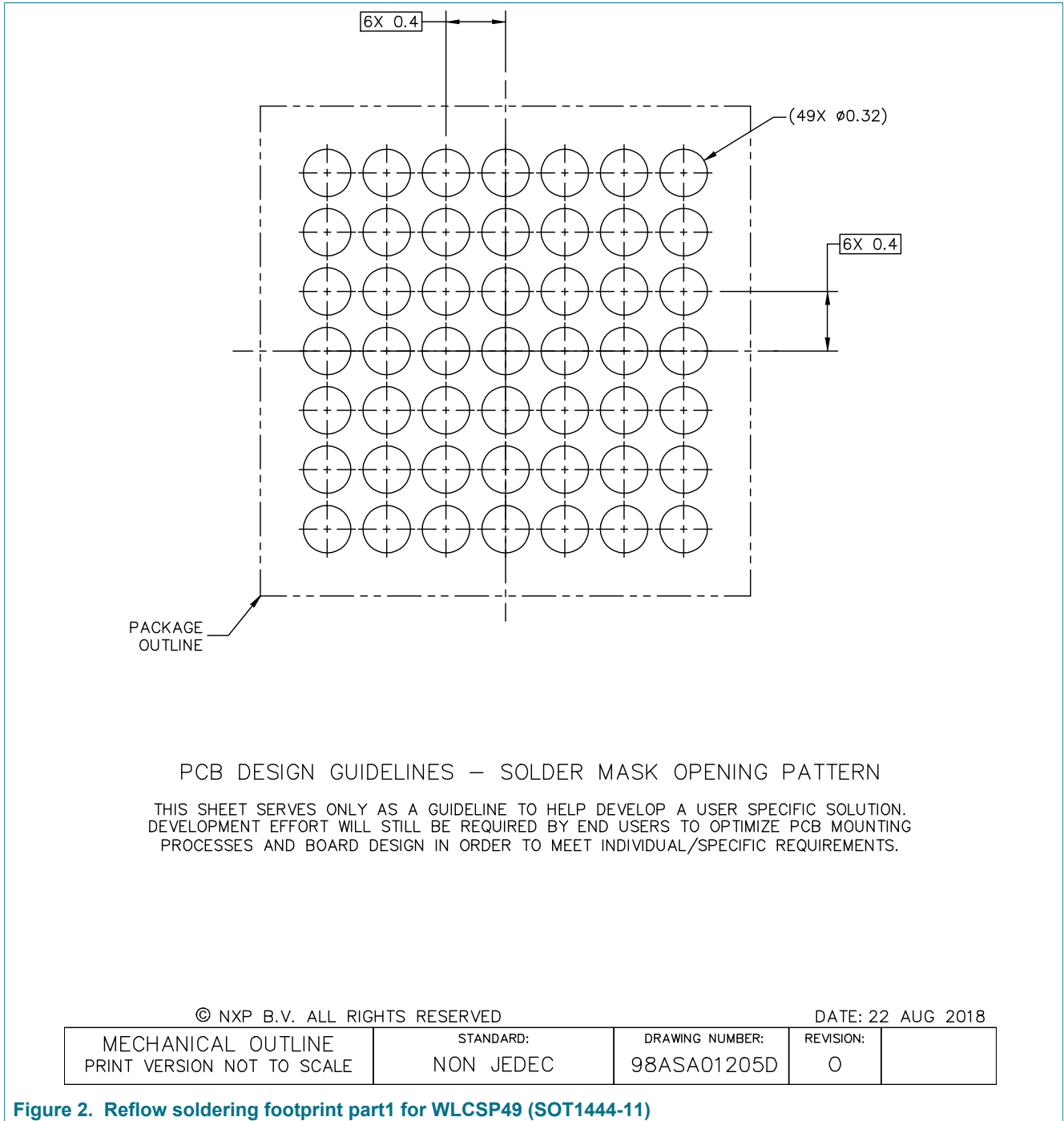
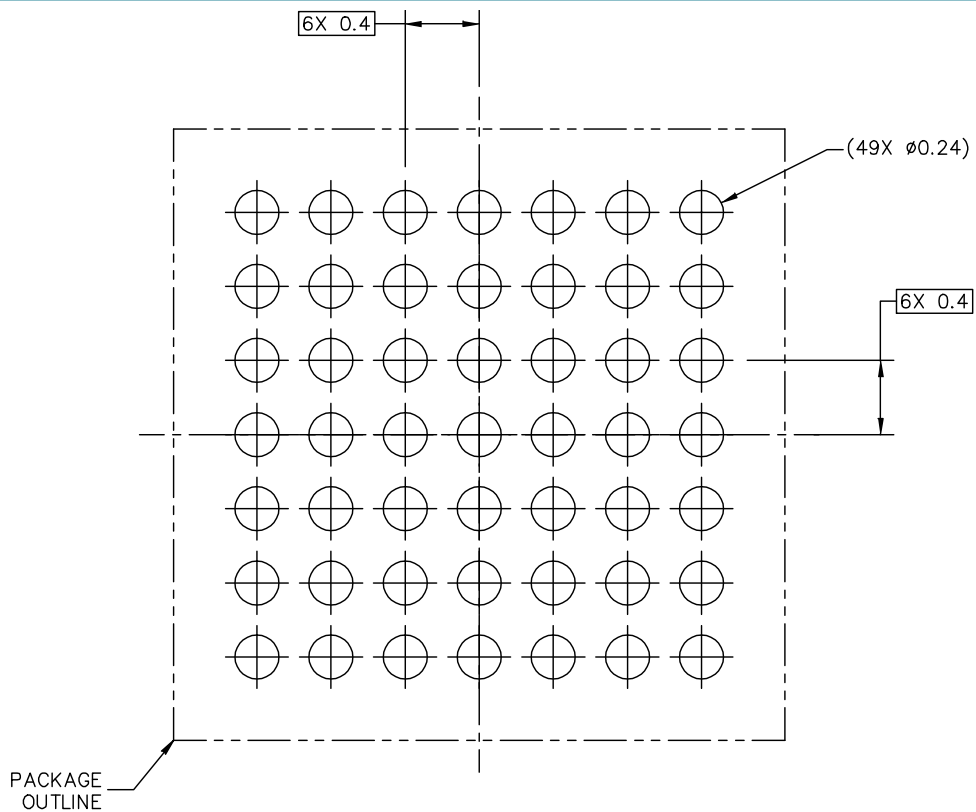


Figure 2. Reflow soldering footprint part1 for WLCSP49 (SOT1444-11)

WLCSP49, wafer level chip-scale package; 49 bumps; 3.3 mm x 3.3 mm x 0.525 mm body (Backside coating included)



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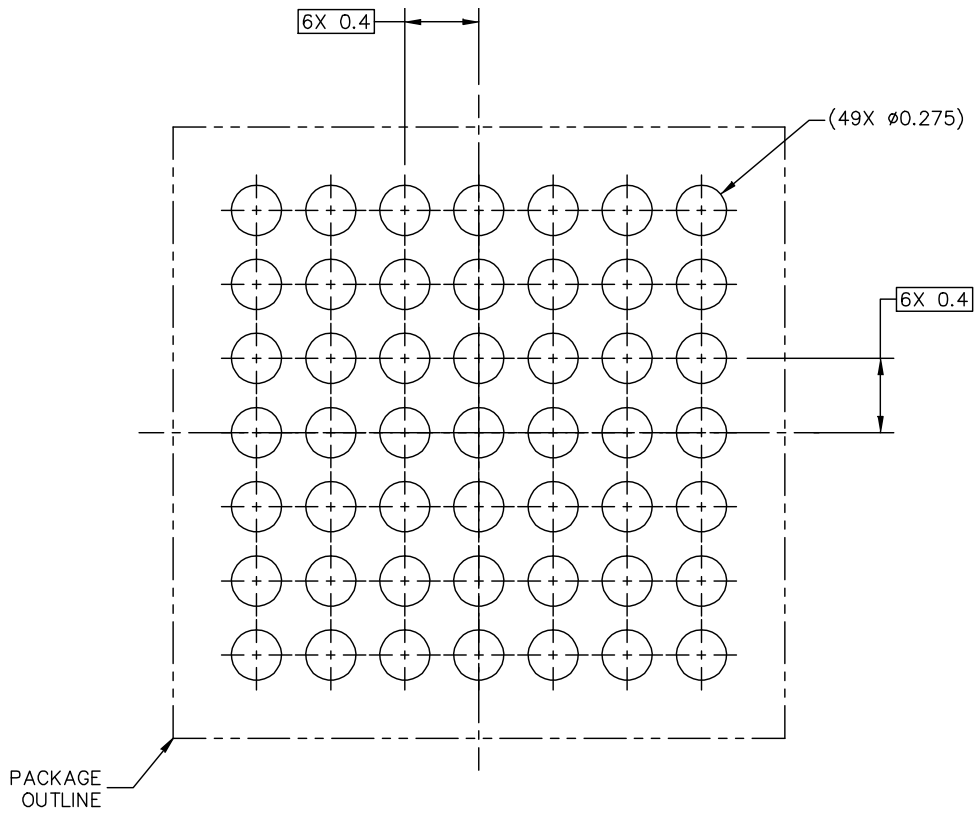
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Figure 3. Reflow soldering footprint part2 for WLCSP49 (SOT1444-11)

WLCSP49, wafer level chip-scale package; 49 bumps; 3.3 mm x 3.3 mm x 0.525 mm body (Backside coating included)



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 4. Reflow soldering footprint part3 for WLCSP49 (SOT1444-11)

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NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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Figure 5. Package outline note WLCSP49 (SOT1444-11)

4 Legal information

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