

SOT1444-13

WLCSP49, wafer level chip-scale package, 49 terminals, 0.4 mm pitch, 3 mm x 2.9 mm x 0.525 mm body (backside coating included)

29 April 2022

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP49
Package style descriptive code	WLCSP (wafer level chip-size package)
Package body material type	S (silicon)
Mounting method type	S (surface mount)
Issue date	23-12-2021
Manufacturer package code	98ASA01877D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	3	-	mm
package width	-	2.9	-	mm
seated height	-	0.525	0.565	mm



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2 Package outline

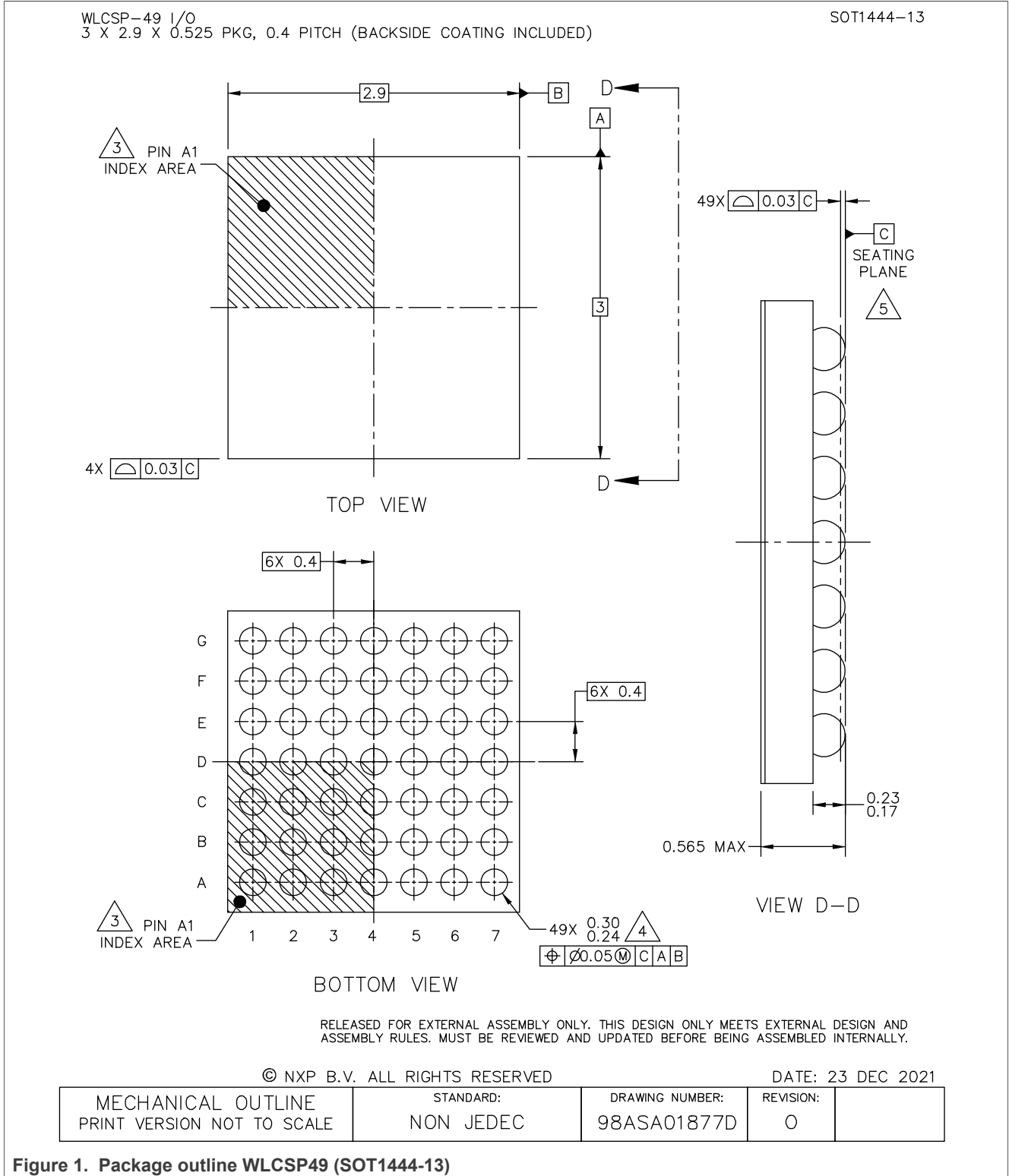


Figure 1. Package outline WLCSP49 (SOT1444-13)

WLCSP49, wafer level chip-scale package, 49 terminals, 0.4 mm pitch, 3 mm x 2.9 mm x 0.525 mm body (backside coating included)

3 Soldering

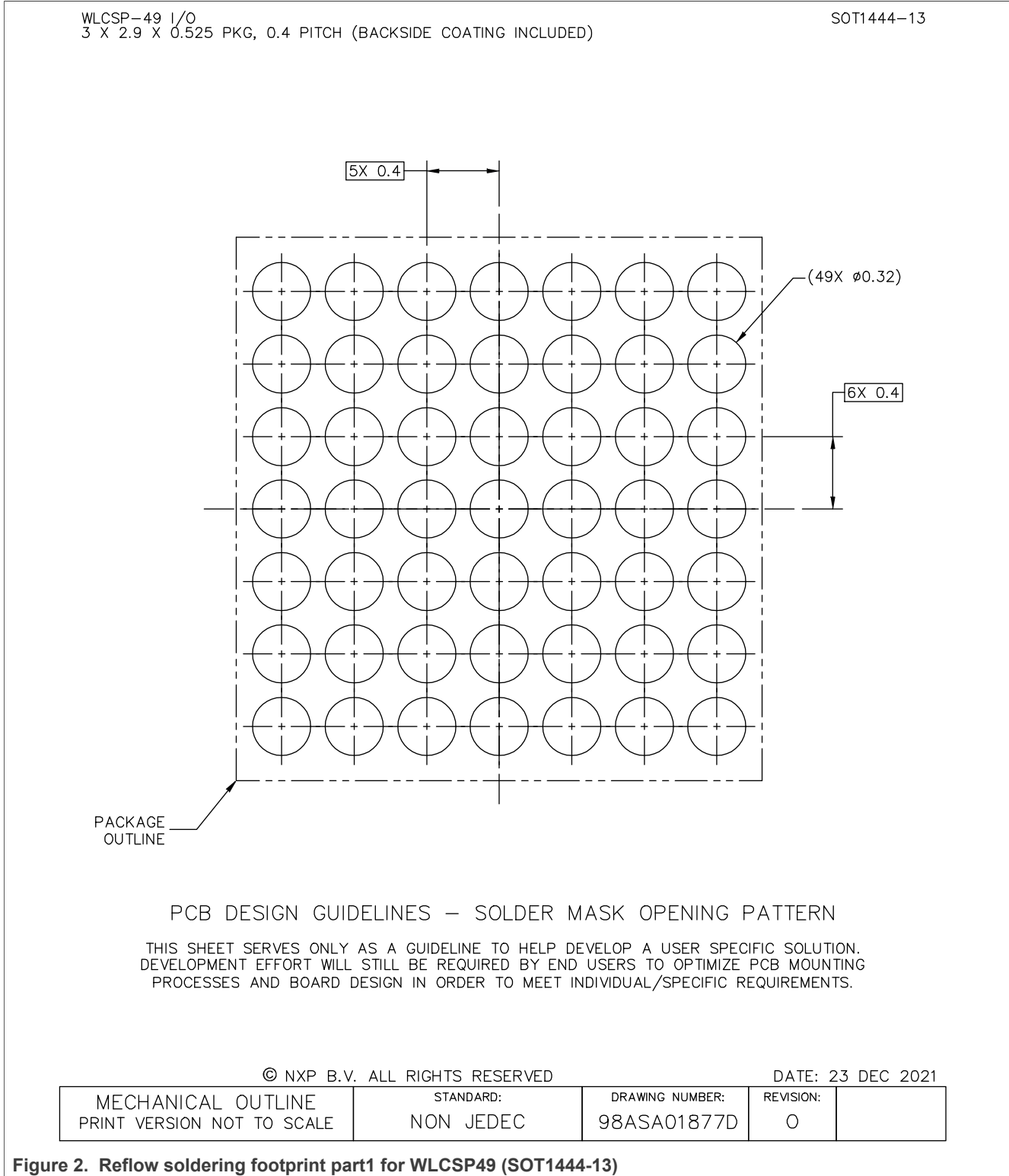
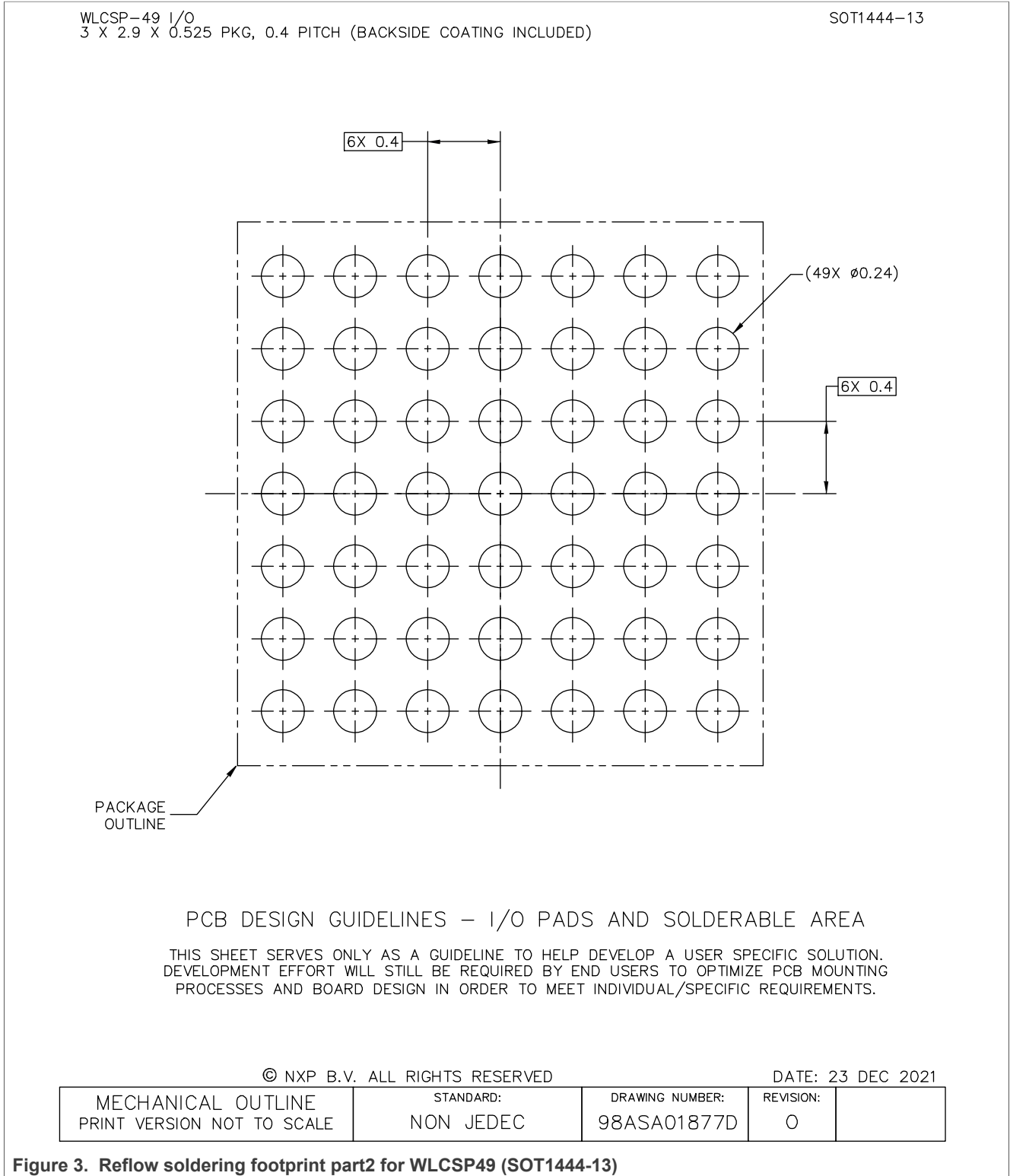


Figure 2. Reflow soldering footprint part1 for WLCSP49 (SOT1444-13)

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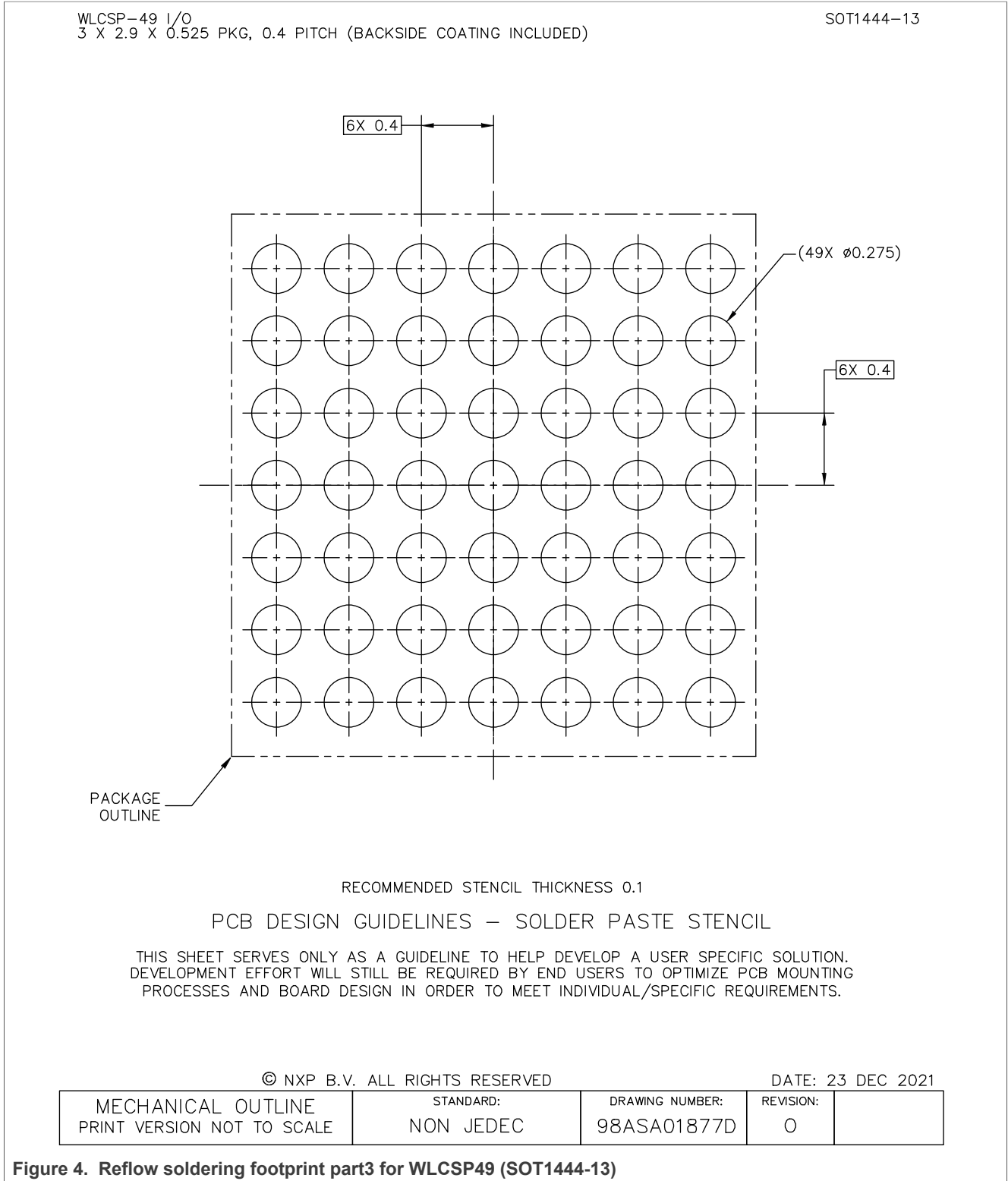


Figure 4. Reflow soldering footprint part3 for WLCSP49 (SOT1444-13)

WLCSP49, wafer level chip-scale package, 49 terminals, 0.4 mm pitch, 3 mm x 2.9 mm x 0.525 mm body (backside coating included)

WLCSP-49 I/O
3 X 2.9 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1444-13

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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DATE: 23 DEC 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01877D	REVISION: 0	
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Figure 5. Package outline note WLCSP49 (SOT1444-13)

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4 Legal information

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