

SOT1445-3

WLCSP6, wafer level chip scale package, 6 terminals, 0.25 mm pitch, 0.7 mm x 0.45 mm x 0.23 mm body

6 September 2018

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP6
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	23-08-2018
Manufacturer package code	98ASA01188D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	0.7	-	mm
package width	-	0.45	-	mm
seated height	-	0.23	-	mm
nominal pitch	-	0.25	-	mm
actual quantity of termination	-	6	-	



2 Package outline

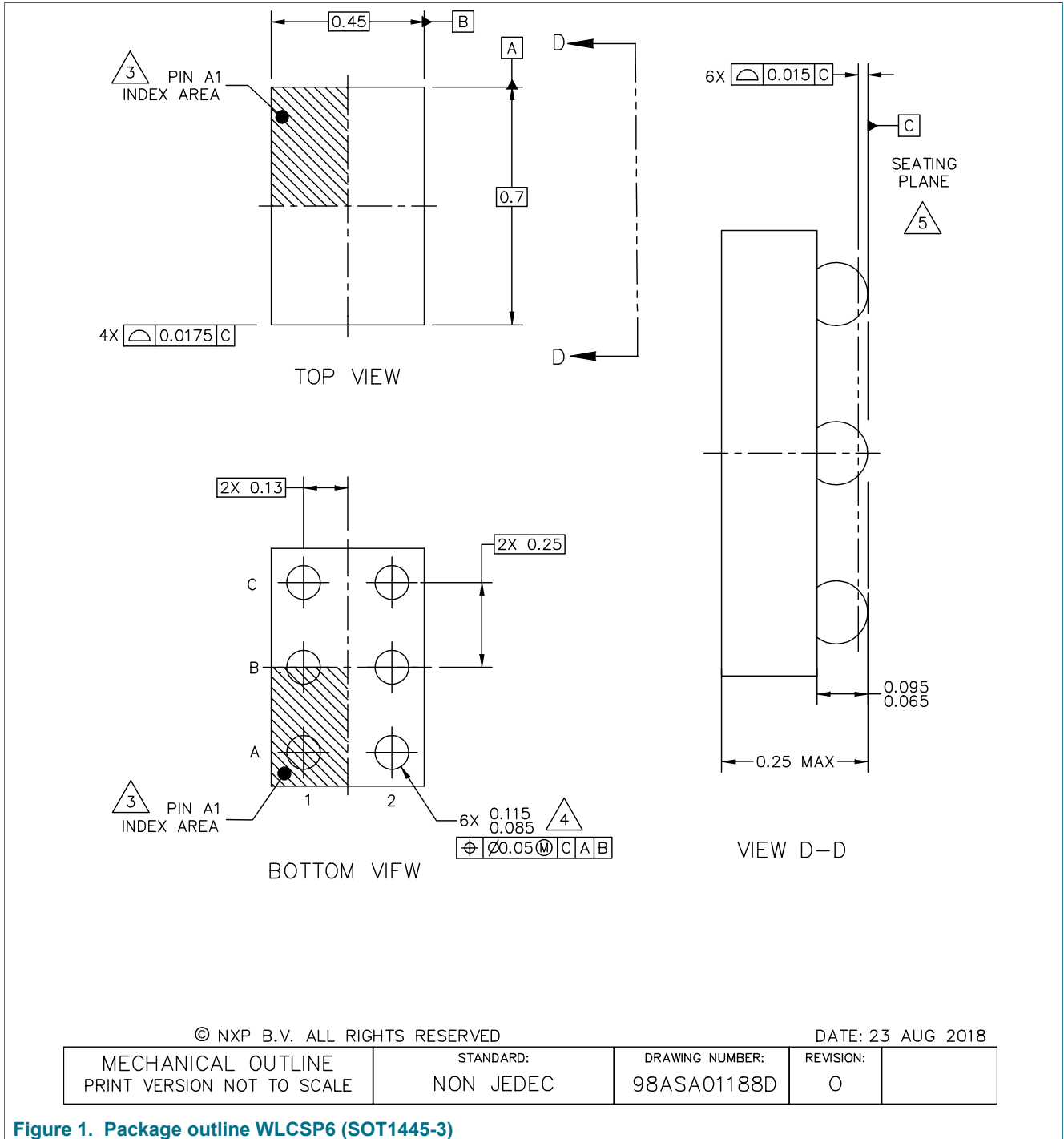


Figure 1. Package outline WLCSP6 (SOT1445-3)

3 Soldering

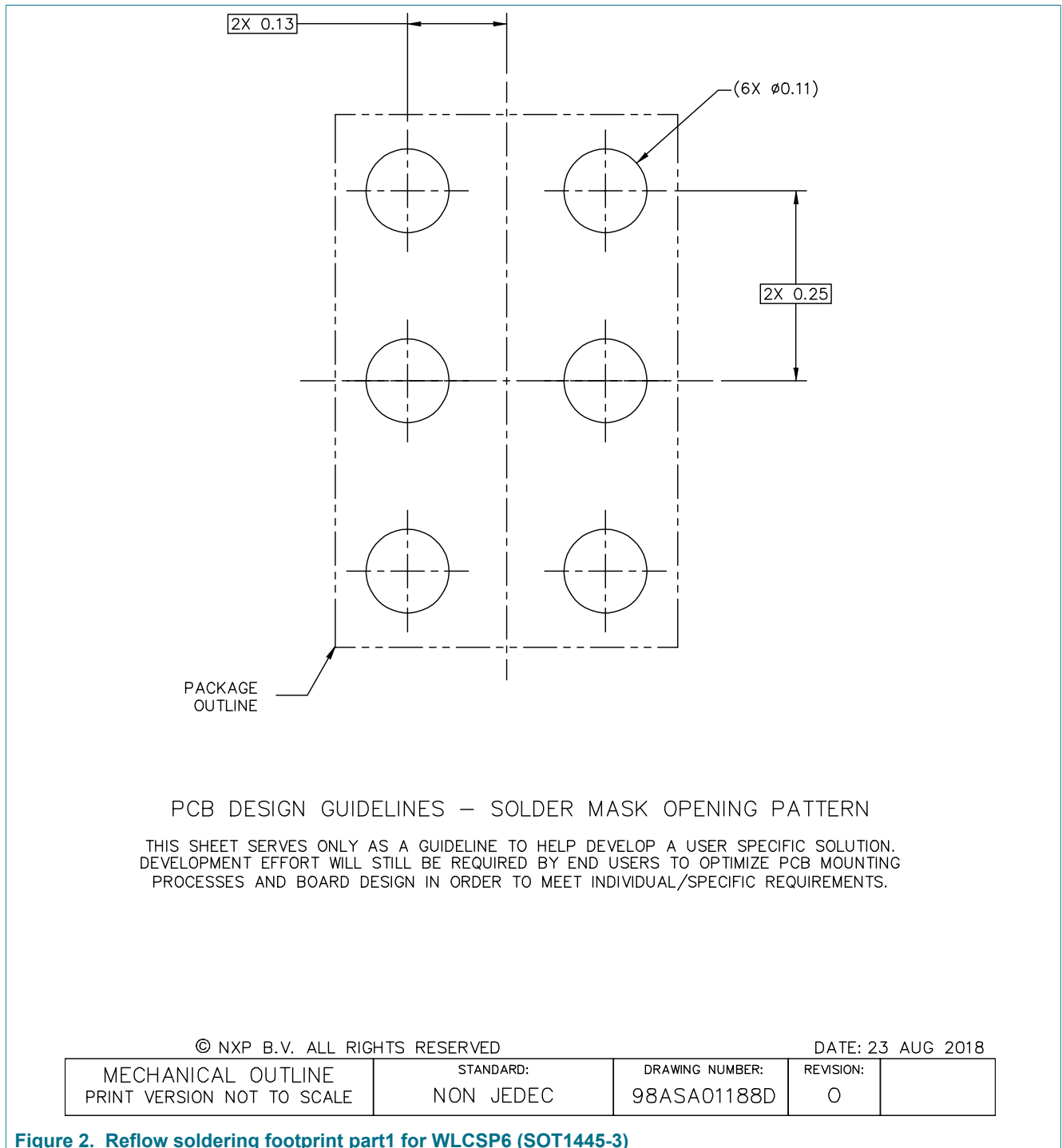
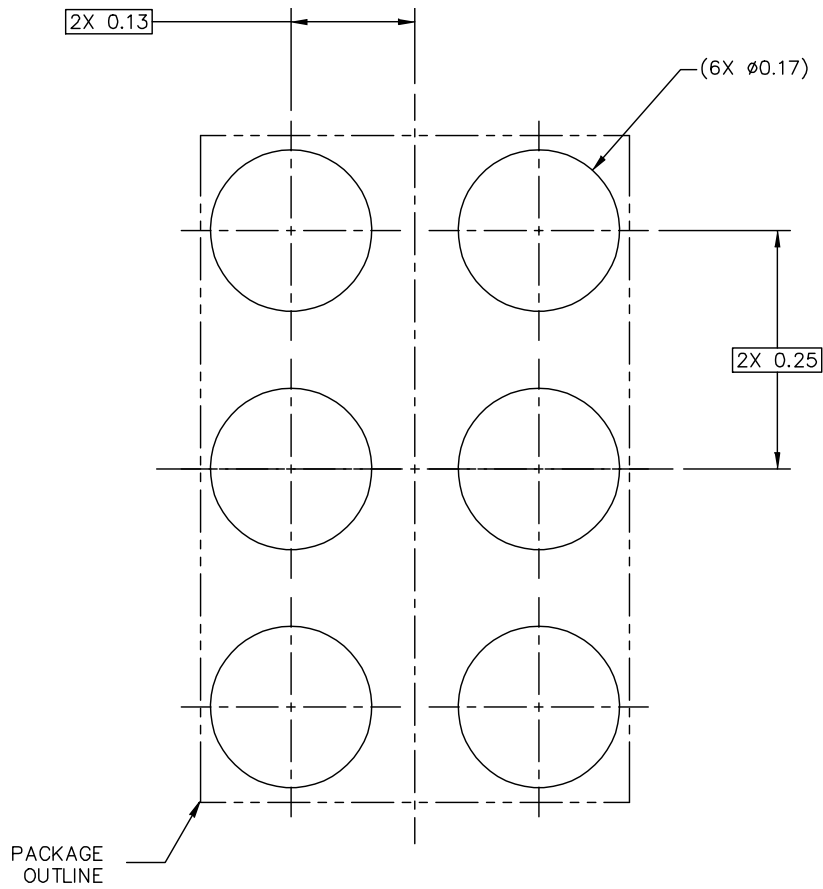


Figure 2. Reflow soldering footprint part1 for WLCSP6 (SOT1445-3)



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

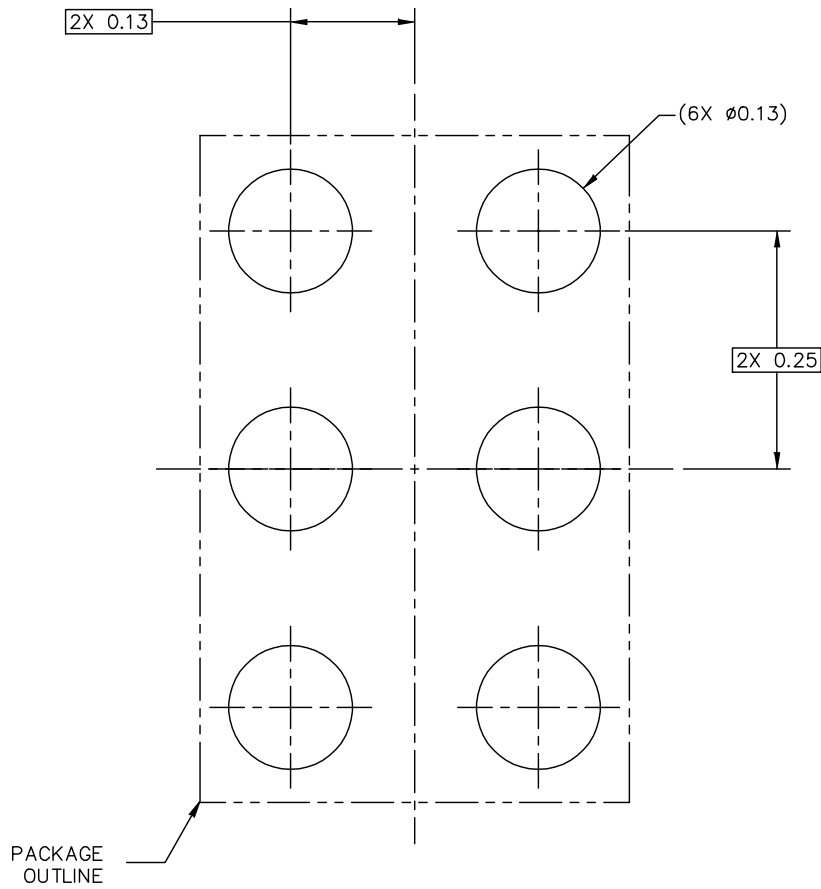
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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01188D	REVISION: 0	
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Figure 3. Reflow soldering footprint part2 for WLCSP6 (SOT1445-3)



RECOMMENDED STENCIL THICKNESS 0.06

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 4. Reflow soldering footprint part3 for WLCSP6 (SOT1445-3)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

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Figure 5. Package outline note WLCSP6 (SOT1445-3)

4 Legal information

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