



SOT1459-7

WLCSP42, wafer level chip scale package, 42 terminals, 0.4 mm pitch, 2.86 mm x 2.46 mm x 0.525 mm body (backside coating included)

25 May 2020

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP42
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	13-05-2020
Manufacturer package code	98ASA01565D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	2.83	2.86	2.89	mm
package width	2.43	2.46	2.49	mm
package height	-	0.525	0.565	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	42	-	



WLCSP42, wafer level chip scale package, 42 terminals, 0.4 mm pitch, 2.86 mm x 2.46 mm x 0.525 mm body (backside coating included)

2 Package outline

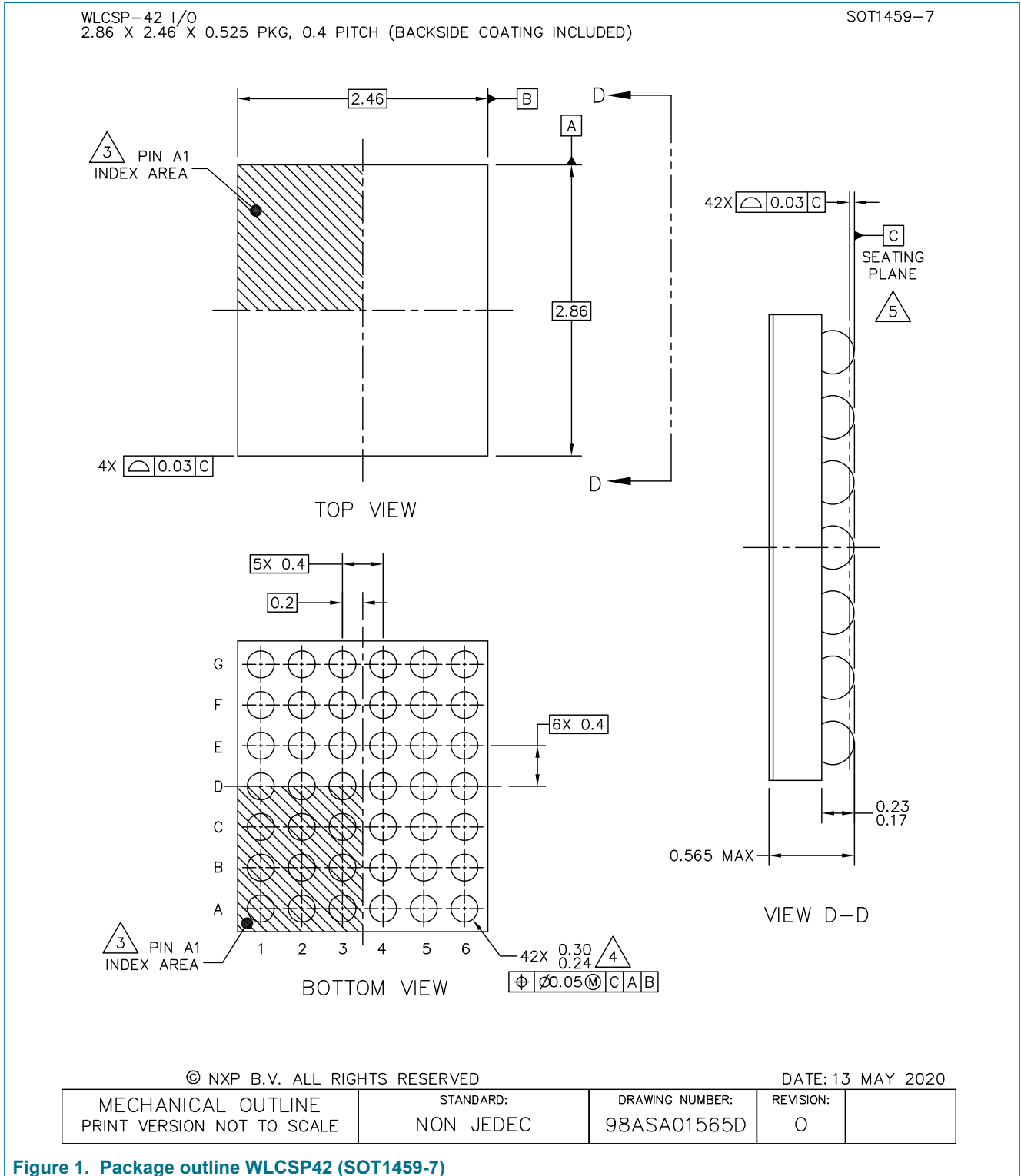


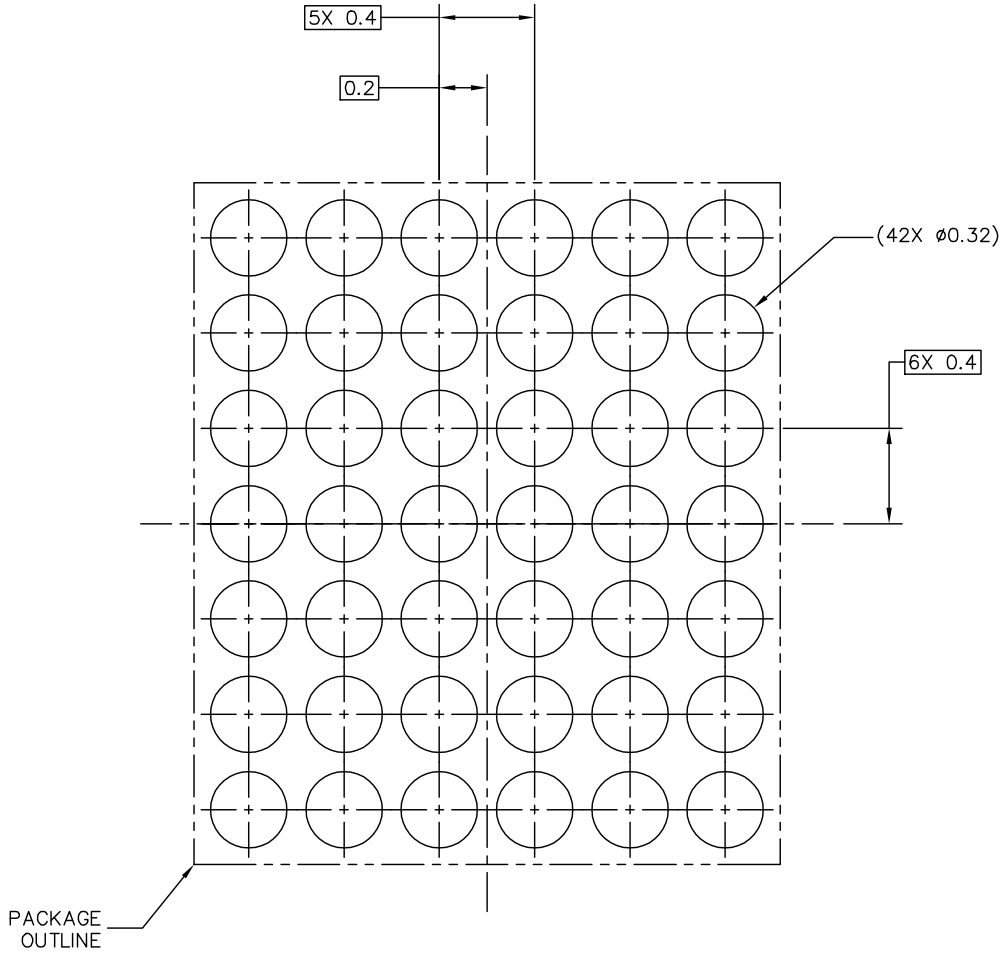
Figure 1. Package outline WLCSP42 (SOT1459-7)

WLCSP42, wafer level chip scale package, 42 terminals, 0.4 mm pitch, 2.86 mm x 2.46 mm x 0.525 mm body (backside coating included)

3 Soldering

WLCSP-42 I/O
2.86 X 2.46 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1459-7



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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DATE: 13 MAY 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01565D	REVISION: 0	
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Figure 2. Reflow soldering footprint part1 for WLCSP42 (SOT1459-7)

WLCSP42, wafer level chip scale package, 42 terminals, 0.4 mm pitch, 2.86 mm x 2.46 mm x 0.525 mm body (backside coating included)

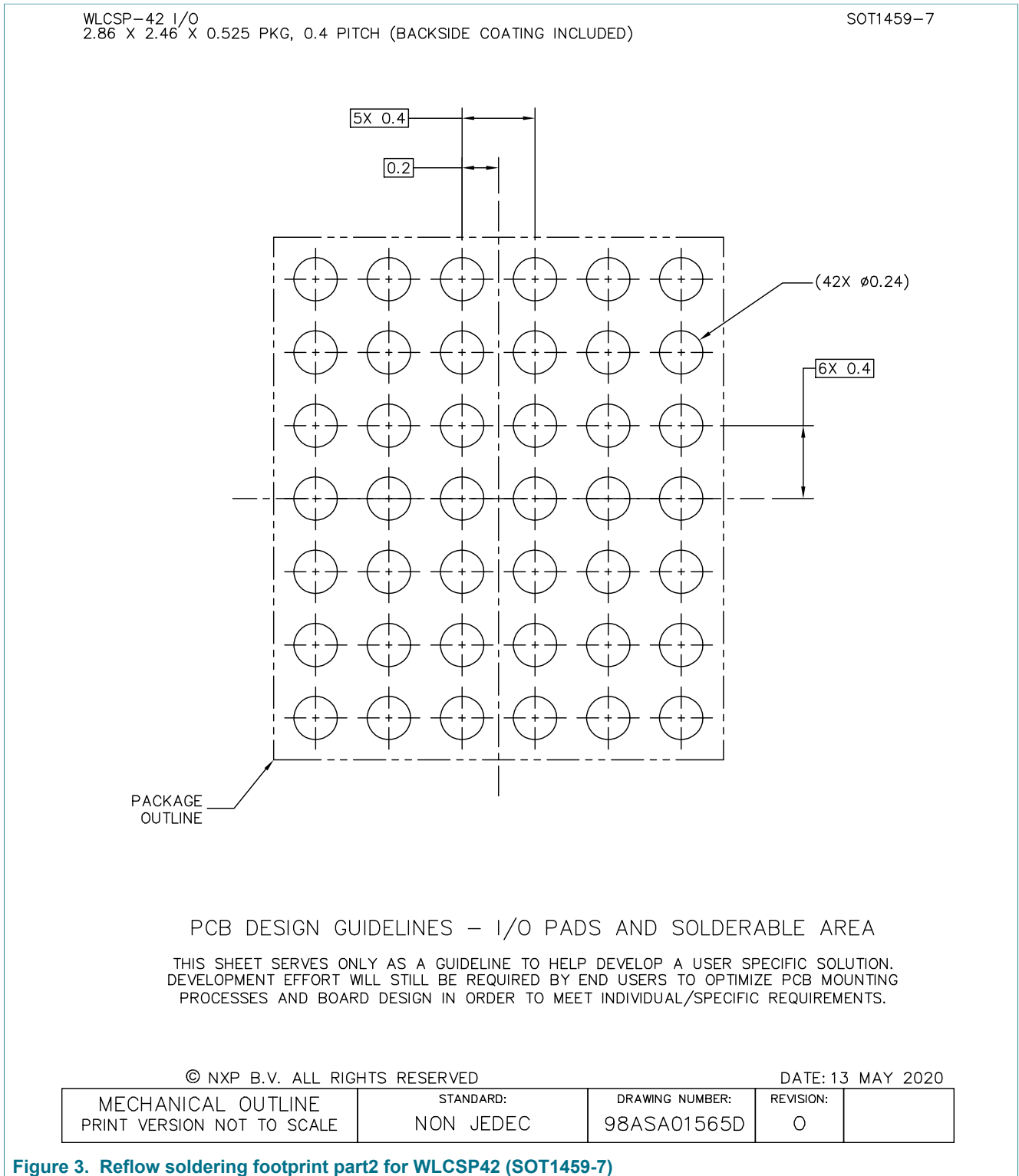


Figure 3. Reflow soldering footprint part2 for WLCSP42 (SOT1459-7)

WLCSP42, wafer level chip scale package, 42 terminals, 0.4 mm pitch, 2.86 mm x 2.46 mm x 0.525 mm body (backside coating included)

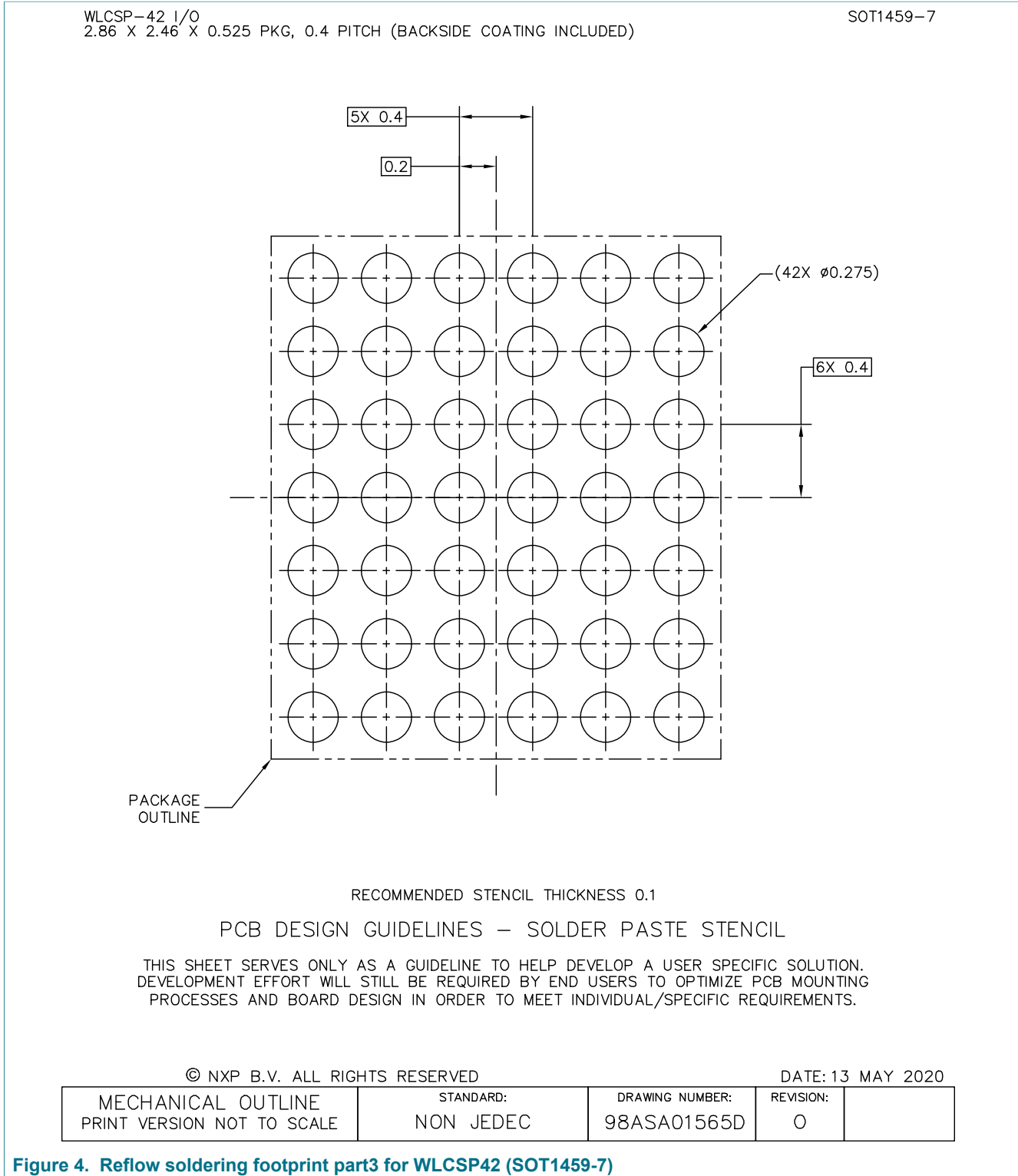


Figure 4. Reflow soldering footprint part3 for WLCSP42 (SOT1459-7)

WLCSP42, wafer level chip scale package, 42 terminals, 0.4 mm pitch, 2.86 mm x 2.46 mm x 0.525 mm body (backside coating included)

WLCSP-42 I/O
2.86 X 2.46 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1459-7

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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Figure 5. Package outline note WLCSP42 (SOT1459-7)

4 Legal information

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