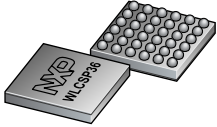


SOT1780-14

WLCSP36, wafer level chip-size package, 36 terminals, 0.4 mm pitch, 2.46 mm x 2.46 mm x 0.525 mm body

11 May 2026

Package information



1 Package summary

Terminal position code	Q (quad)
Package type descriptive code	WLCSP36
Package style descriptive code	WLCSP (wafer level chip-size package)
Package body material type	P (plastic)
Mounting method type	S (surface mount)
Issue date	05-05-2026
Manufacturer package code	98ASA02052D

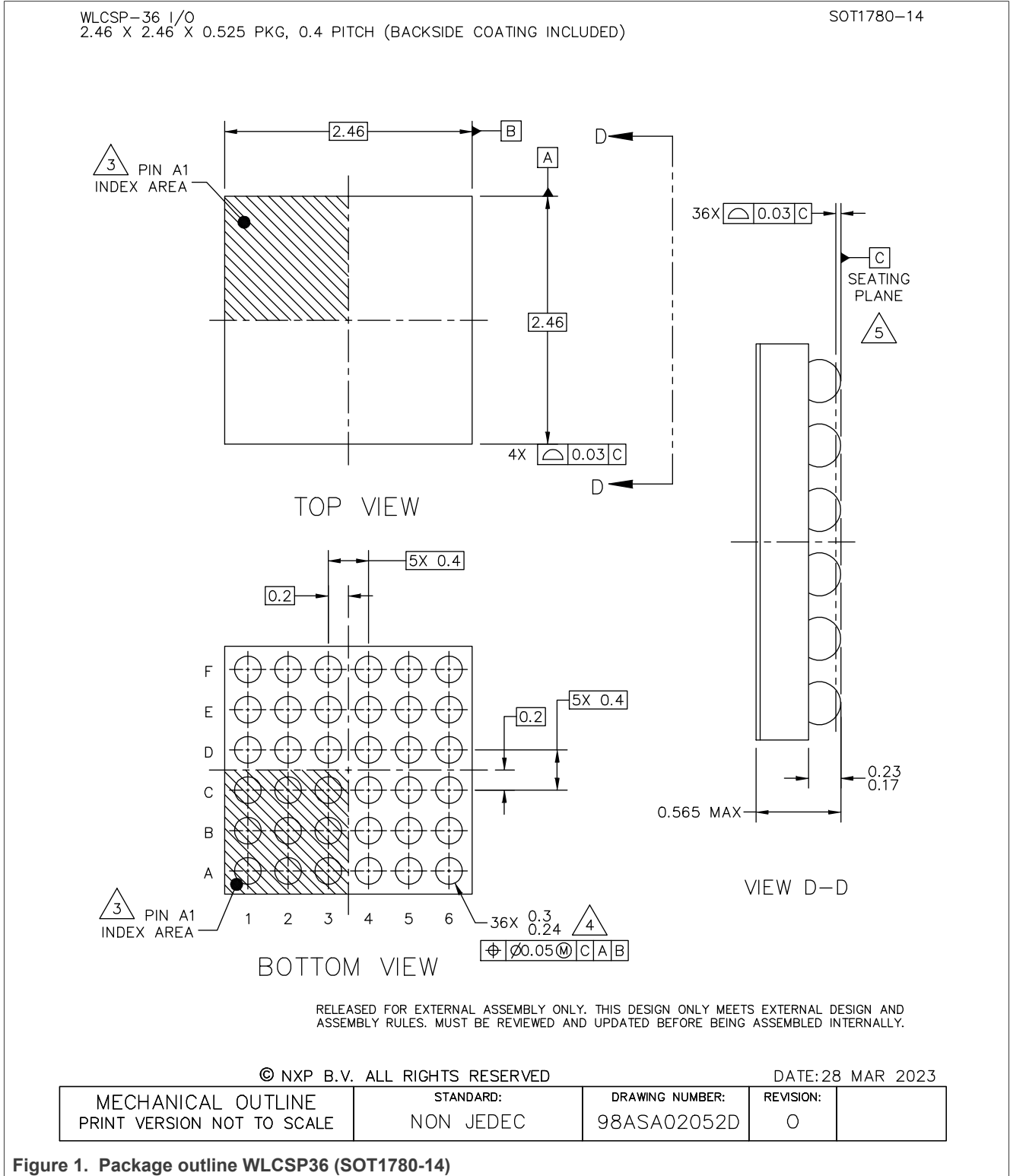
Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	2.43	2.46	2.49	mm
package width	2.43	2.46	2.49	mm
seated height	0.485	0.525	0.565	mm
package height	0.335	0.365	0.395	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	36	-	



WLCSP36, wafer level chip-size package, 36 terminals, 0.4 mm pitch, 2.46 mm x 2.46 mm x 0.525 mm body

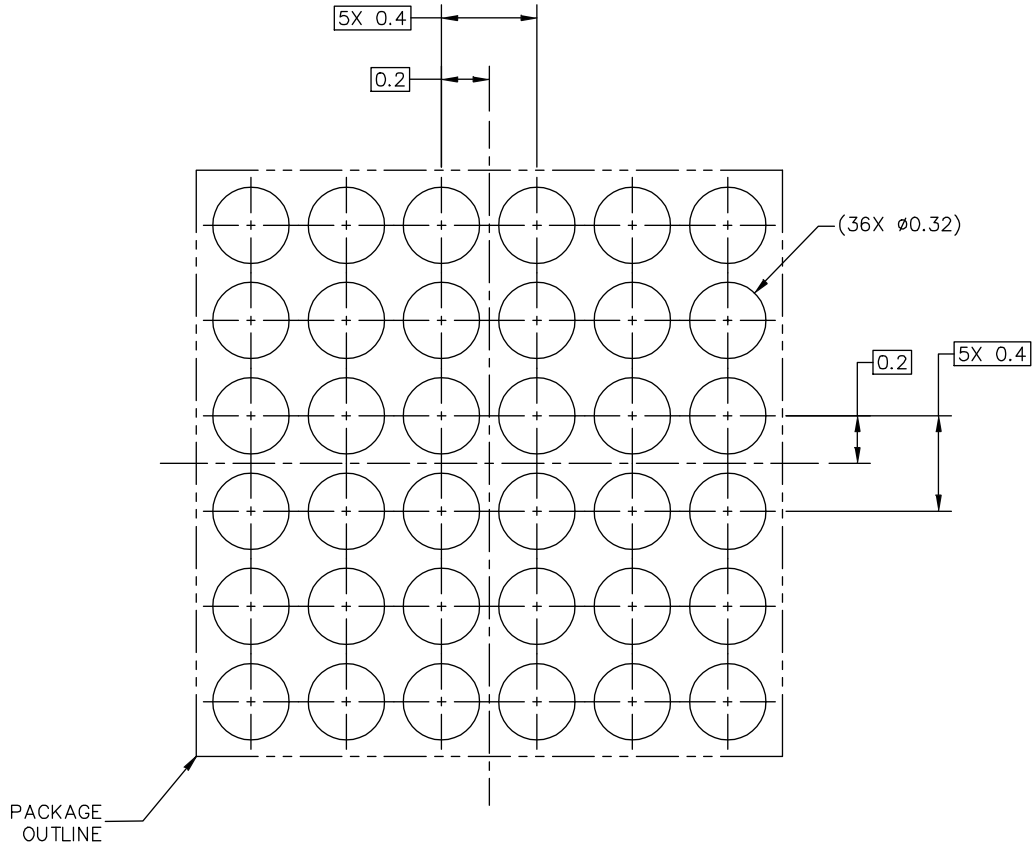
2 Package outline



3 Soldering

WLCSP-36 I/O
2.46 X 2.46 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1780-14



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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DATE: 28 MAR 2023

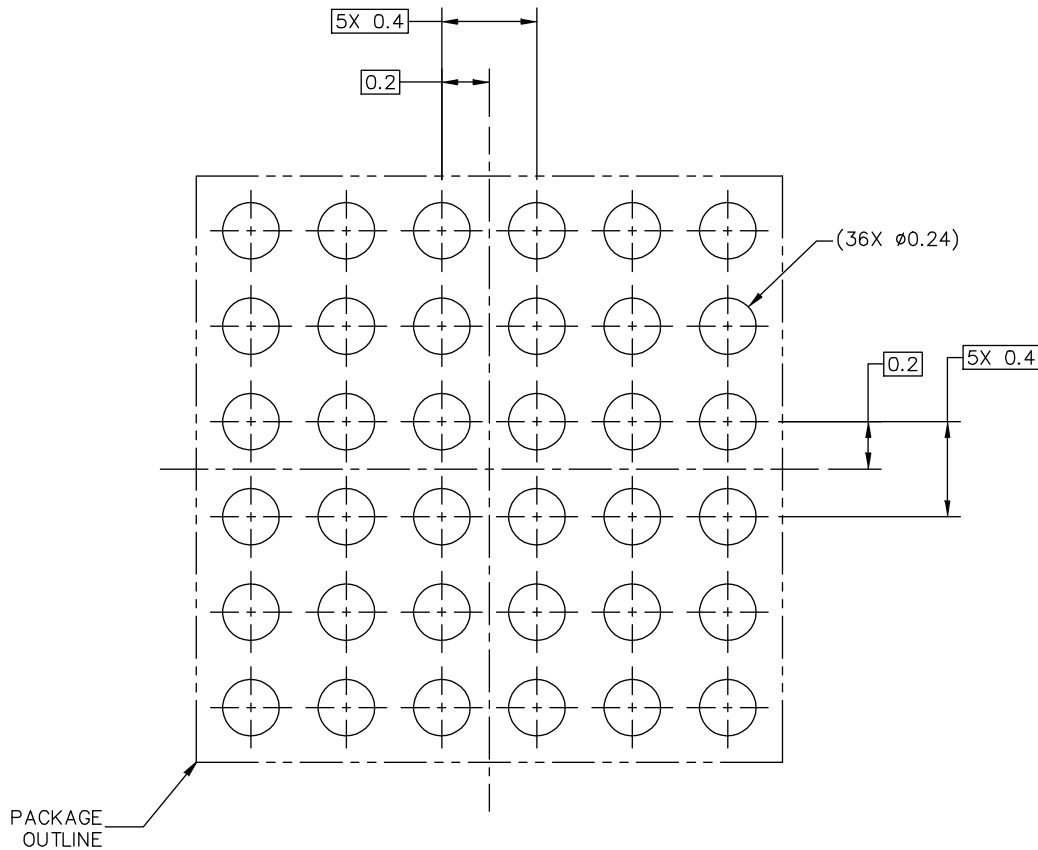
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02052D	REVISION: 0	
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Figure 2. Reflow soldering footprint part1 for WLCSP36 (SOT1780-14)

WLCSP36, wafer level chip-size package, 36 terminals, 0.4 mm pitch, 2.46 mm x 2.46 mm x 0.525 mm body

WLCSP-36 I/O
2.46 X 2.46 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1780-14



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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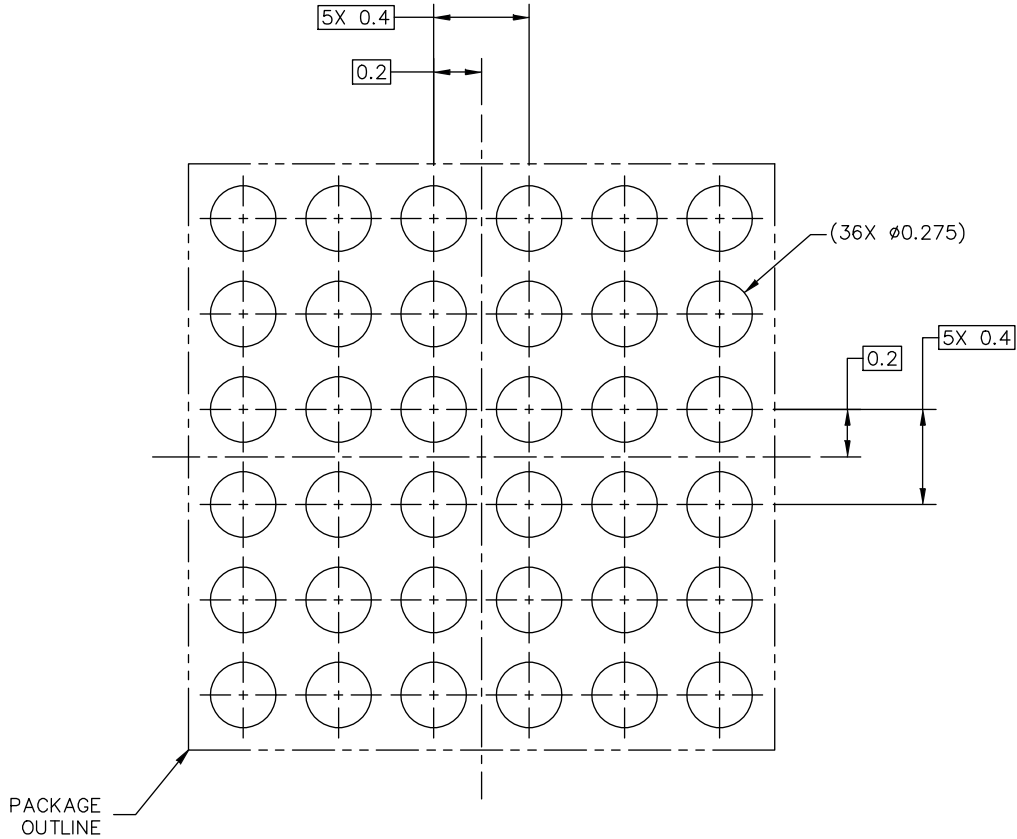
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02052D	REVISION: 0	
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Figure 3. Reflow soldering footprint part2 for WLCSP36 (SOT1780-14)

WLCSP36, wafer level chip-size package, 36 terminals, 0.4 mm pitch, 2.46 mm x 2.46 mm x 0.525 mm body

WLCSP-36 I/O
2.46 X 2.46 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1780-14



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 4. Reflow soldering footprint part3 for WLCSP36 (SOT1780-14)

WLCSP36, wafer level chip-size package, 36 terminals, 0.4 mm pitch, 2.46 mm x 2.46 mm x 0.525 mm body

WLCSP-36 I/O
2.46 X 2.46 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1780-14

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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DATE: 28 MAR 2023

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Figure 5. Package outline note WLCSP36 (SOT1780-14)

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