



# SOT1780-4

WLCSP36, wafer level chip-scale package; 36 bumps; 0.4 mm pitch, 2.62 mm x 2.51 mm x 0.525 mm body (backside coating included)

22 March 2020

Package information

## 1 Package summary

<b>Terminal position code</b>	B (bottom)
<b>Package type descriptive code</b>	WLCSP36
<b>Package style descriptive code</b>	WLCSP (wafer level chip-size package)
<b>Mounting method type</b>	S (surface mount)
<b>Issue date</b>	20-12-2017
<b>Manufacturer package code</b>	98ASA01158D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	2.59	2.62	2.65	mm
package width	2.48	2.51	2.54	mm
seated height	-	0.525	0.565	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	36	-	



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2 Package outline

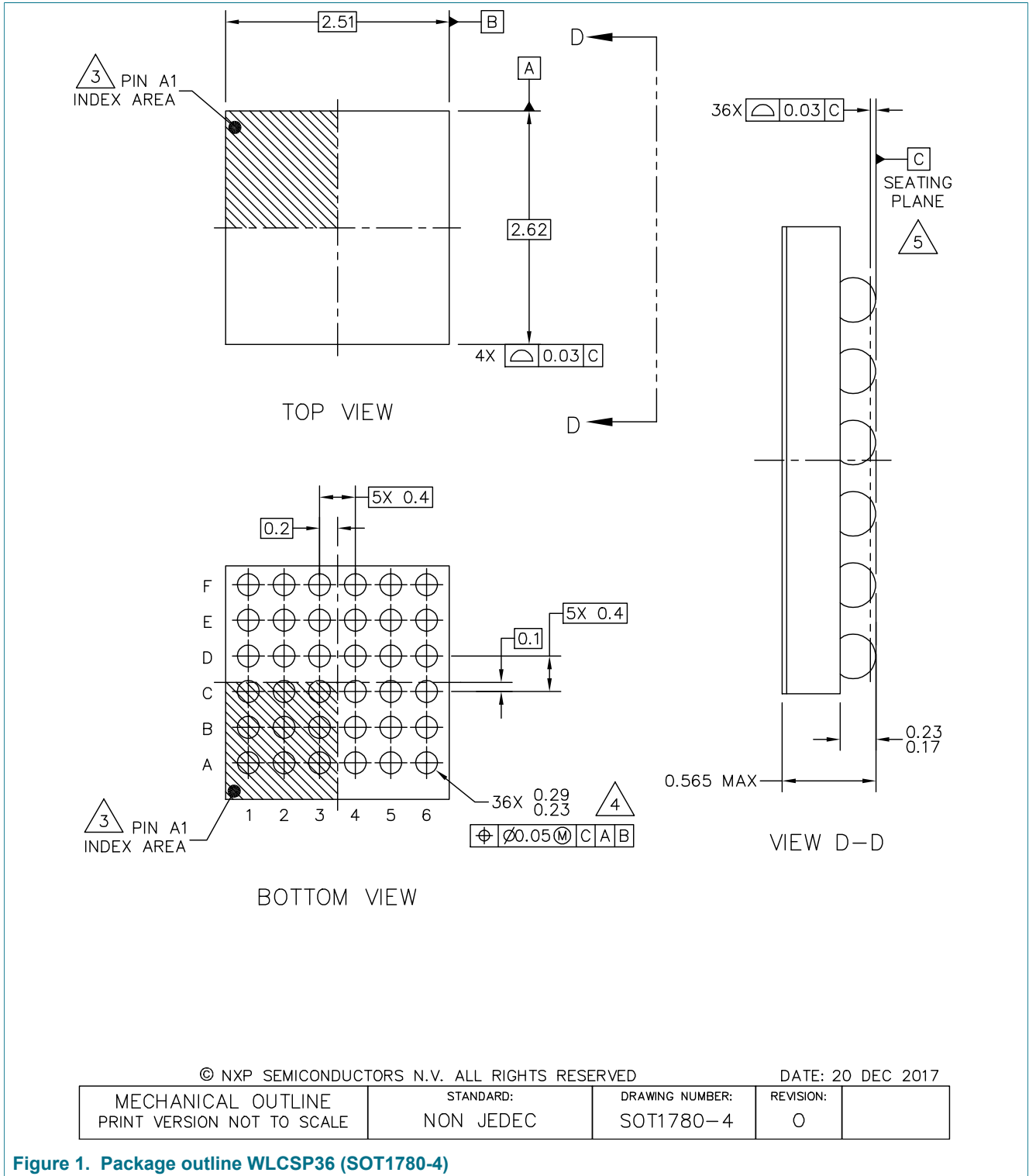


Figure 1. Package outline WLCSP36 (SOT1780-4)

WLCSP36, wafer level chip-scale package; 36 bumps; 0.4 mm pitch, 2.62 mm x 2.51 mm x 0.525 mm body (backside coating included)

3 Soldering

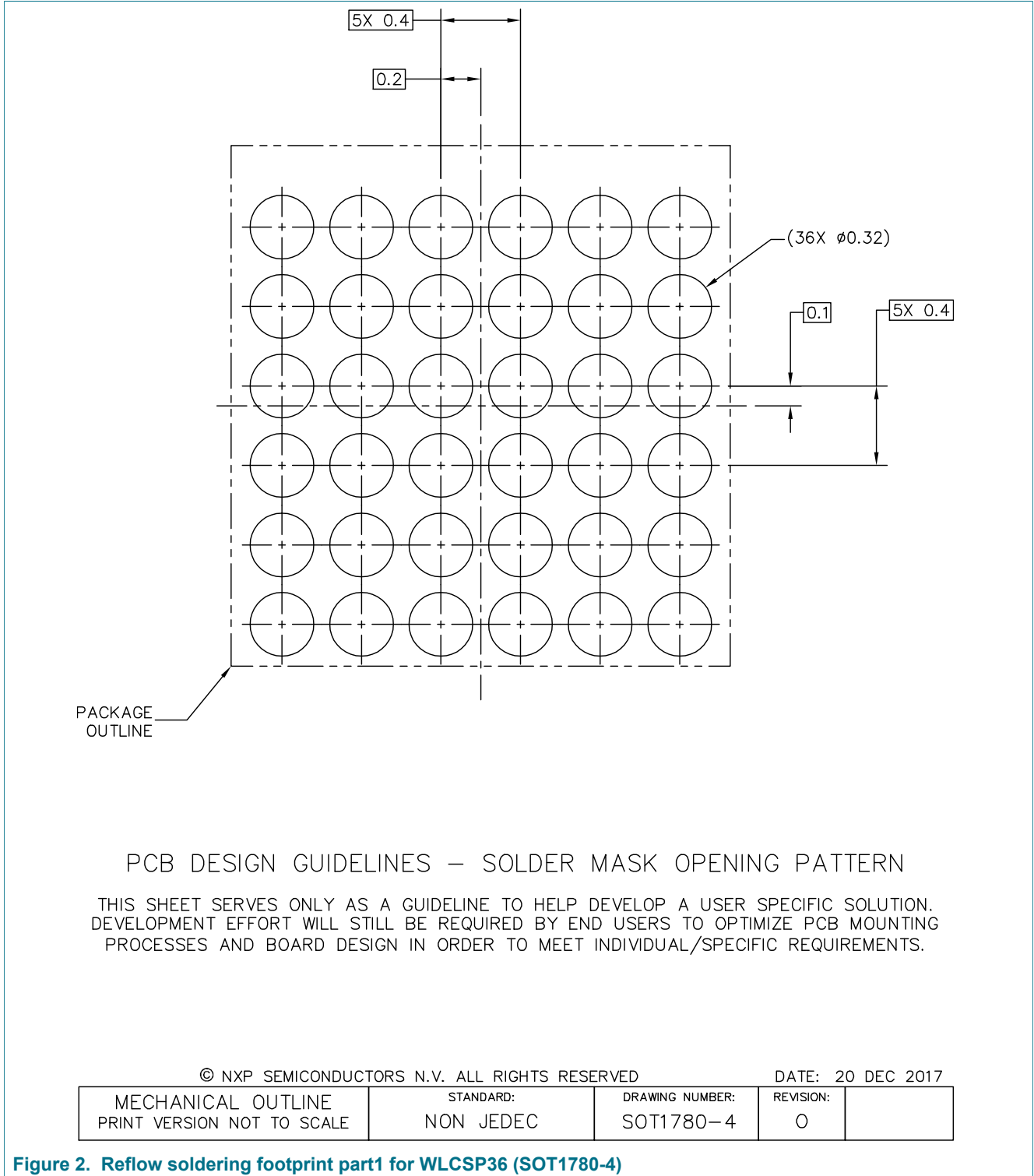


Figure 2. Reflow soldering footprint part1 for WLCSP36 (SOT1780-4)

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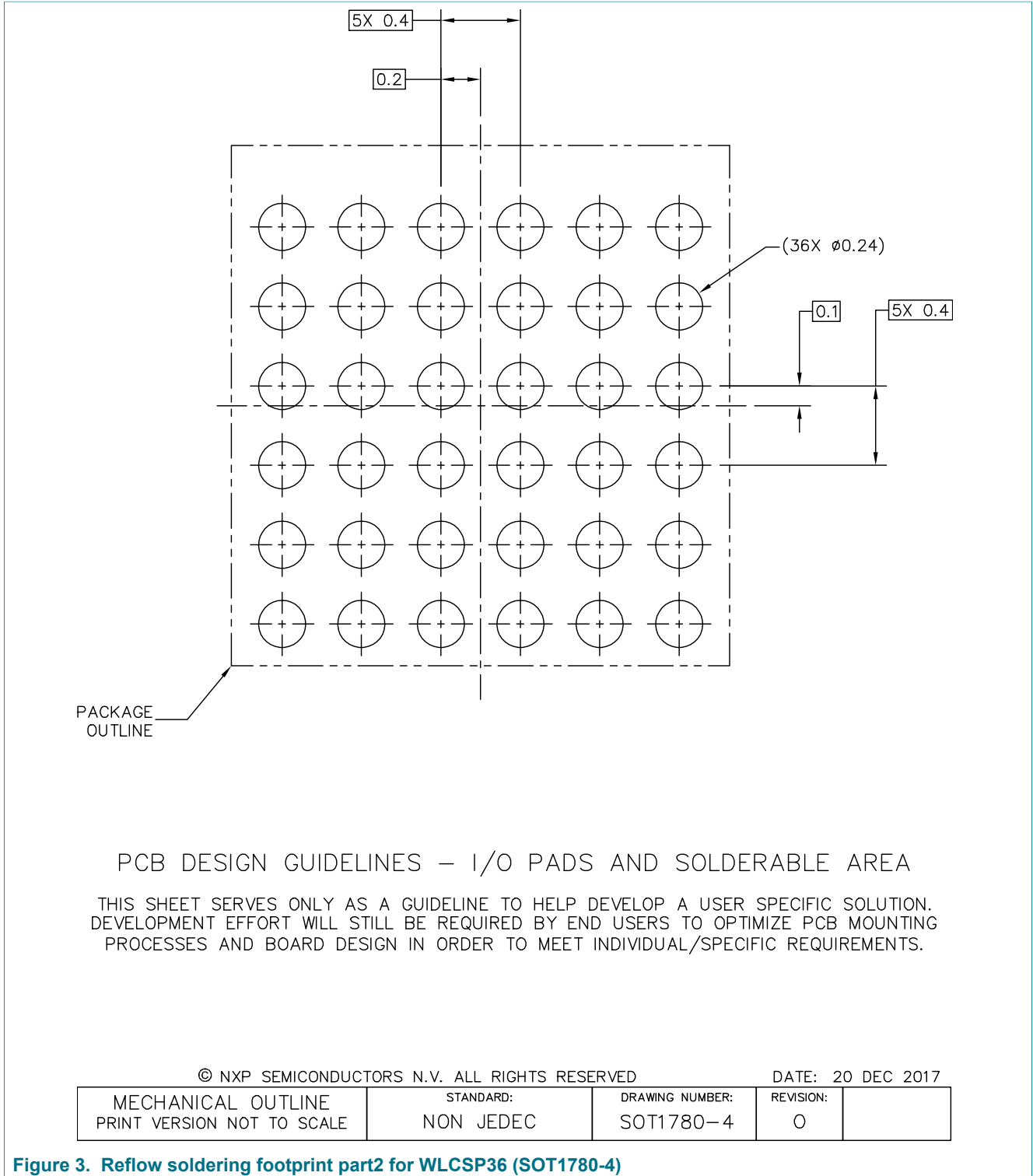


Figure 3. Reflow soldering footprint part2 for WLCSP36 (SOT1780-4)

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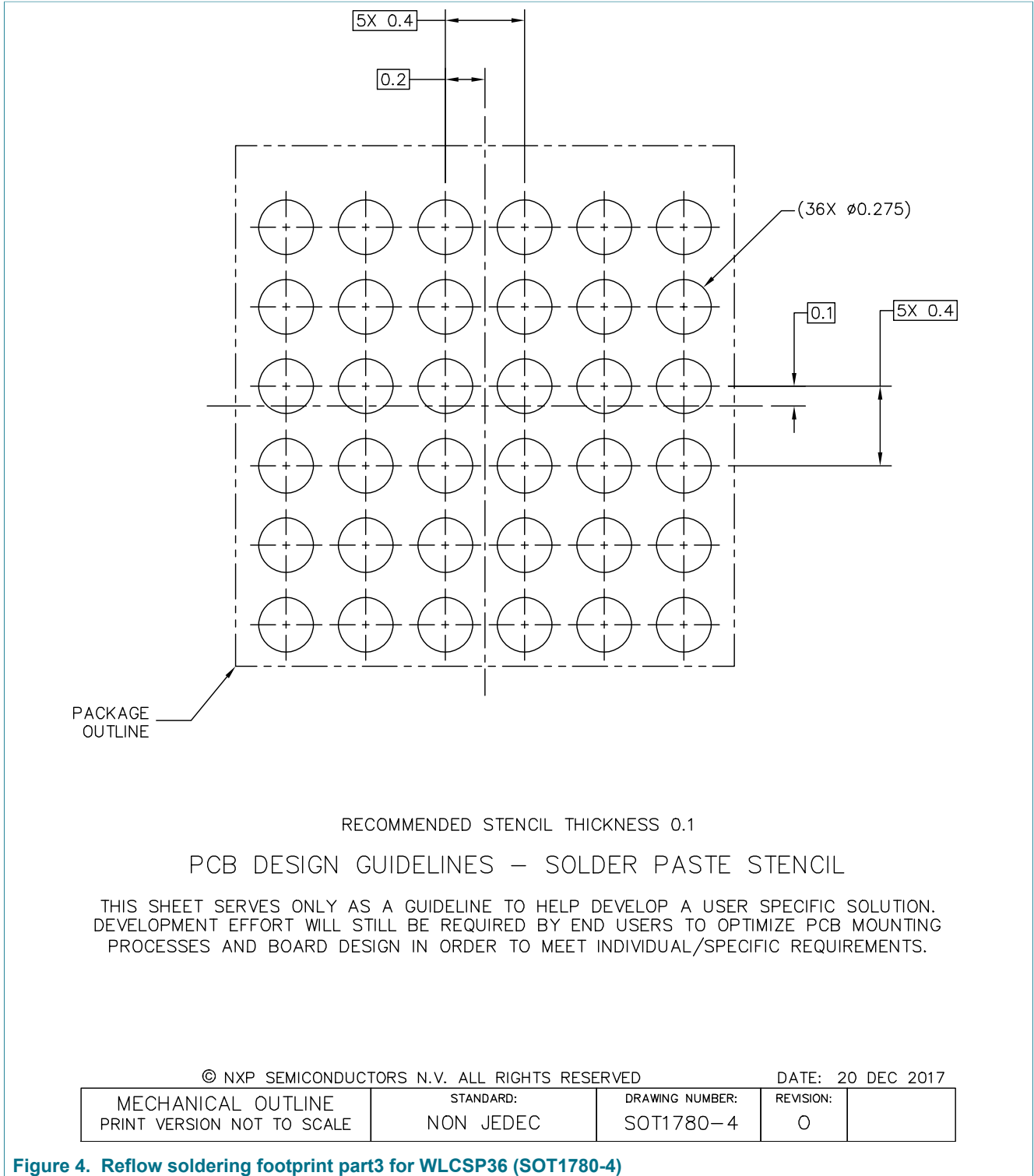


Figure 4. Reflow soldering footprint part3 for WLCSP36 (SOT1780-4)

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NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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DATE: 20 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1780-4	REVISION: 0	
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Figure 5. Package outline note WLCSP36 (SOT1780-4)

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## 4 Legal information

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