

# SOT1780-7

WLCSP36, wafer level chip-scale package; 36 bumps; 0.4 mm pitch, 2.62 mm x 2.51 mm x 0.525 mm body

4 October 2017

Package information

## 1. Package summary

<b>Terminal position code</b>	B (bottom)
<b>Package type descriptive code</b>	WLCSP36
<b>Package type industry code</b>	WLCSP36
<b>Package style descriptive code</b>	WLCSP (wafer level chip-size package)
<b>Mounting method type</b>	S (surface mount)
<b>Issue date</b>	18-9-2017
<b>Manufacturer package code</b>	SOT1780-7

Table 1. Package summary

Symbol	Parameter	Min	Typ	Nom	Max	Unit
D	package length	-	-	2.62	-	mm
E	package width	-	-	2.51	-	mm
A	seated height	-	-	0.525	-	mm
e	nominal pitch	-	-	0.4	-	mm
n <sub>2</sub>	actual quantity of termination	-	-	36	-	A/A



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## 2. Package outline

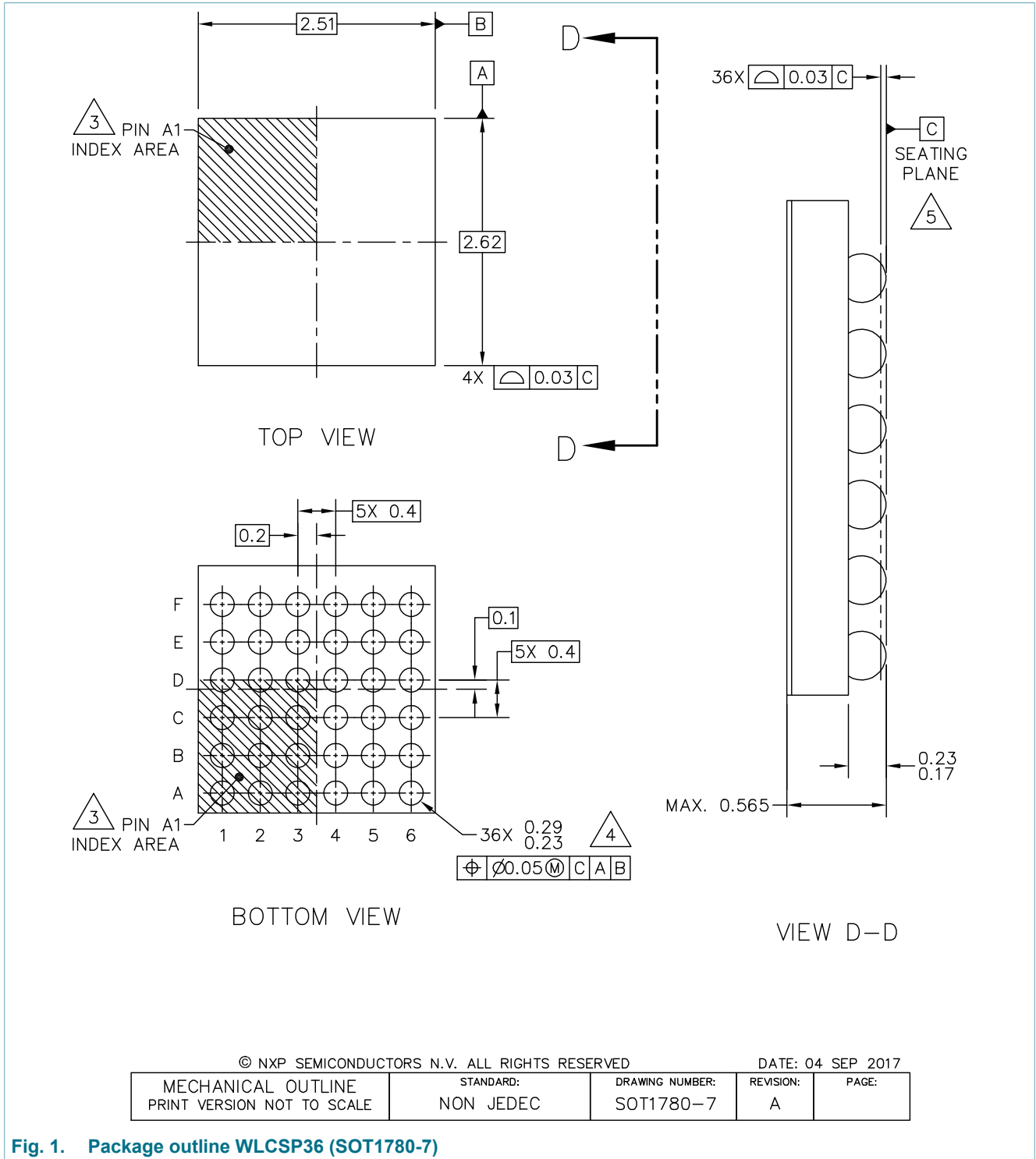





Fig. 1. Package outline WLCSP36 (SOT1780-7)

WLCSP36, wafer level chip-scale package; 36 bumps; 0.4 mm pitch, 2.62 mm x 2.51 mm x 0.525 mm  
body

## NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3.  PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4.  MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5.  DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

**Fig. 2. Package outline note WLCSP36 (SOT1780-7)**

### 3. Soldering

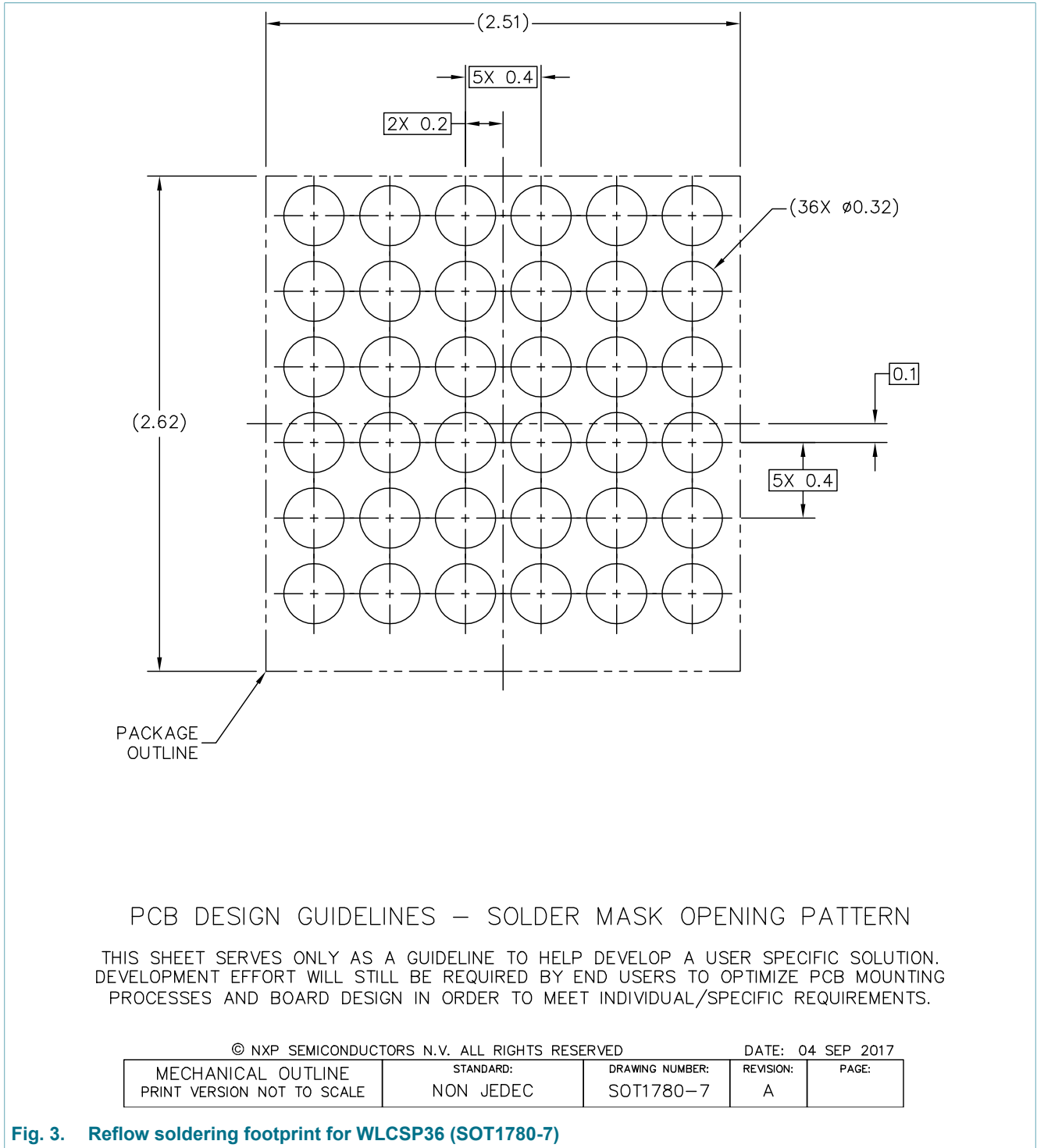
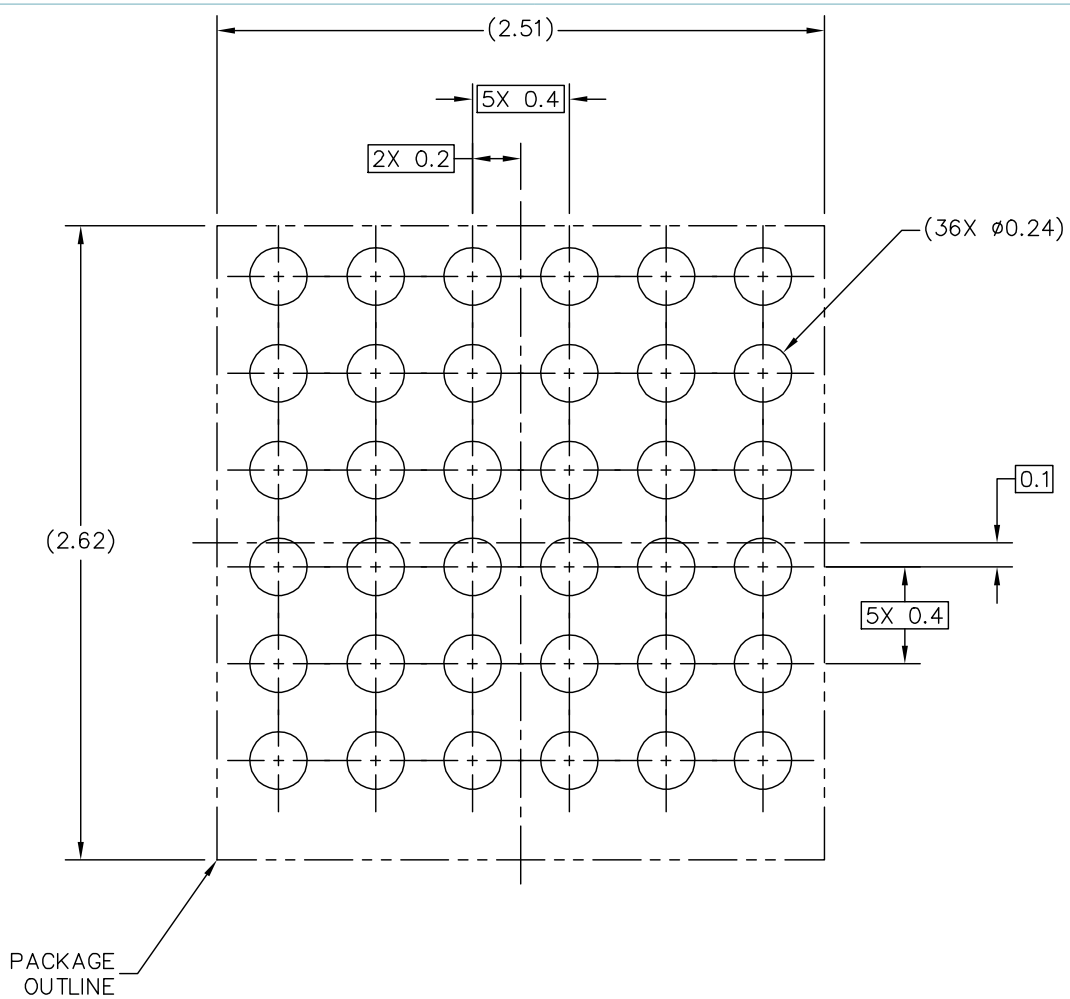


Fig. 3. Reflow soldering footprint for WLCSP36 (SOT1780-7)

WLCSP36, wafer level chip-scale package; 36 bumps; 0.4 mm pitch, 2.62 mm x 2.51 mm x 0.525 mm body



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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DATE: 04 SEP 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1780-7	REVISION: A	PAGE:
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Fig. 4. Reflow soldering footprint part2 for WLCSP36 (SOT1780-7)

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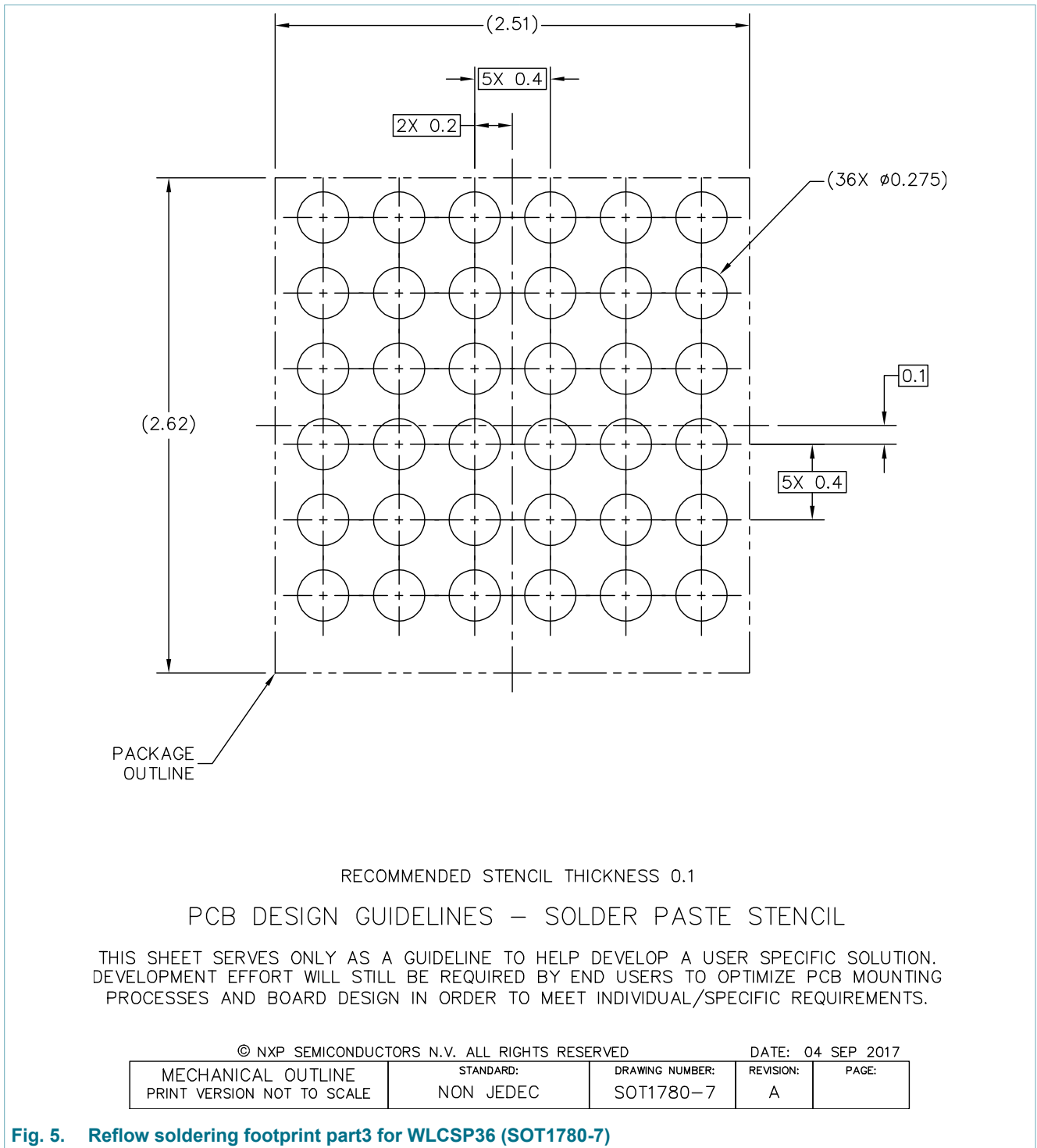


Fig. 5. Reflow soldering footprint part3 for WLCSP36 (SOT1780-7)

## 4. Legal information

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