

# SOT1887-2

WLCSP48, wafer level chip-scale package; 48 bumps; 0.4 mm pitch, 2.51 mm x 3.55 mm x 0.5 mm body

11 January 2018

Package information

## 1. Package summary

<b>Terminal position code</b>	B (bottom)
<b>Package type descriptive code</b>	WLCSP48
<b>Package type industry code</b>	WLCSP48
<b>Package style descriptive code</b>	WLCSP (wafer level chip-size package)
<b>Mounting method type</b>	S (surface mount)
<b>Issue date</b>	11-12-2017
<b>Manufacturer package code</b>	98ASA01162D

Table 1. Package summary

Symbol	Parameter	Min	Typ	Nom	Max	Unit
D	package length	-	-	2.51	-	mm
E	package width	-	-	3.55	-	mm
A	seated height	-	-	0.5	-	mm
e	nominal pitch	-	-	0.4	-	mm
n <sub>2</sub>	actual quantity of termination	-	-	48	-	A/A



## 2. Package outline

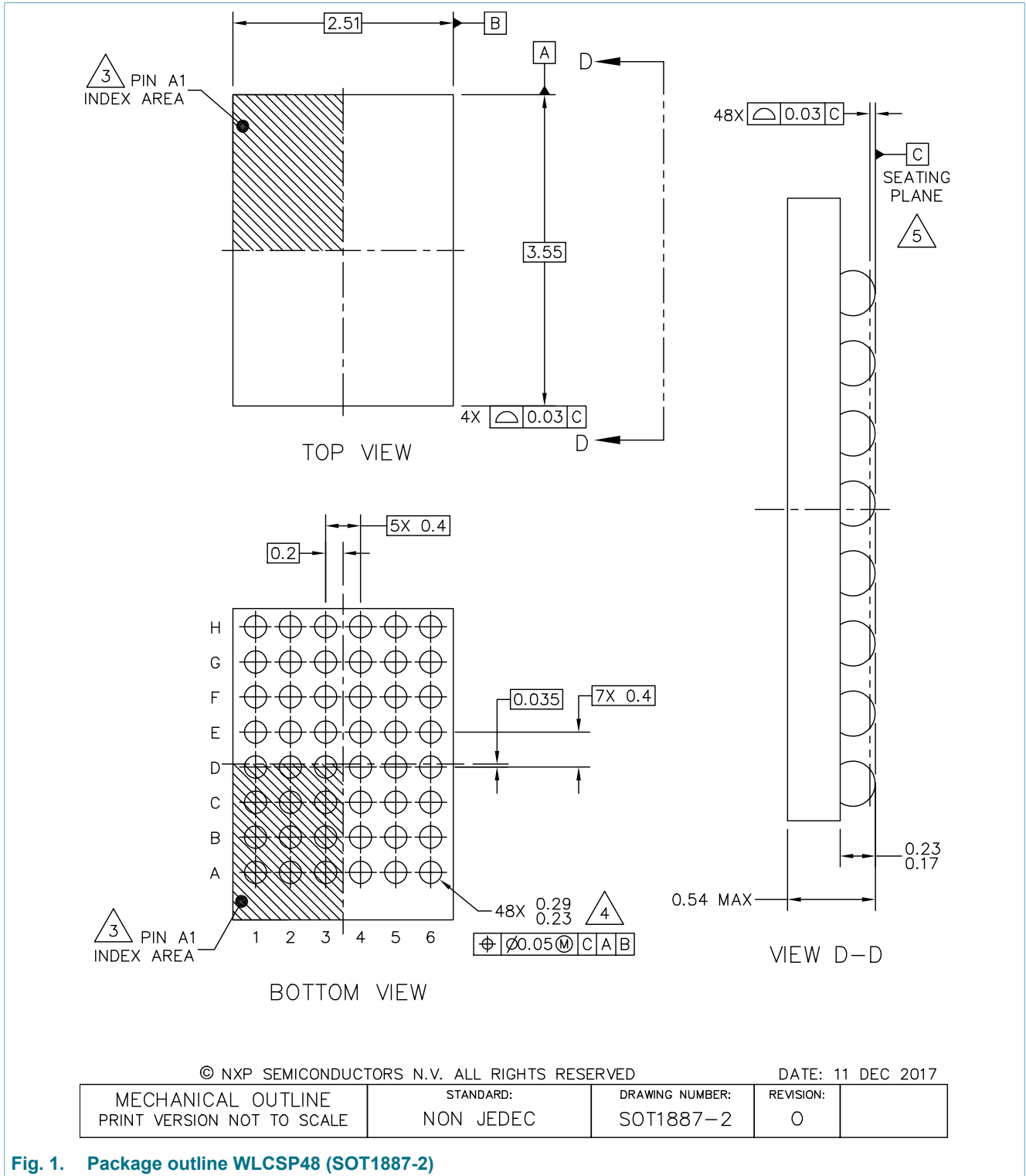


Fig. 1. Package outline WLCSP48 (SOT1887-2)

WLCSP48, wafer level chip-scale package; 48 bumps; 0.4 mm pitch, 2.51 mm x 3.55 mm x 0.5 mm body

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED

DATE: 11 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1887-2	REVISION: 0	
--	------------------------	------------------------------	----------------	--

Fig. 2. Package outline note WLCSP48 (SOT1887-2)

### 3. Soldering

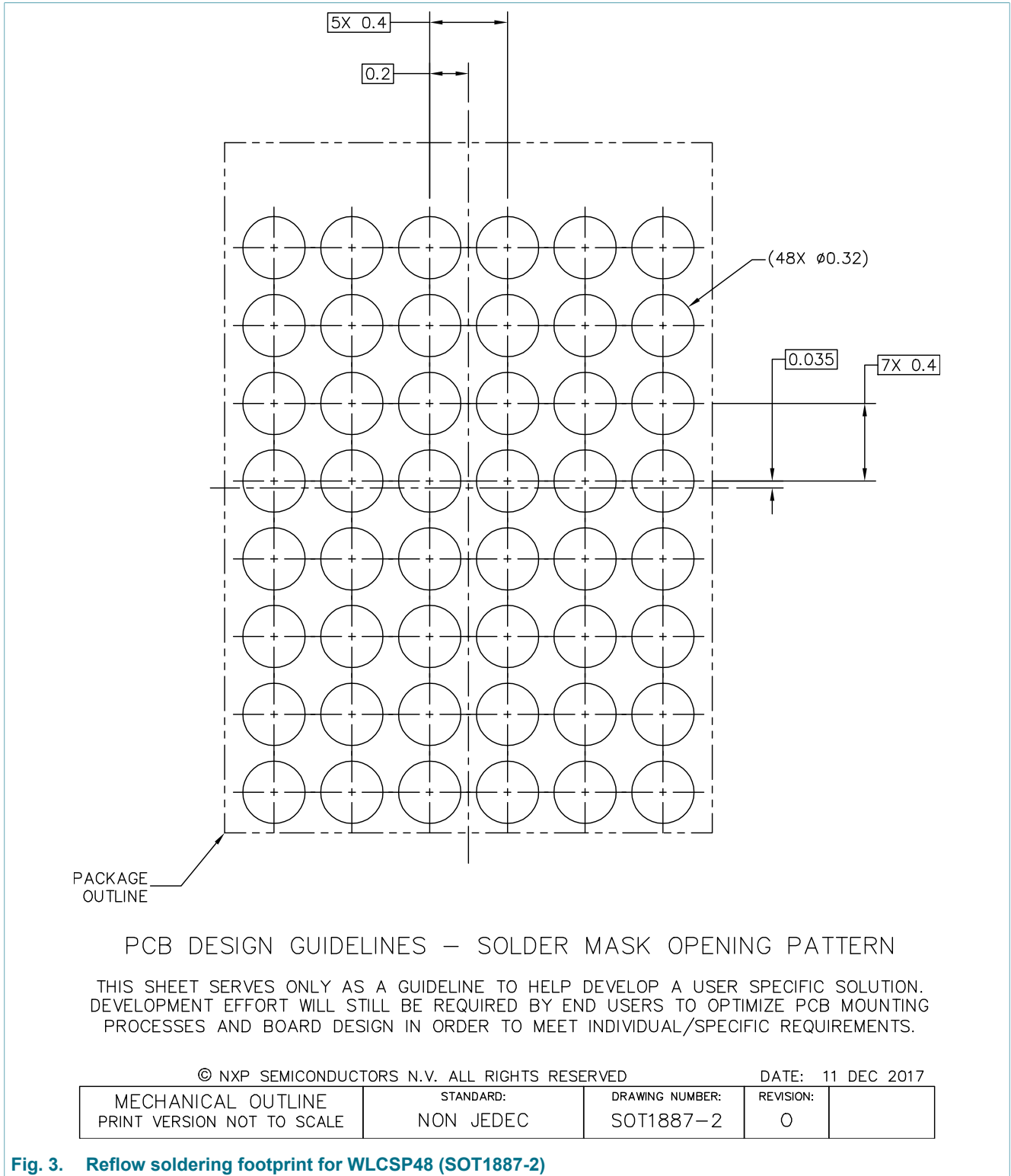
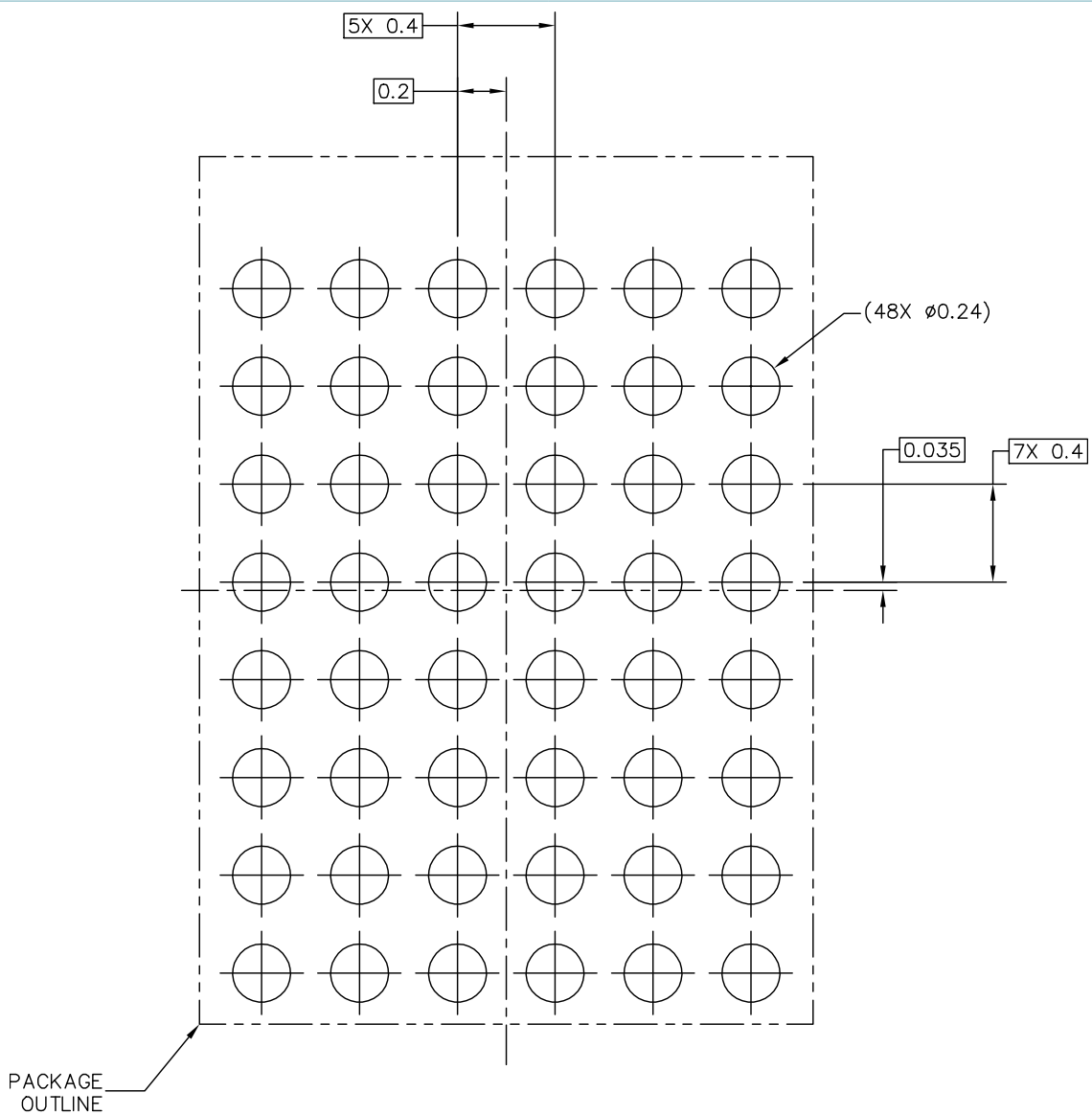


Fig. 3. Reflow soldering footprint for WLCSP48 (SOT1887-2)

WLCSP48, wafer level chip-scale package; 48 bumps; 0.4 mm pitch, 2.51 mm x 3.55 mm x 0.5 mm body



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

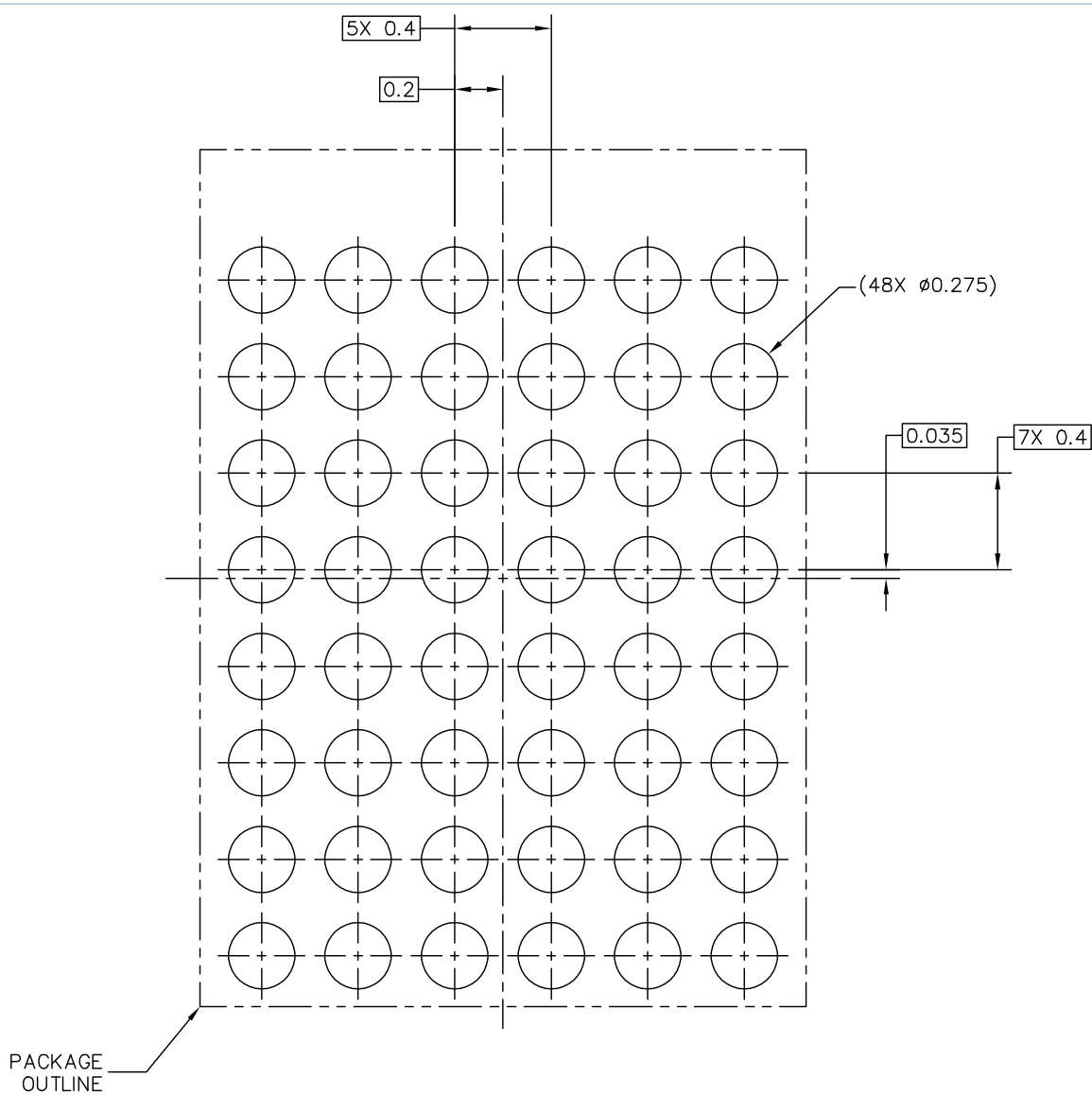
© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED

DATE: 11 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1887-2	REVISION: 0	
--	------------------------	------------------------------	----------------	--

Fig. 4. Reflow soldering footprint part2 for WLCSP48 (SOT1887-2)

WLCSP48, wafer level chip-scale package; 48 bumps; 0.4 mm pitch, 2.51 mm x 3.55 mm x 0.5 mm body



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED

DATE: 11 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1887-2	REVISION: 0	
--	------------------------	------------------------------	----------------	--

Fig. 5. Reflow soldering footprint part3 for WLCSP48 (SOT1887-2)

## 4. Legal information

---

### Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

WLCSP48, wafer level chip-scale package; 48 bumps; 0.4 mm pitch, 2.51 mm x 3.55 mm x 0.5 mm body

## 5. Contents

---

1. Package summary.....	1
2. Package outline.....	2
3. Soldering.....	4
4. Legal information.....	7

---

© NXP B.V. 2018. All rights reserved

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 11 January 2018

---