

SOT1887-5

WLCSP48, wafer level chip-scale package; 48 bumps; 0.4 mm pitch, 2.51 mm x 3.55 mm x 0.525 mm body

10 January 2018

Package information

1. Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP48
Package type industry code	WLCSP48
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	8-12-2017
Manufacturer package code	98ASA01165D

Table 1. Package summary

Symbol	Parameter	Min	Typ	Nom	Max	Unit
D	package length	-	-	2.51	-	mm
E	package width	-	-	3.55	-	mm
A	seated height	-	-	0.525	-	mm
e	nominal pitch	-	-	0.4	-	mm
n ₂	actual quantity of termination	-	-	48	-	A/A



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2. Package outline

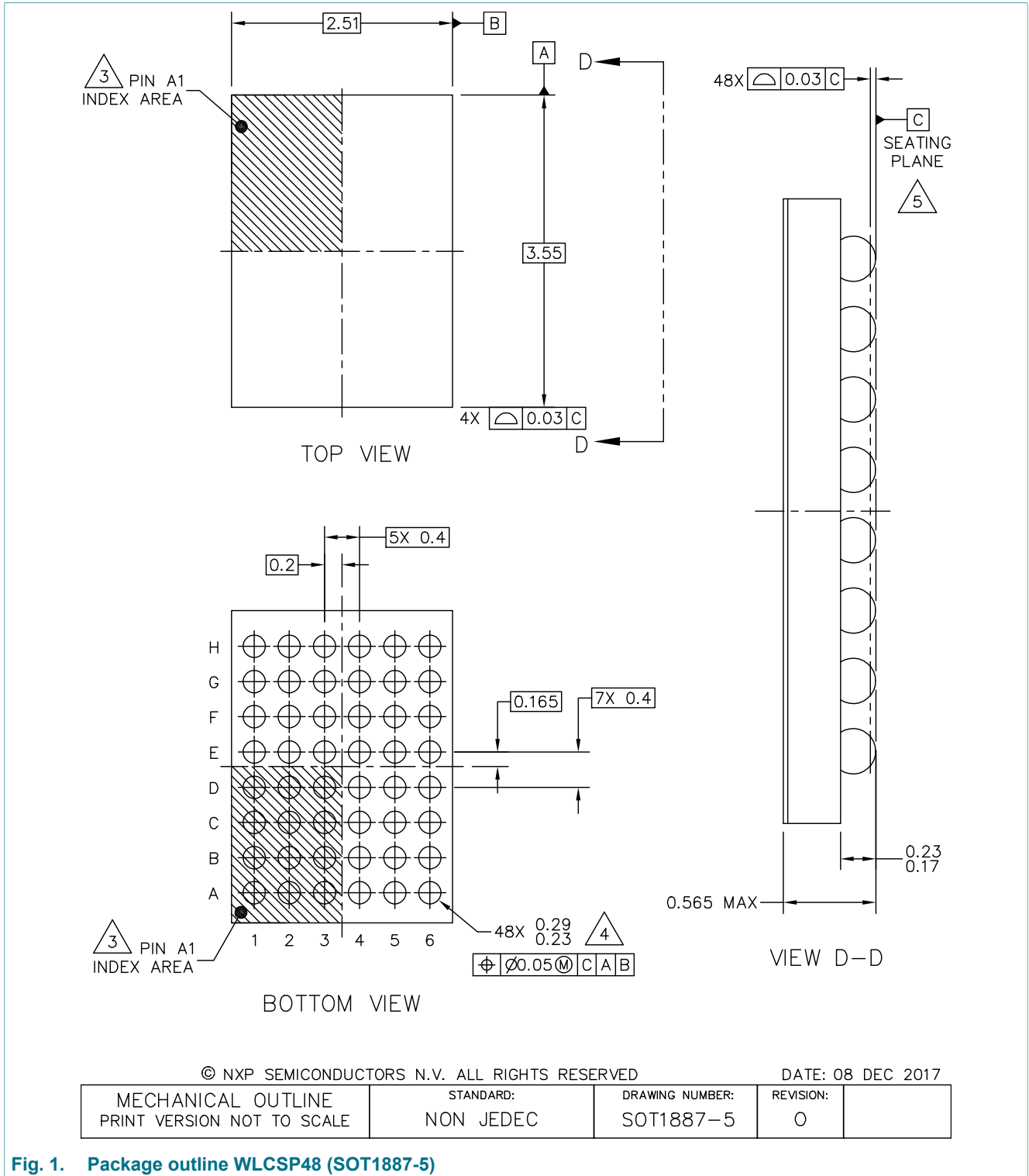


Fig. 1. Package outline WLCSP48 (SOT1887-5)

WLCSP48, wafer level chip-scale package; 48 bumps; 0.4 mm pitch, 2.51 mm x 3.55 mm x 0.525 mm body

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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DATE: 08 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1887-5	REVISION: 0	
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Fig. 2. Package outline note WLCSP48 (SOT1887-5)

3. Soldering

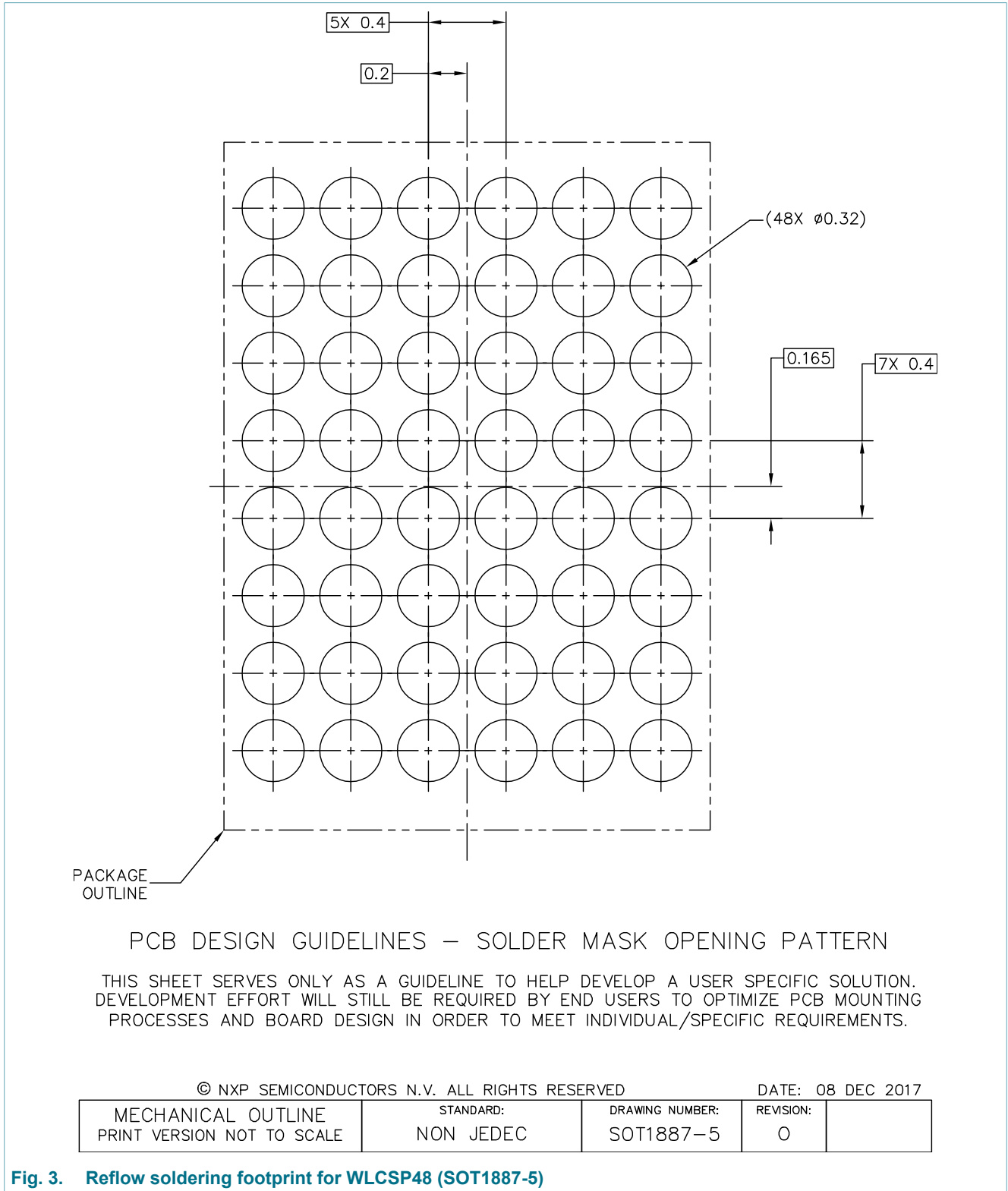


Fig. 3. Reflow soldering footprint for WLCSP48 (SOT1887-5)

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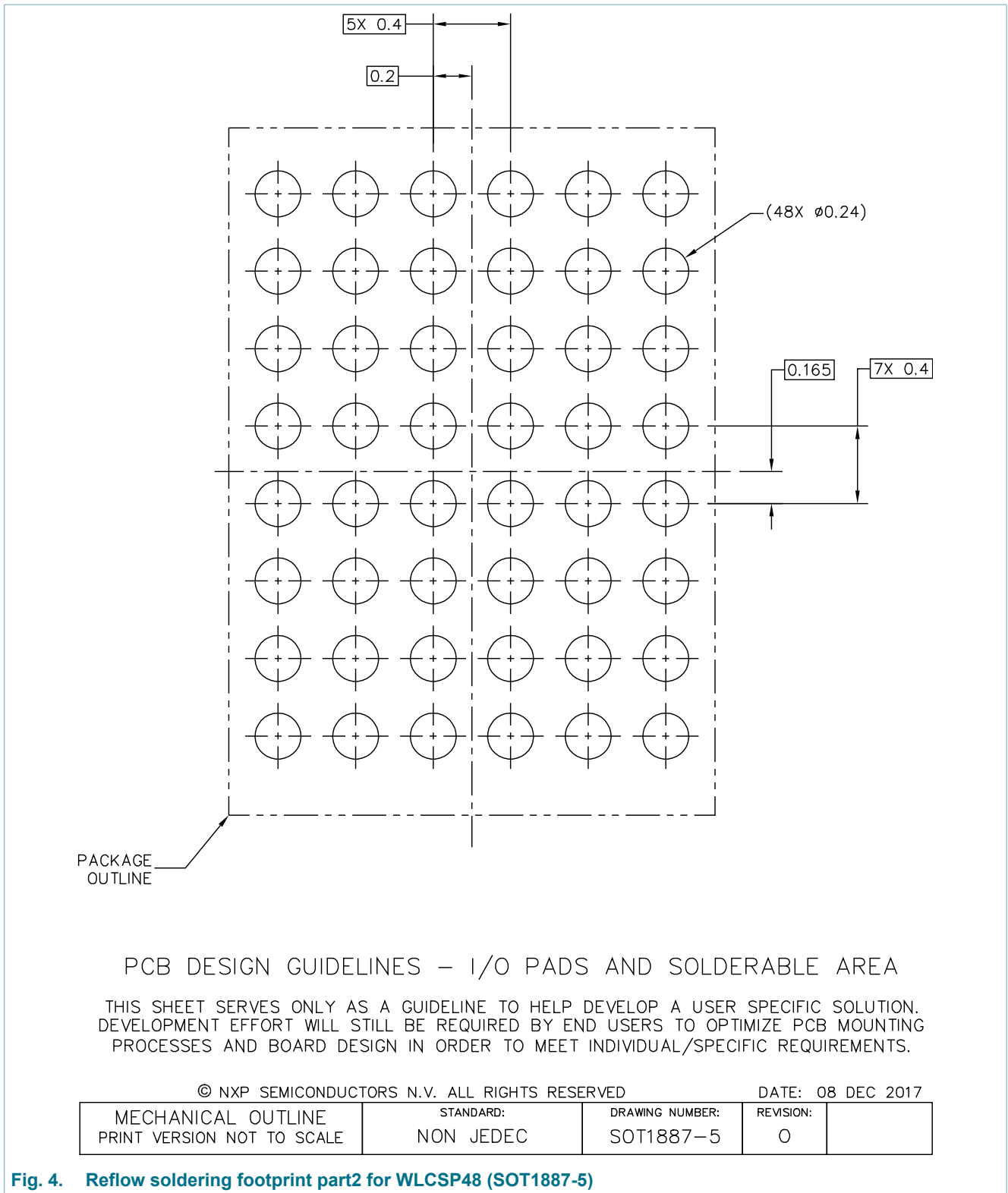
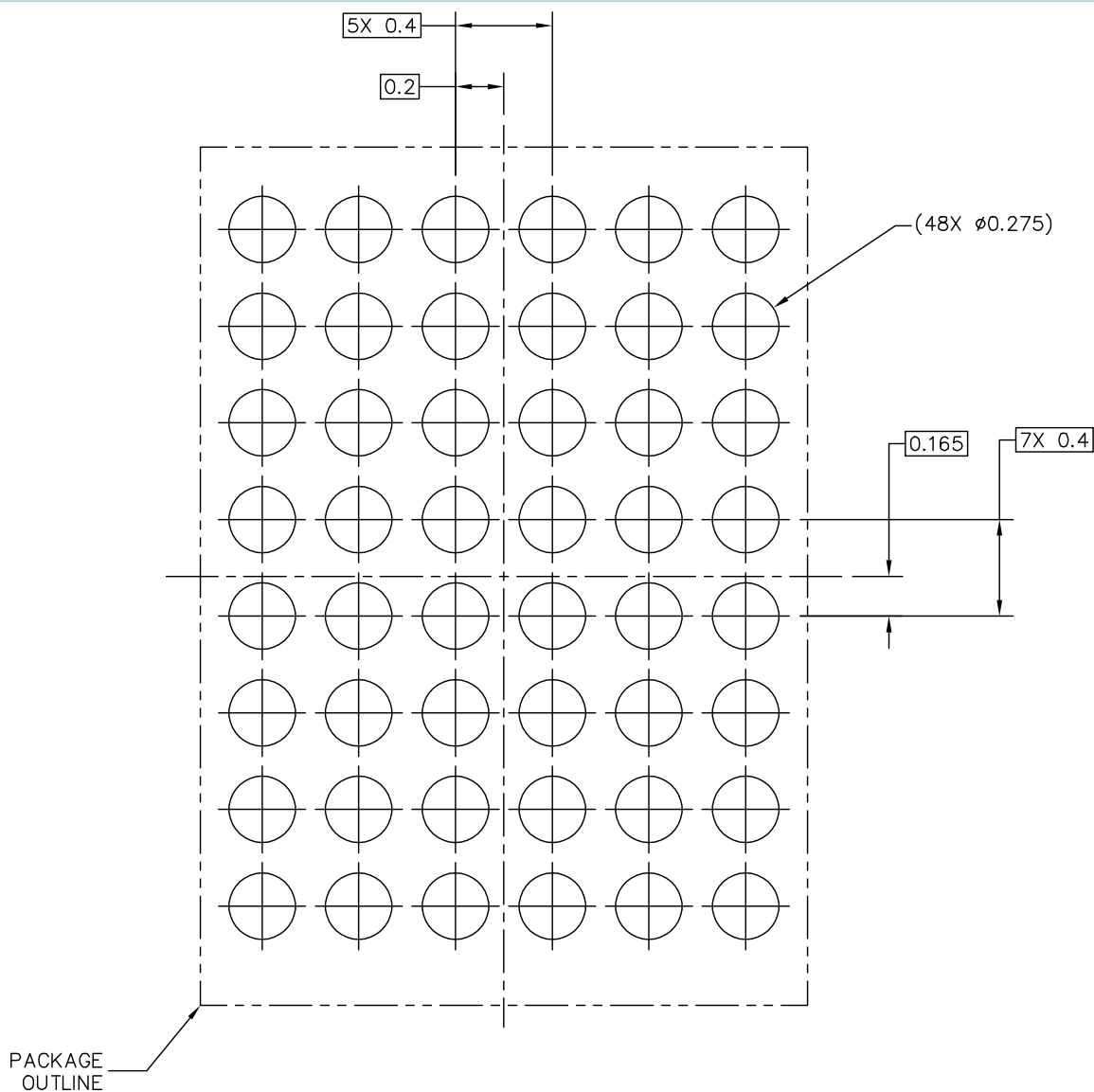


Fig. 4. Reflow soldering footprint part2 for WLCSP48 (SOT1887-5)

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RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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Fig. 5. Reflow soldering footprint part3 for WLCSP48 (SOT1887-5)

4. Legal information

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