

SOT1890-3

WLCSP56, wafer level chip-scale package; 56 bumps; 0.35 mm pitch, 2.95 mm x 2.6 mm x 0.415 mm body (backside coating included)

4 October 2019

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP56
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	23-01-2019
Manufacturer package code	98ASA01353D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	2.92	2.95	2.98	mm
package width	2.57	2.6	2.63	mm
seated height	-	0.415	0.45	mm
nominal pitch	-	0.35	-	mm
actual quantity of termination	-	56	-	



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2 Package outline

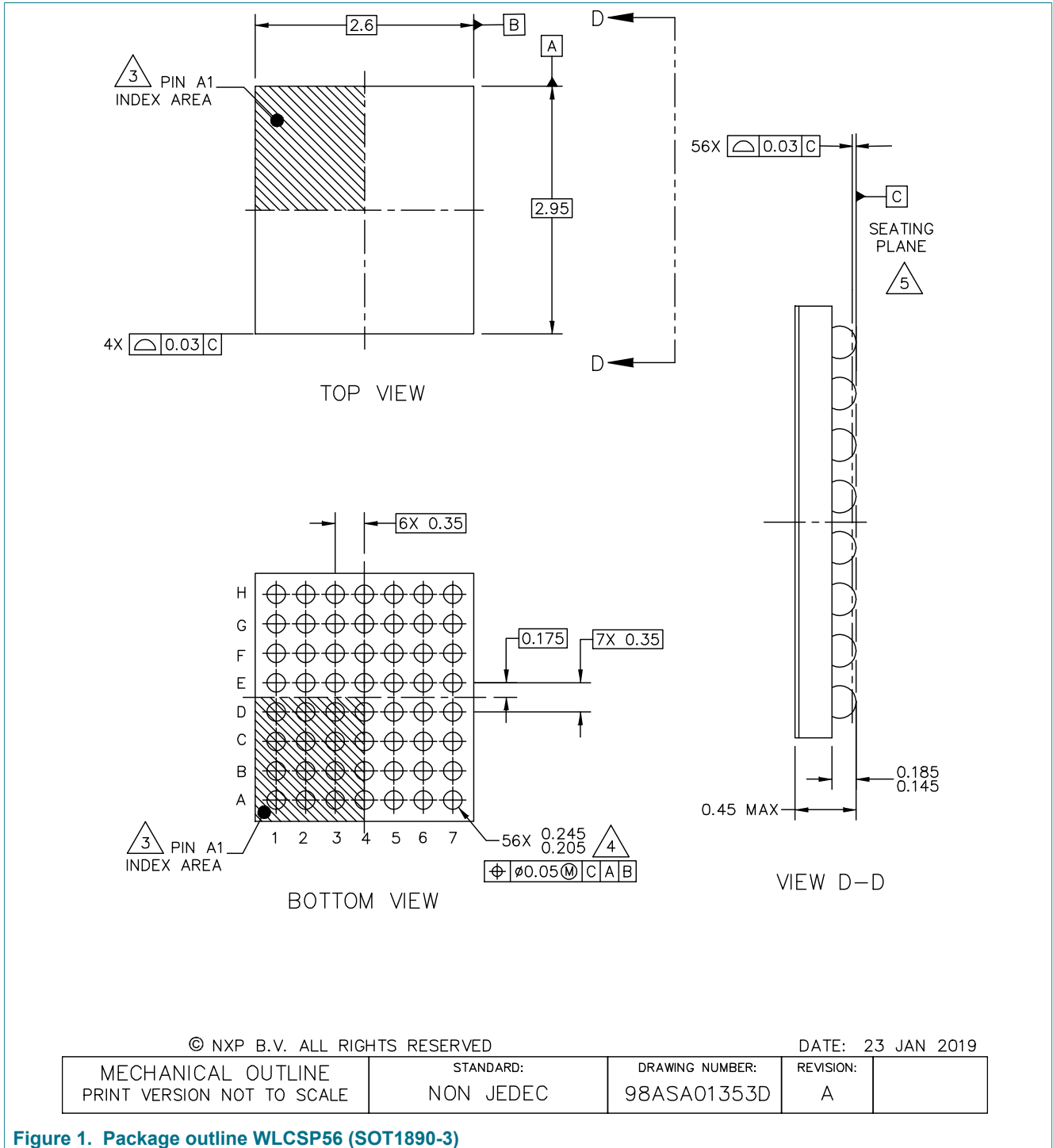


Figure 1. Package outline WLCSP56 (SOT1890-3)

WLCSP56, wafer level chip-scale package; 56 bumps; 0.35 mm pitch, 2.95 mm x 2.6 mm x 0.415 mm body (backside coating included)

3 Soldering

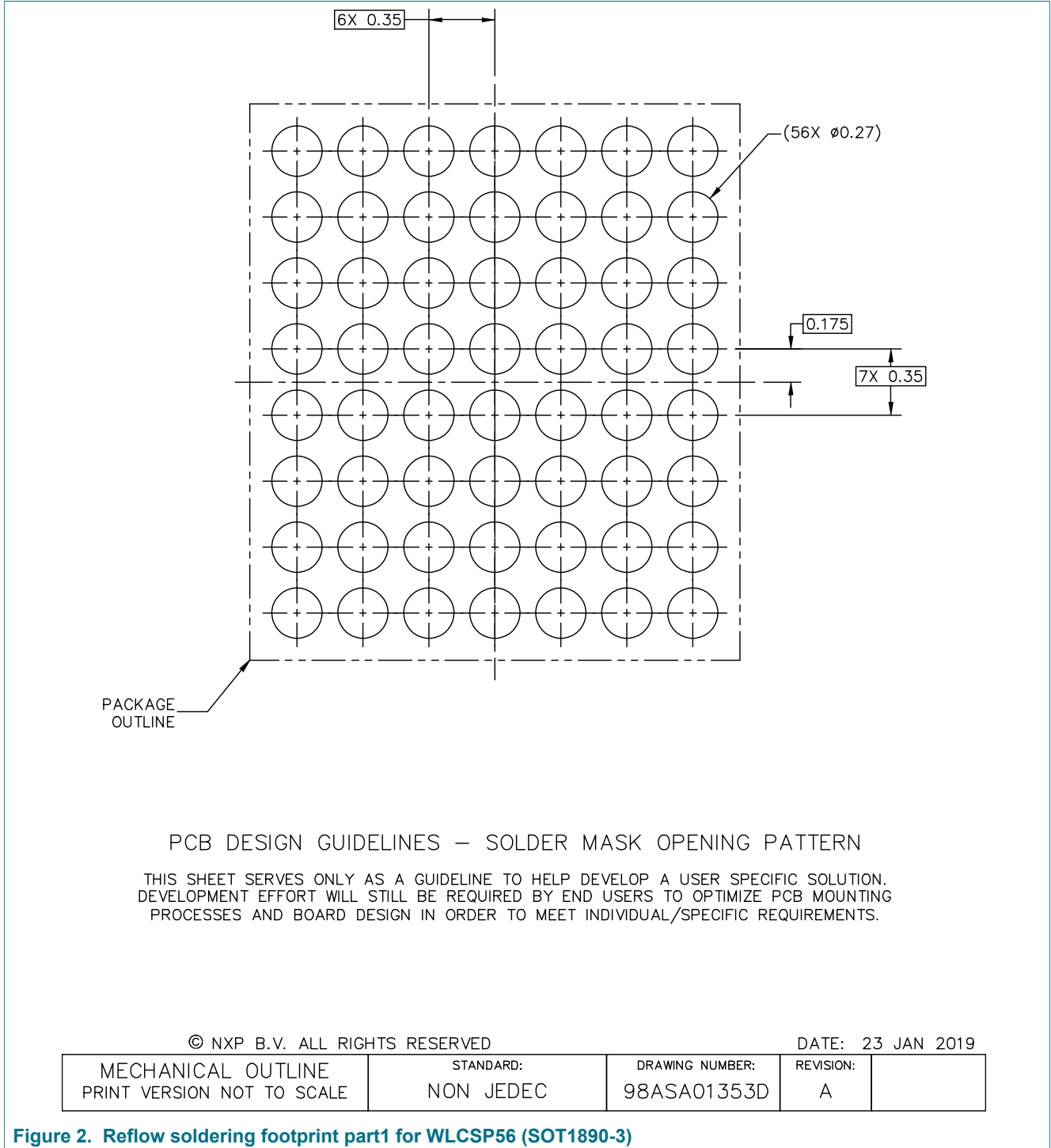


Figure 2. Reflow soldering footprint part1 for WLCSP56 (SOT1890-3)

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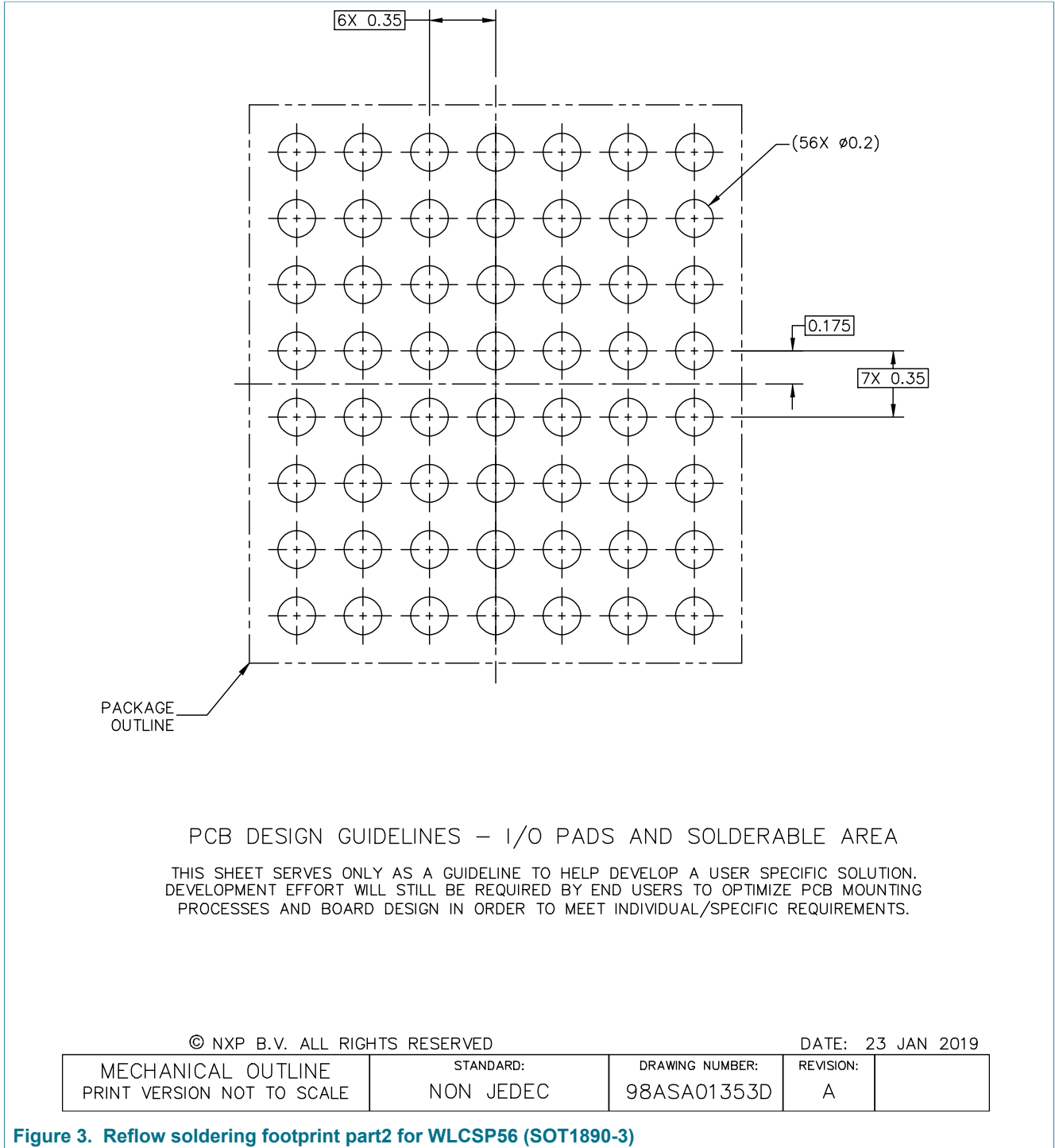
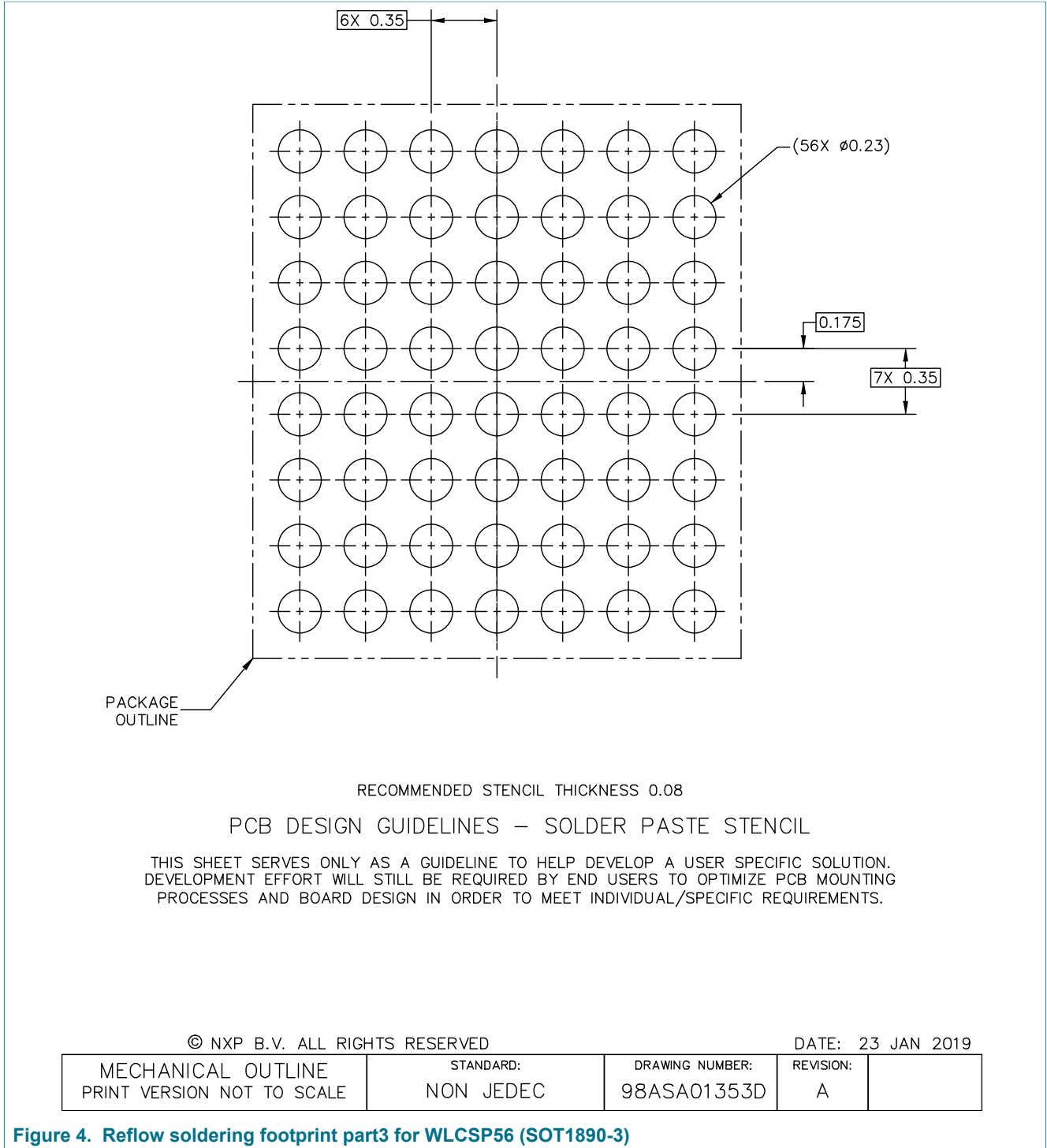


Figure 3. Reflow soldering footprint part2 for WLCSP56 (SOT1890-3)

WLCSP56, wafer level chip-scale package; 56 bumps; 0.35 mm pitch, 2.95 mm x 2.6 mm x 0.415 mm body (backside coating included)



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NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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DATE: 23 JAN 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01353D	REVISION: A	
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Figure 5. Package outline note WLCSP56 (SOT1890-3)

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