



# SOT1934-1

HLLGA17R, thermal enhanced low profile land grid array package, 17 terminals, 0.65 mm pitch, 4 mm x 3 mm x 1.348 mm body

27 June 2019

Package information

## 1 Package summary

<b>Package type descriptive code</b>	HLLGA17R
<b>Package style descriptive code</b>	HLLGA (thermal enhanced low profile land grid array)
<b>Package body material type</b>	P (plastic)
<b>Mounting method type</b>	S (surface mount)
<b>Issue date</b>	18-02-2019
<b>Manufacturer package code</b>	98ASA01096D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	4	-	mm
package width	-	3	-	mm
seated height	-	1.348	-	mm
nominal pitch	-	0.65	-	mm
actual quantity of termination	-	17	-	



2 Package outline

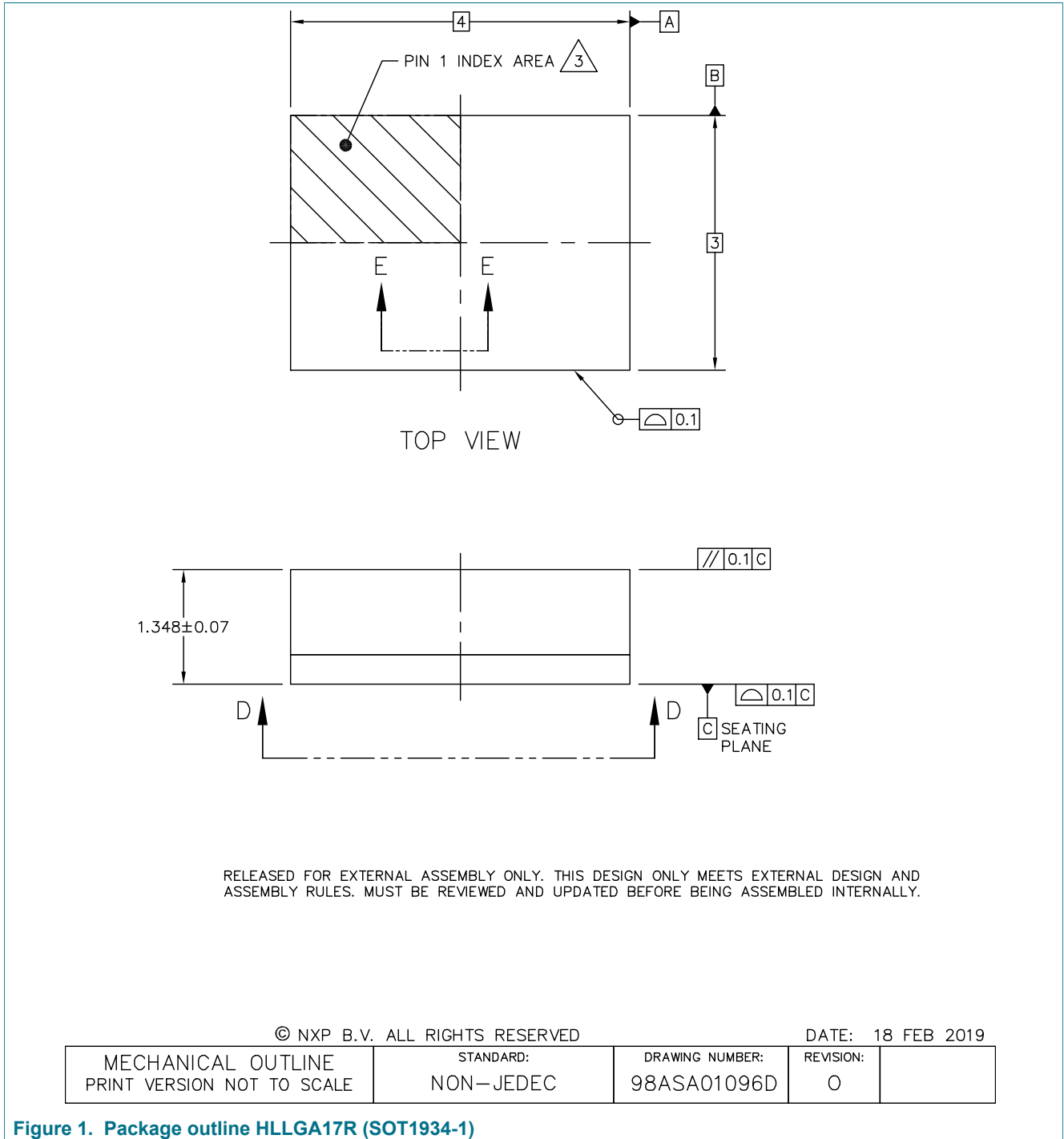
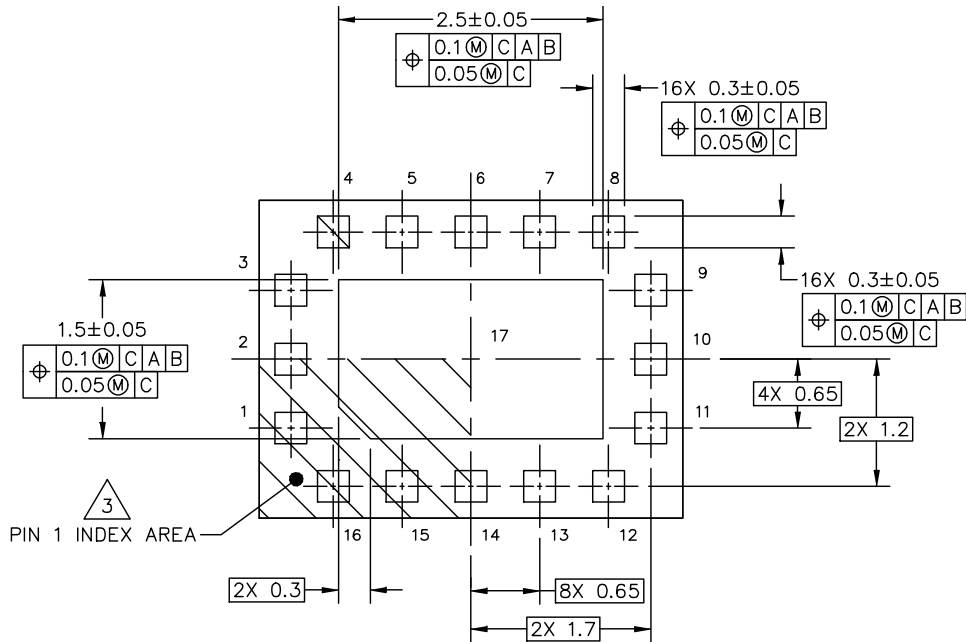
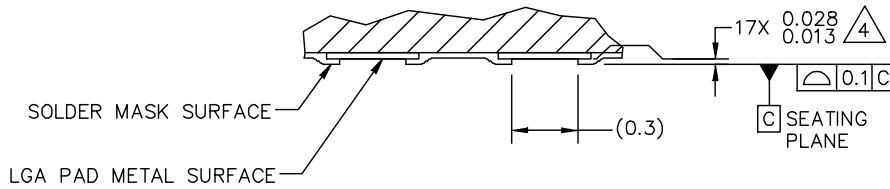


Figure 1. Package outline HLLGA17R (SOT1934-1)

HLLGA17R, thermal enhanced low profile land grid array package, 17 terminals, 0.65 mm pitch, 4 mm x 3 mm x 1.348 mm body



VIEW D-D  
(BOTTOM VIEW)



SECTION E-E

RELEASED FOR EXTERNAL ASSEMBLY ONLY. THIS DESIGN ONLY MEETS EXTERNAL DESIGN AND ASSEMBLY RULES. MUST BE REVIEWED AND UPDATED BEFORE BEING ASSEMBLED INTERNALLY.

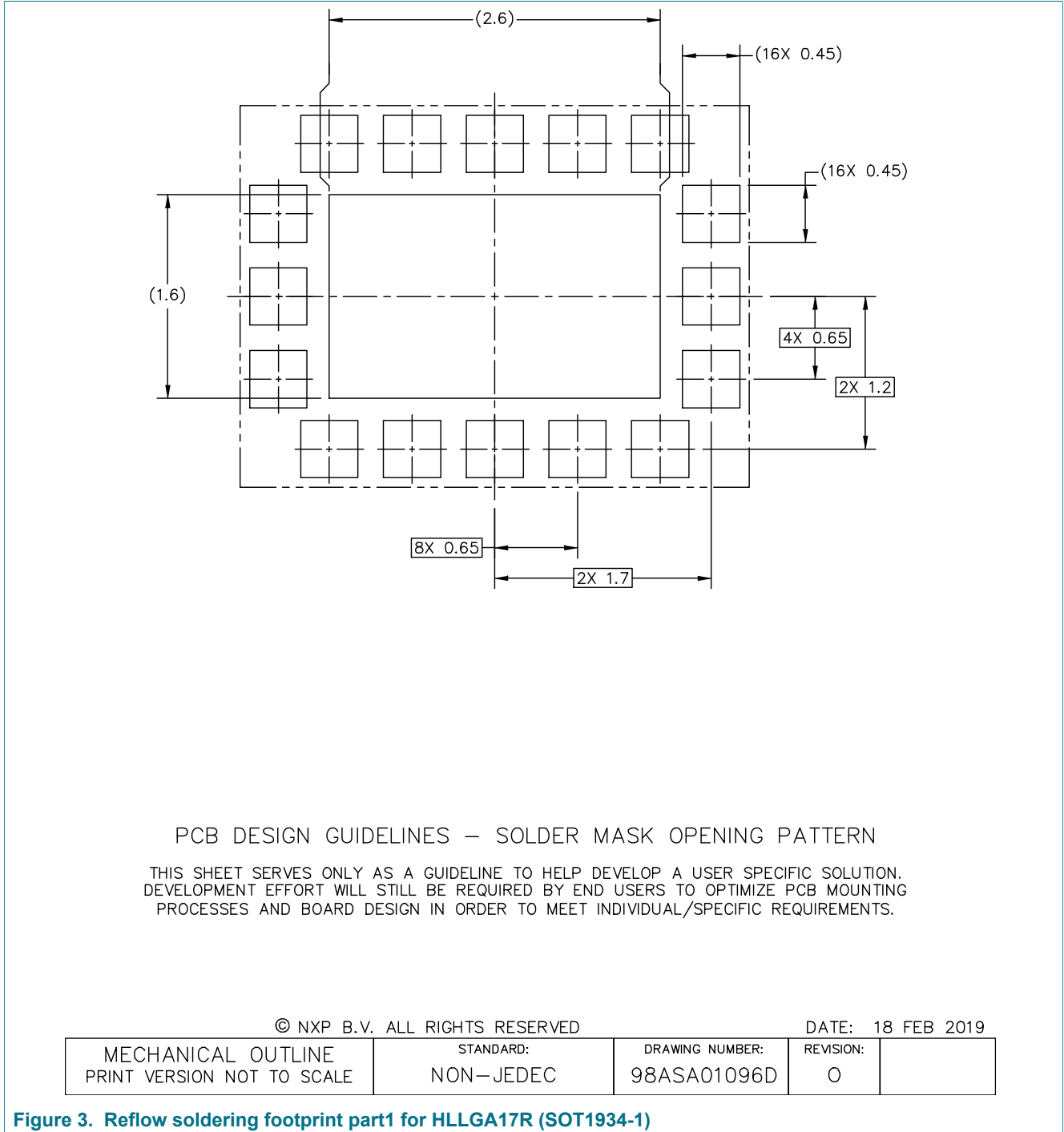
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DATE: 18 FEB 2019

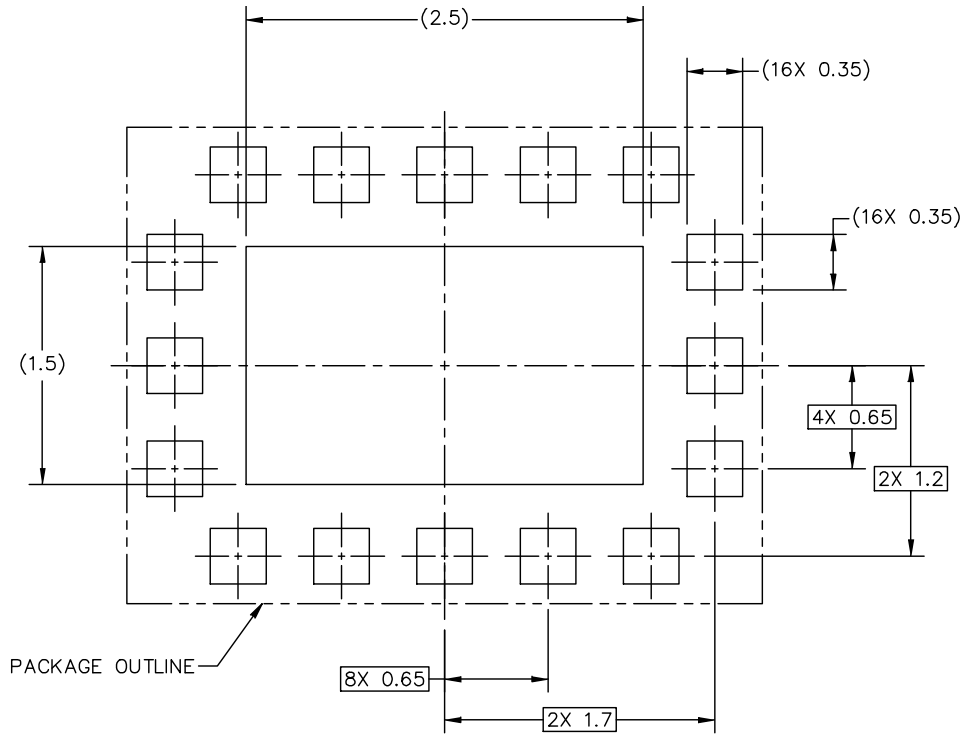
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01096D	REVISION: O
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Figure 2. Package outline detail HLLGA17R (SOT1934-1)

3 Soldering



HLLGA17R, thermal enhanced low profile land grid array package, 17 terminals, 0.65 mm pitch, 4 mm x 3 mm x 1.348 mm body



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREAS

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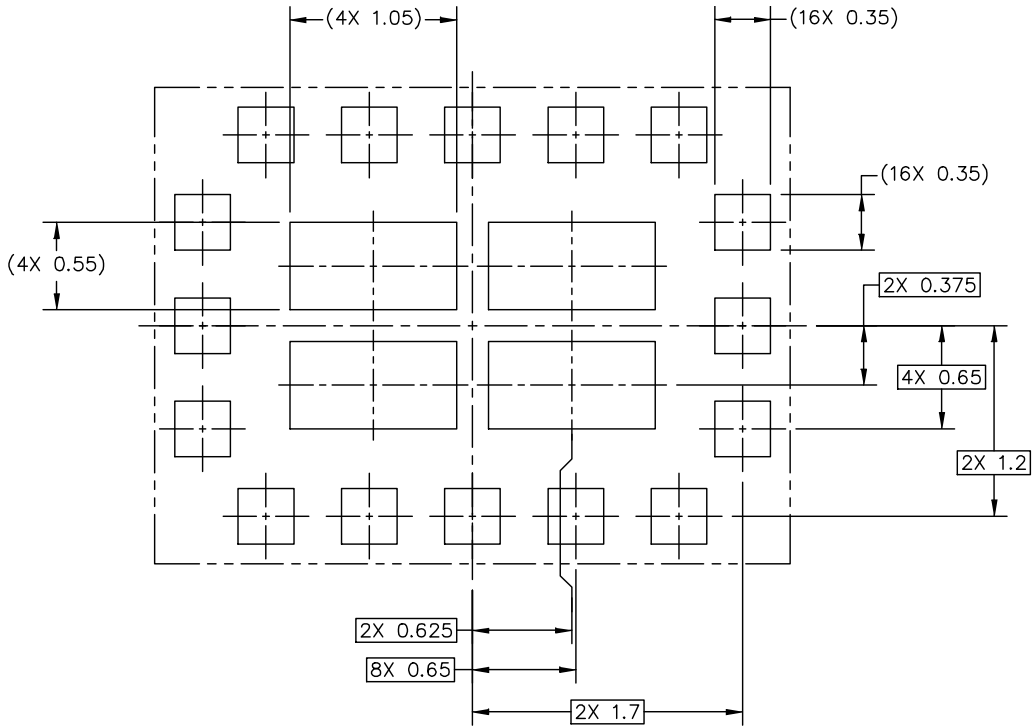
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Figure 4. Reflow soldering footprint part2 for HLLGA17R (SOT1934-1)

HLLGA17R, thermal enhanced low profile land grid array package, 17 terminals, 0.65 mm pitch, 4 mm x 3 mm x 1.348 mm body



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 5. Reflow soldering footprint part3 for HLLGA17R (SOT1934-1)

HLLGA17R, thermal enhanced low profile land grid array package, 17 terminals, 0.65 mm pitch, 4 mm x 3 mm x 1.348 mm body

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
- 4. DIMENSION APPLIES TO ALL LEADS AND FLAG.

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Figure 6. Package outline note HLLGA17R (SOT1934-1)

## 4 Legal information

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