

SOT2035-1

WLCSP12, wafer level chip scale package, 12 terminals, 0.25 mm pitch, 1.185 mm x 0.935 mm x 0.22 mm body

27 January 2020

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP12
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	24-10-2019
Manufacturer package code	98ASA01491D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	0.905	0.935	0.965	mm
package width	1.155	1.185	1.215	mm
package height	-	0.22	0.24	mm
nominal pitch	-	0.25	-	mm
actual quantity of termination	-	12	-	



WLCSP12, wafer level chip scale package, 12 terminals, 0.25 mm pitch, 1.185 mm x 0.935 mm x 0.22 mm body

2 Package outline

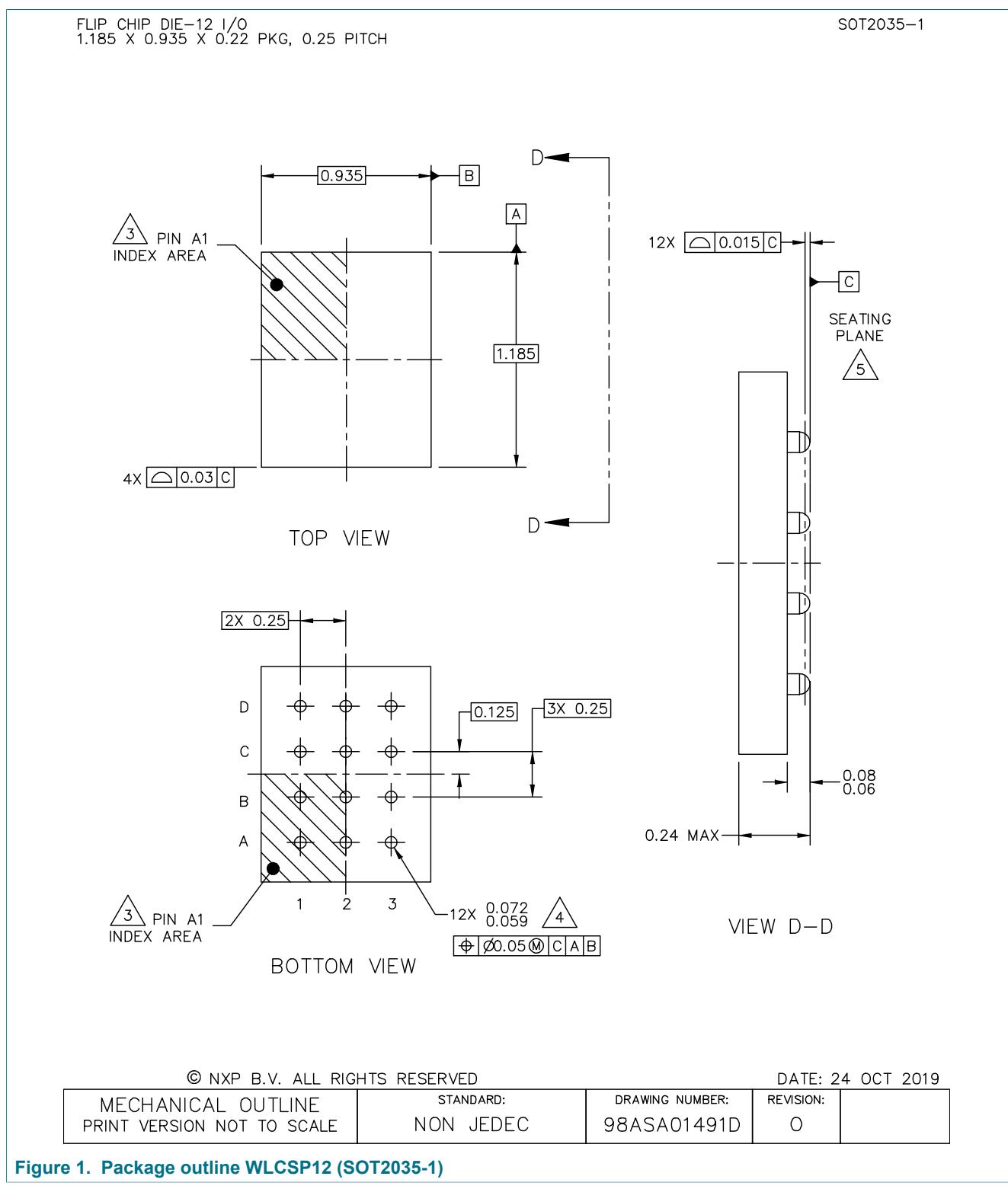


Figure 1. Package outline WLCSP12 (SOT2035-1)

WLCSP12, wafer level chip scale package, 12 terminals, 0.25 mm pitch, 1.185 mm x 0.935 mm x 0.22 mm bodyFLIP CHIP DIE-12 I/O
1.185 X 0.935 X 0.22 PKG, 0.25 PITCH

SOT2035-1

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

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DATE: 24 OCT 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01491D	REVISION: O	
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Figure 2. Package outline note WLCSP12 (SOT2035-1)

3 Legal information

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