

SOT2057-1

WLCSP70, wafer level chip scale package, 70 terminals, 0.4 mm pitch, 4.16 mm x 2.96 mm x 0.525 mm body (backside coating included)

29 May 2020

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP70
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	20-05-2020
Manufacturer package code	98ASA01576D

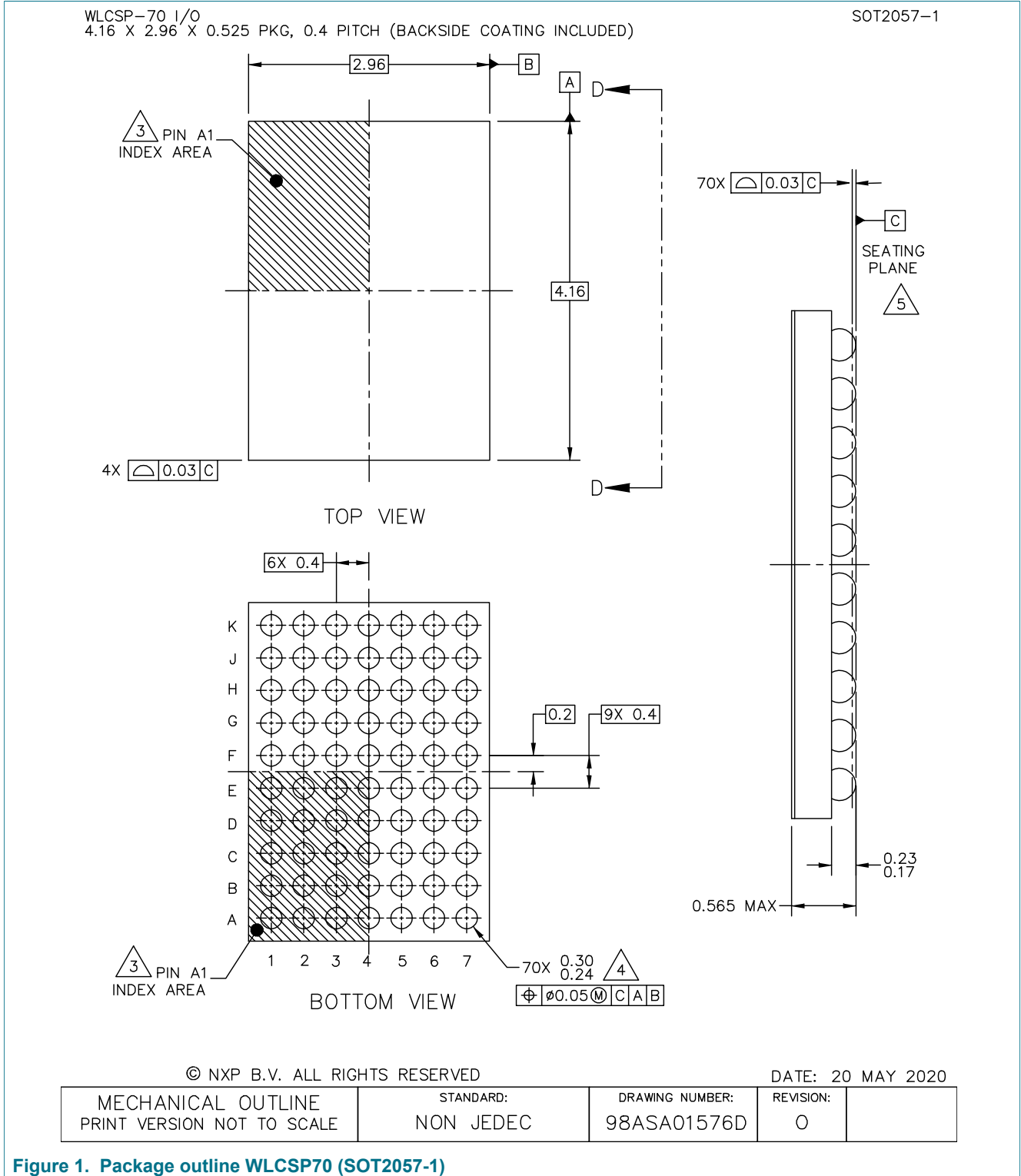
Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	4.13	4.16	4.19	mm
package width	2.93	2.96	2.99	mm
package height	-	0.525	0.565	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	70	-	



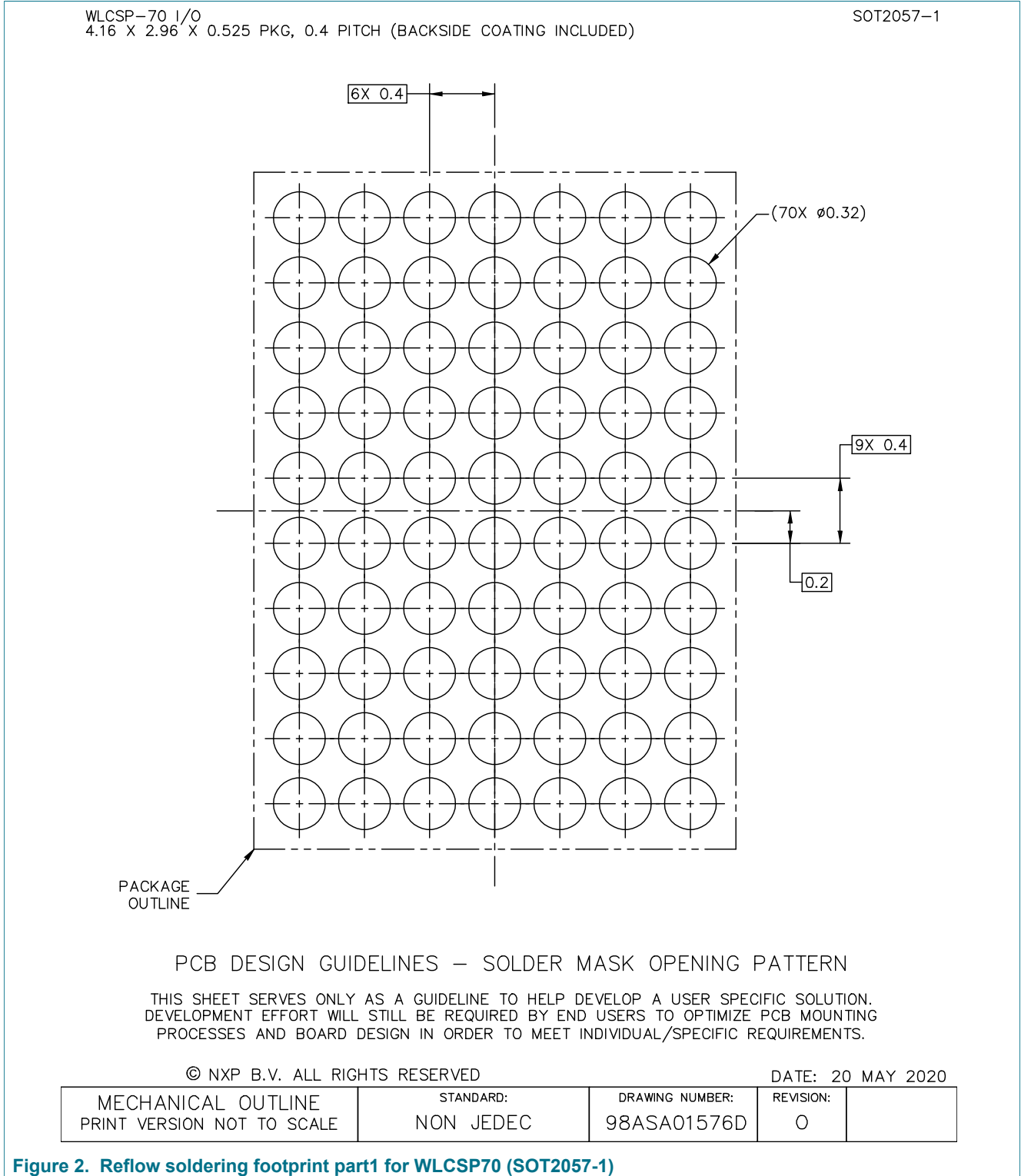
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2 Package outline



WLCSP70, wafer level chip scale package, 70 terminals, 0.4 mm pitch, 4.16 mm x 2.96 mm x 0.525 mm body (backside coating included)

3 Soldering



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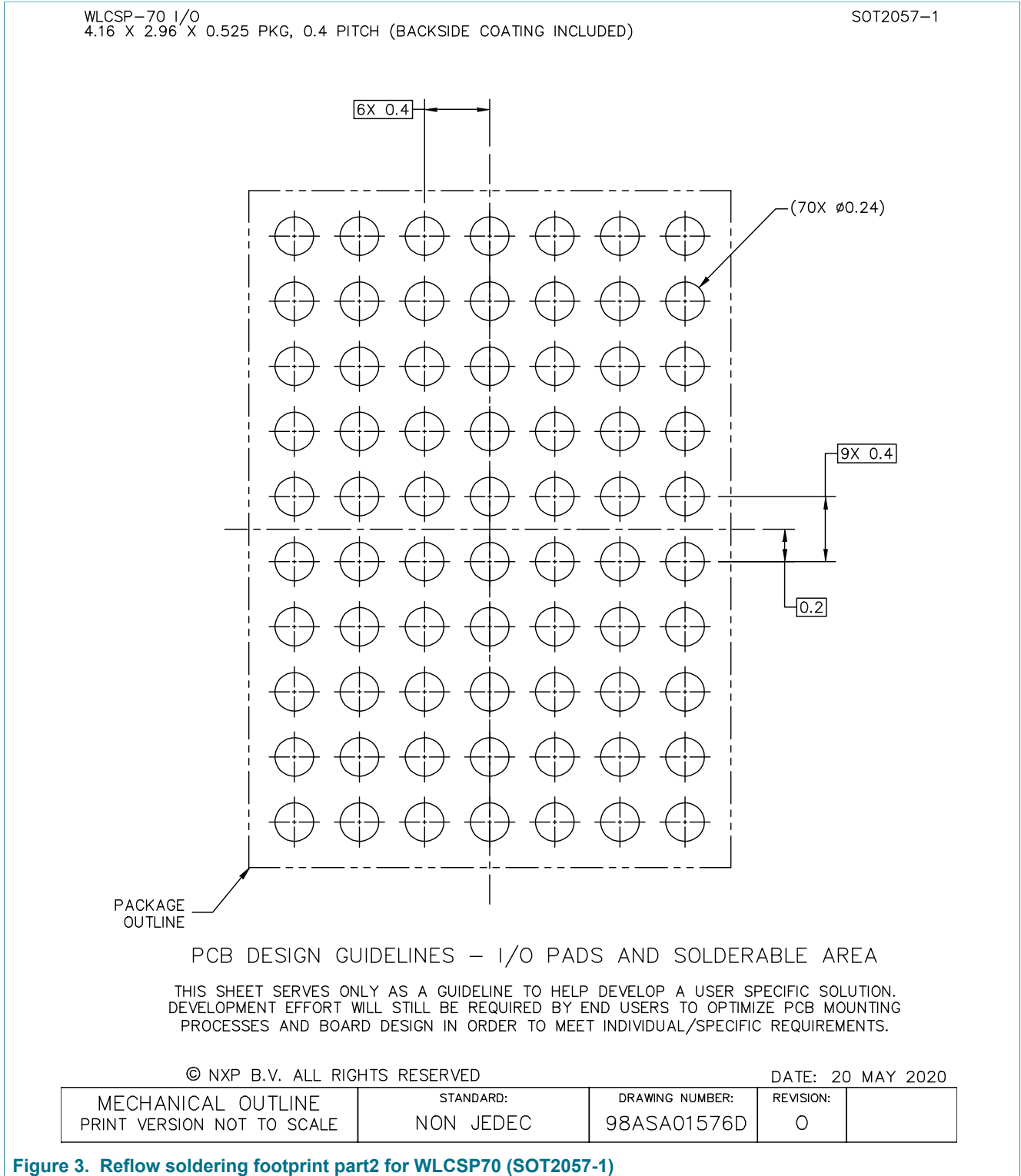


Figure 3. Reflow soldering footprint part2 for WLCSP70 (SOT2057-1)

WLCSP70, wafer level chip scale package, 70 terminals, 0.4 mm pitch, 4.16 mm x 2.96 mm x 0.525 mm body (backside coating included)

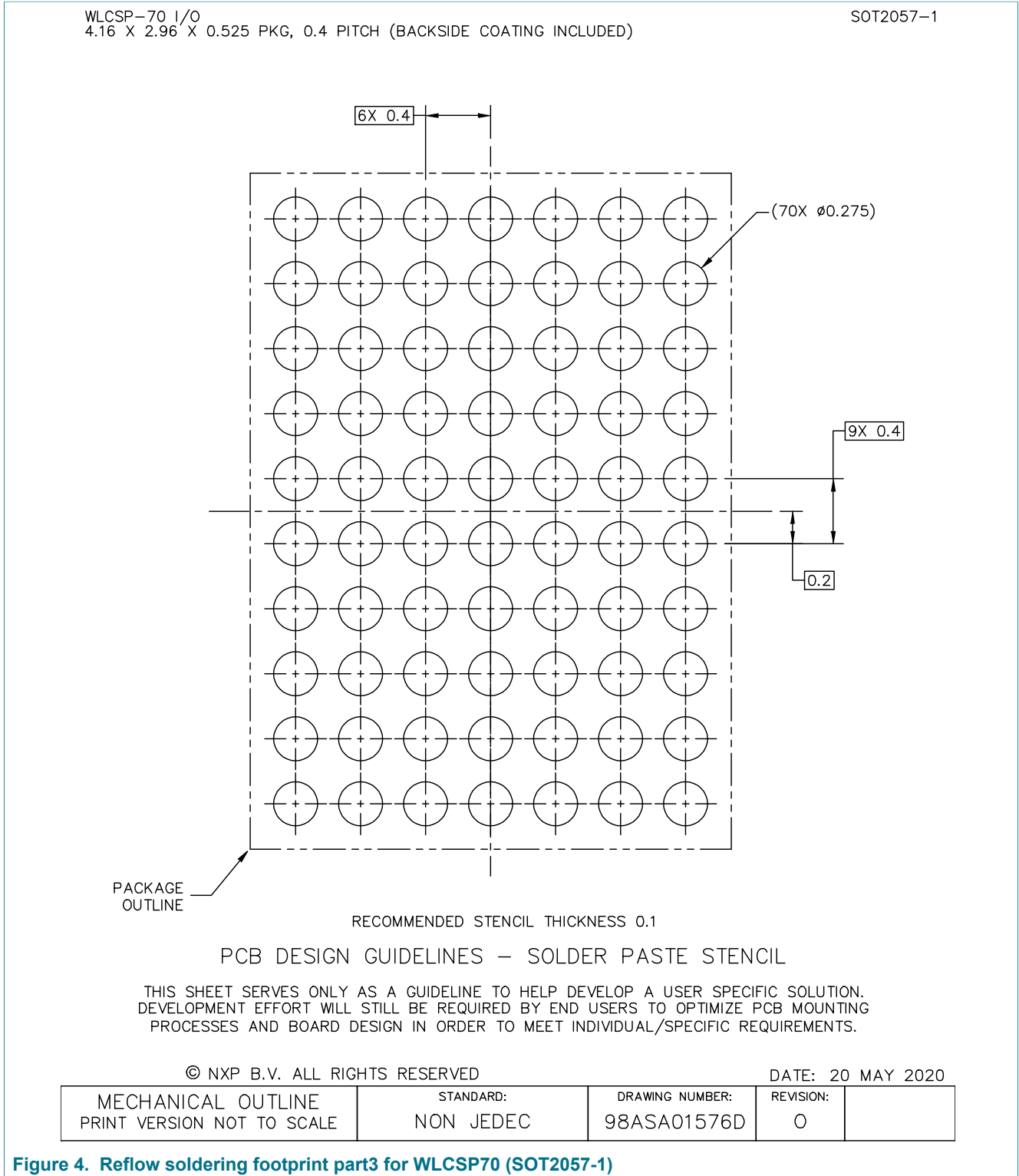


Figure 4. Reflow soldering footprint part3 for WLCSP70 (SOT2057-1)

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WLCSP-70 I/O
4.16 X 2.96 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT2057-1

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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DATE: 20 MAY 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01576D	REVISION: 0	
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Figure 5. Package outline note WLCSP70 (SOT2057-1)

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4 Legal information

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