

SOT2060-1

WLCSP49, wafer level chip scale package, 49 terminals, 0.35 mm pitch, 2.56 mm x 2.46 mm x 0.365 mm body (backside coating included)

7 May 2020

Package information

1 Package summary

| | |
|---------------------------------------|---------------------------------------|
| Terminal position code | B (bottom) |
| Package type descriptive code | WLCSP49 |
| Package type industry code | WLCSP49 |
| Package style descriptive code | WLCSP (wafer level chip-size package) |
| Mounting method type | S (surface mount) |
| Issue date | 20-04-2020 |
| Manufacturer package code | 98ASA01596D |

Table 1. Package summary

| Parameter | Min | Nom | Max | Unit |
|--------------------------------|------|-------|-------|------|
| package length | 2.53 | 2.56 | 2.59 | mm |
| package width | 2.43 | 2.46 | 2.49 | mm |
| seated height | - | 0.365 | 0.395 | mm |
| nominal pitch | - | 0.35 | - | mm |
| actual quantity of termination | - | 49 | - | |



WLCSP49, wafer level chip scale package, 49 terminals, 0.35 mm pitch, 2.56 mm x 2.46 mm x 0.365 mm body (backside coating included)

2 Package outline

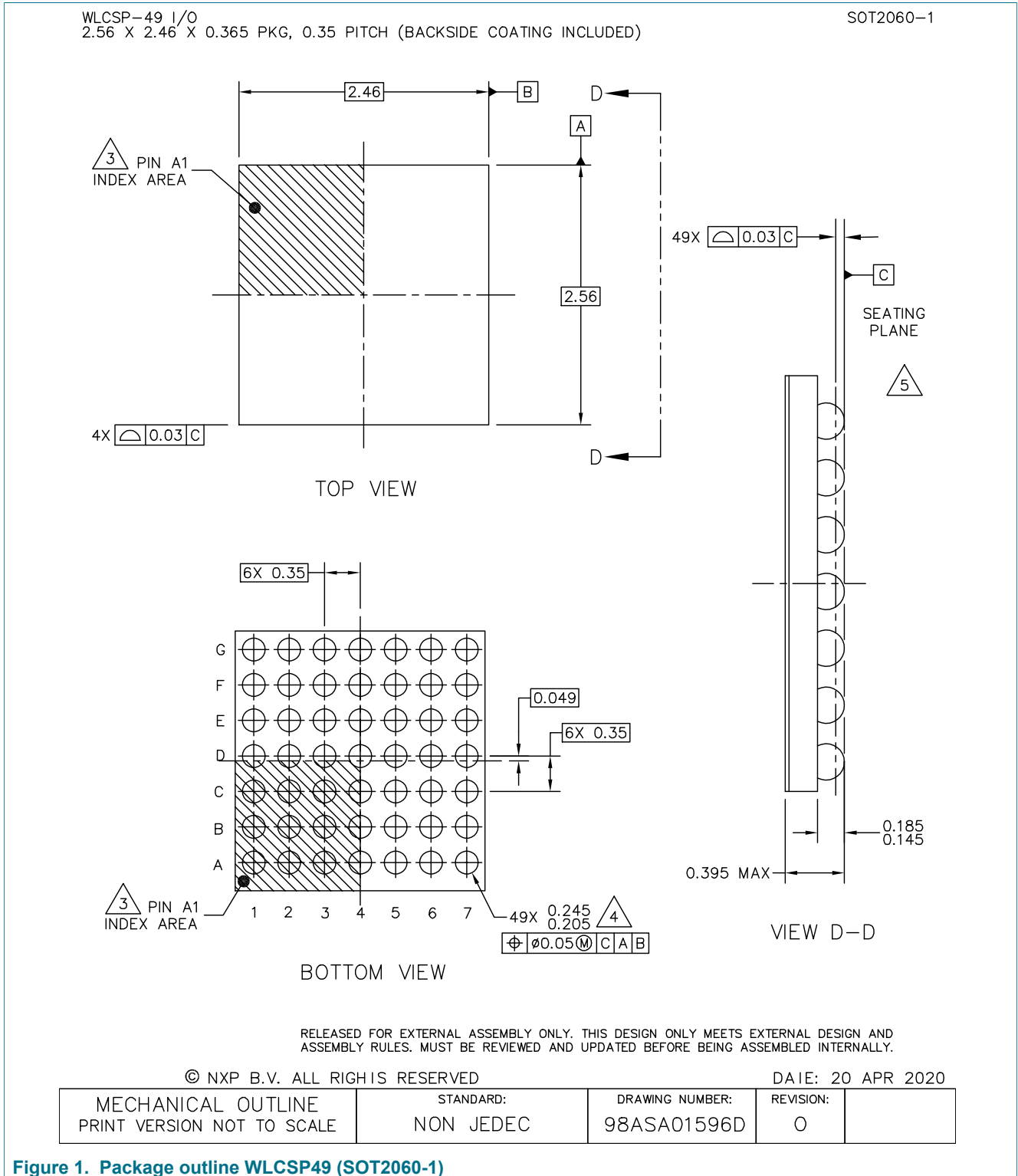


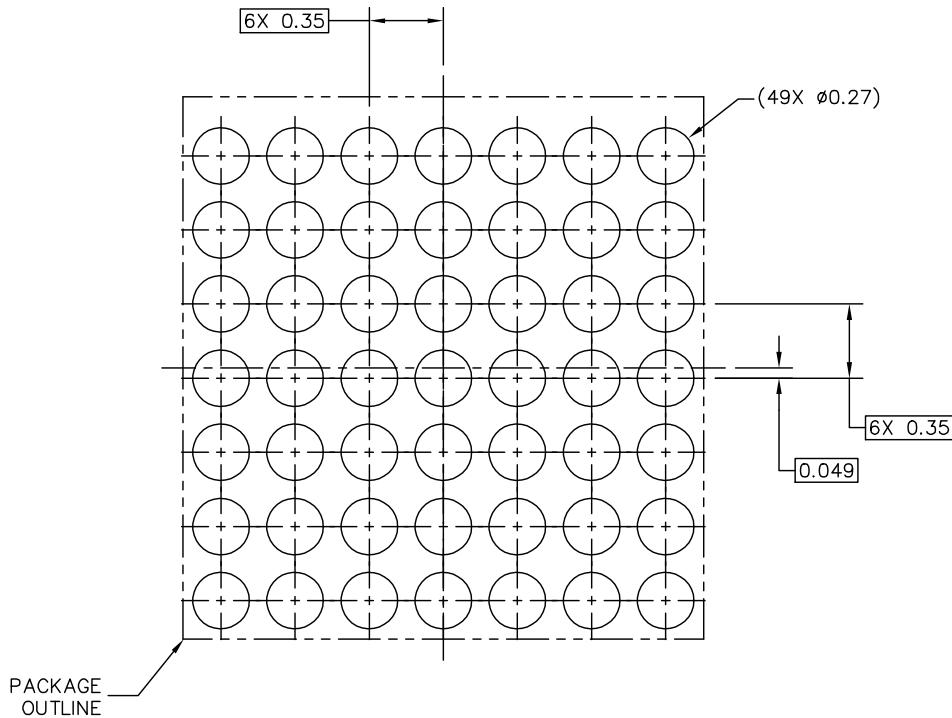
Figure 1. Package outline WLCSP49 (SOT2060-1)

WLCSP49, wafer level chip scale package, 49 terminals, 0.35 mm pitch, 2.56 mm x 2.46 mm x 0.365 mm body (backside coating included)

3 Soldering

WLCSP-49 I/O
2.56 X 2.46 X 0.365 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2060-1



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 20 APR 2020

| | | | | |
|--|------------------------|--------------------------------|----------------|--|
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: NON JEDEC | DRAWING NUMBER: 98ASA01596D | REVISION: 0 | |
|--|------------------------|--------------------------------|----------------|--|

Figure 2. Reflow soldering footprint part1 for WLCSP49 (SOT2060-1)

WLCSP49, wafer level chip scale package, 49 terminals, 0.35 mm pitch, 2.56 mm x 2.46 mm x 0.365 mm body (backside coating included)

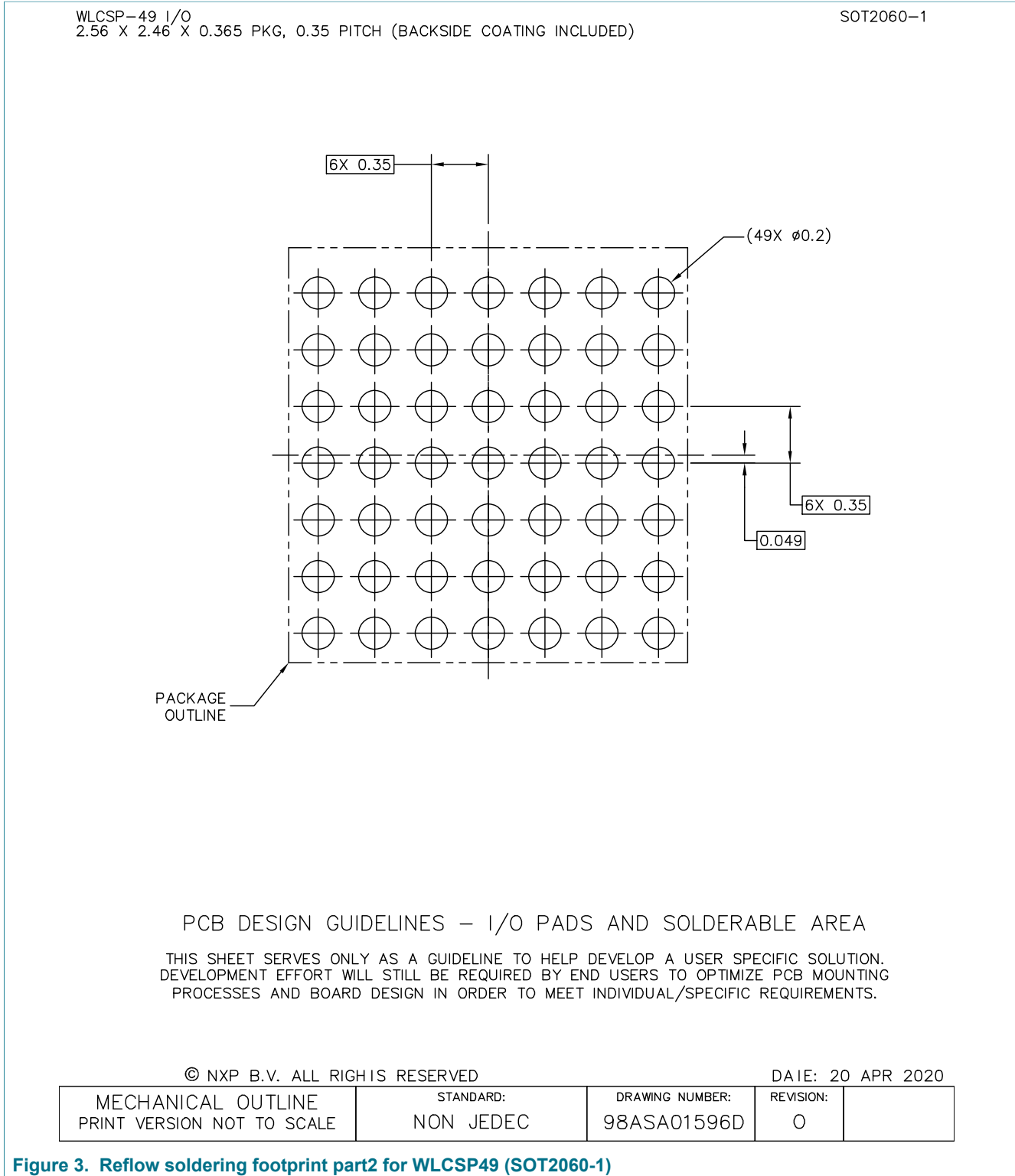
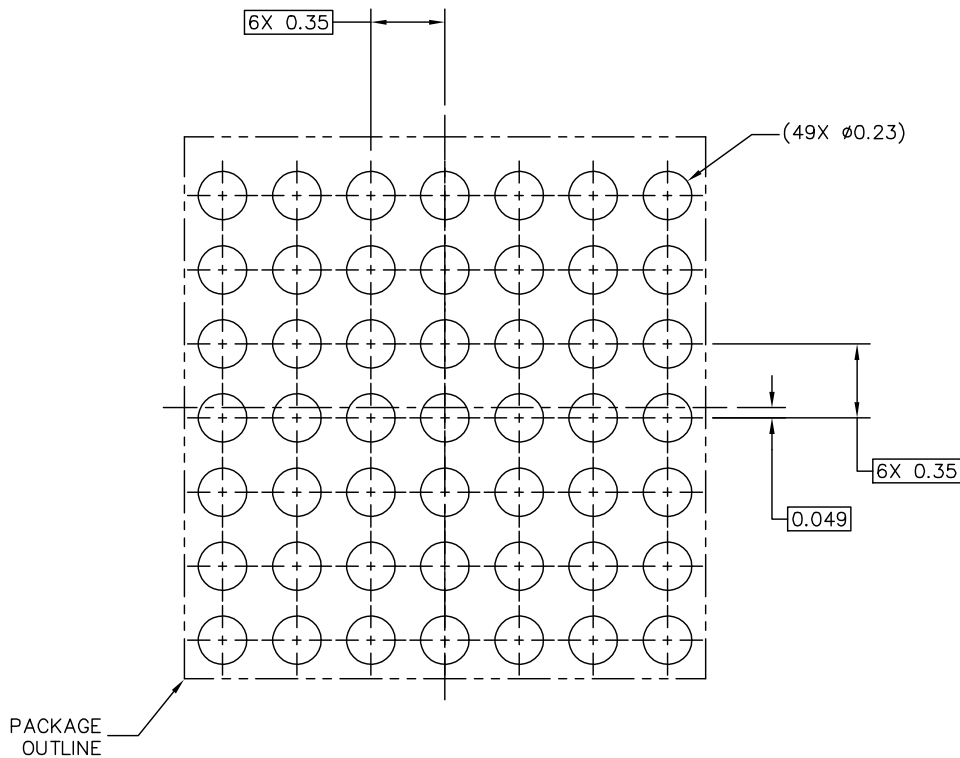


Figure 3. Reflow soldering footprint part2 for WLCSP49 (SOT2060-1)

WLCSP49, wafer level chip scale package, 49 terminals, 0.35 mm pitch, 2.56 mm x 2.46 mm x 0.365 mm body (backside coating included)

WLCSP-49 I/O
2.56 X 2.46 X 0.365 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2060-1



RECOMMENDED STENCIL THICKNESS 0.08

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DAIE: 20 APR 2020

| | | | | |
|--|------------------------|--------------------------------|----------------|--|
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: NON JEDEC | DRAWING NUMBER: 98ASA01596D | REVISION: 0 | |
|--|------------------------|--------------------------------|----------------|--|

Figure 4. Reflow soldering footprint part3 for WLCSP49 (SOT2060-1)

WLCSP49, wafer level chip scale package, 49 terminals, 0.35 mm pitch, 2.56 mm x 2.46 mm x 0.365 mm body (backside coating included)

WLCSP-49 I/O
2.56 X 2.46 X 0.365 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2060-1

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALL
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 20 APR 2020

| | | | | |
|--|------------------------|--------------------------------|----------------|--|
| MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE | STANDARD: NON JEDEC | DRAWING NUMBER: 98ASA01596D | REVISION: 0 | |
|--|------------------------|--------------------------------|----------------|--|

Figure 5. Package outline note WLCSP49 (SOT2060-1)

WLCSP49, wafer level chip scale package, 49 terminals, 0.35 mm pitch, 2.56 mm x 2.46 mm x 0.365 mm body (backside coating included)

4 Legal information

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

WLCSP49, wafer level chip scale package, 49 terminals, 0.35 mm pitch, 2.56 mm x 2.46 mm x 0.365 mm body (backside coating included)

Contents

- 1 Package summary1
- 2 Package outline2
- 3 Soldering3
- 4 Legal information7