

# SOT2060-1

**WLCSP49, wafer level chip scale package, 49 terminals, 0.35 mm pitch, 2.56 mm x 2.46 mm x 0.365 mm body (backside coating included)**

7 May 2020

Package information

## 1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP49
Package type industry code	WLCSP49
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	20-04-2020
Manufacturer package code	98ASA01596D

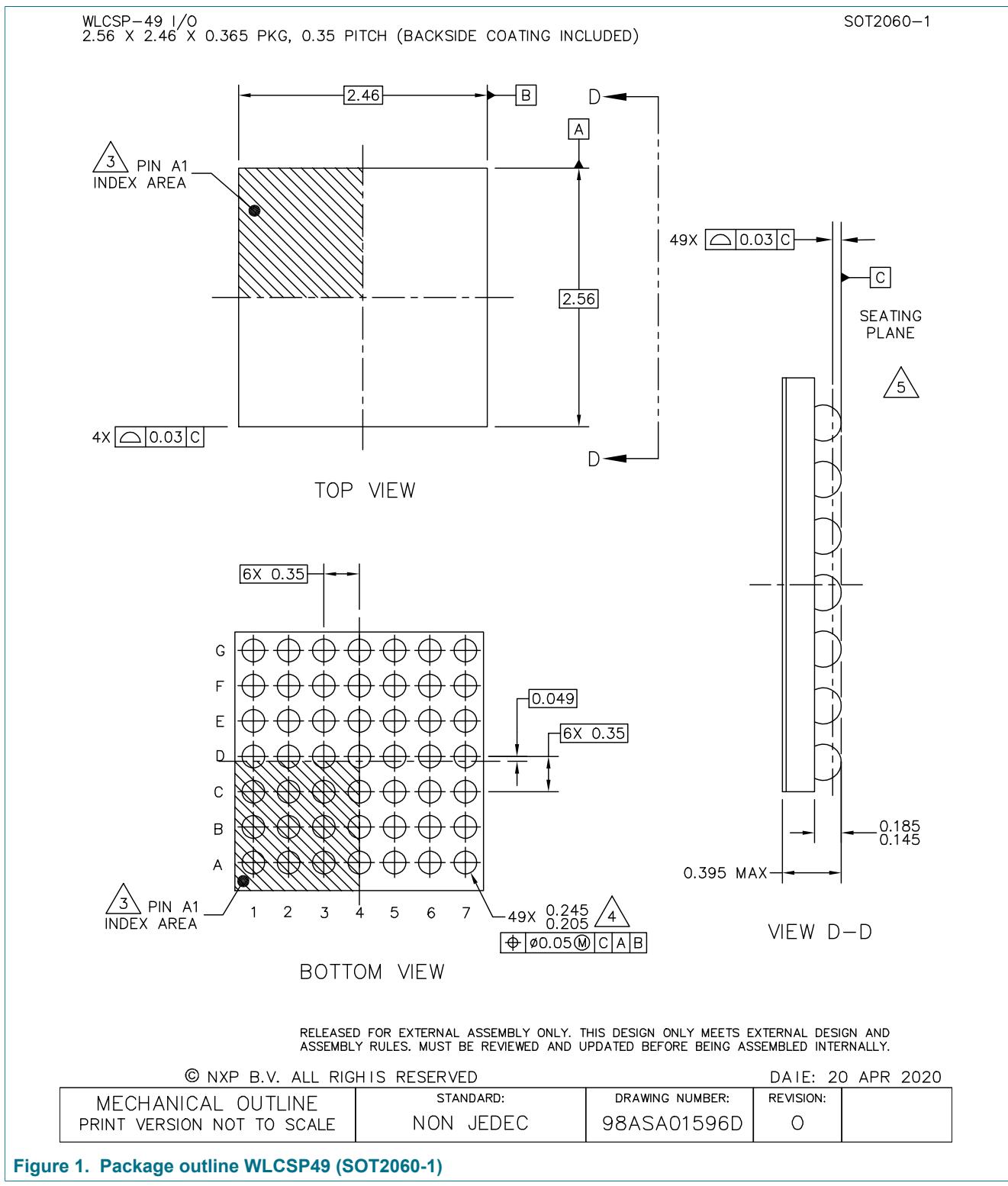
**Table 1. Package summary**

Parameter	Min	Nom	Max	Unit
package length	2.53	2.56	2.59	mm
package width	2.43	2.46	2.49	mm
seated height	-	0.365	0.395	mm
nominal pitch	-	0.35	-	mm
actual quantity of termination	-	49	-	



WLCSP49, wafer level chip scale package, 49 terminals, 0.35 mm pitch, 2.56 mm x 2.46 mm x 0.365 mm body (backside coating included)

## 2 Package outline

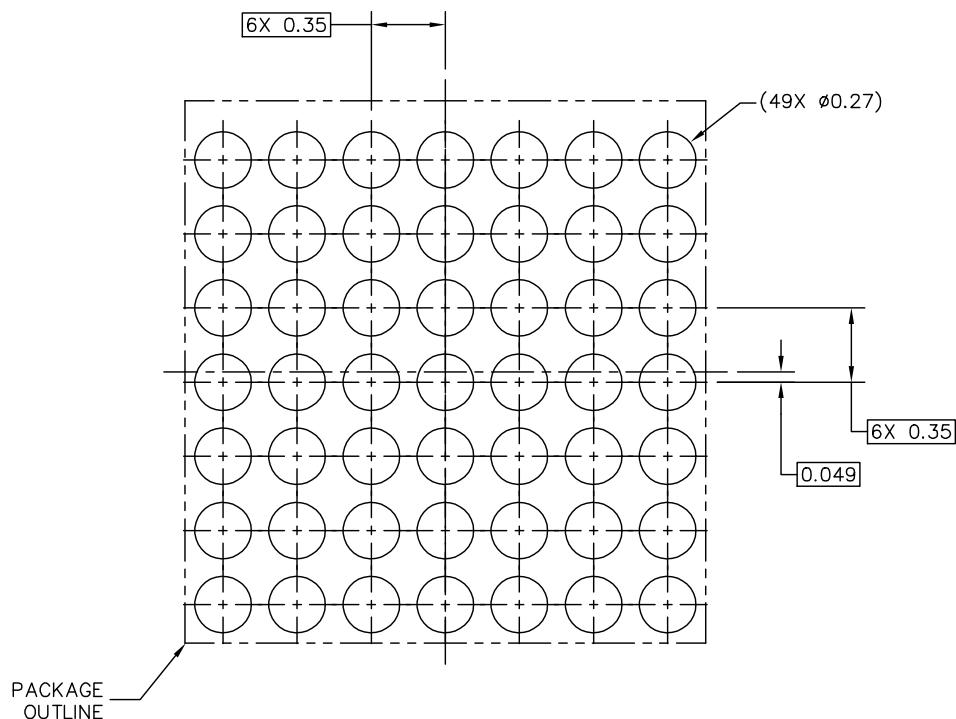


**WLCSP49, wafer level chip scale package, 49 terminals, 0.35 mm pitch, 2.56 mm x 2.46 mm x 0.365 mm body (backside coating included)**

### 3 Soldering

WLCSP-49 I/O  
2.56 X 2.46 X 0.365 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2060-1



#### PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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DATE: 20 APR 2020

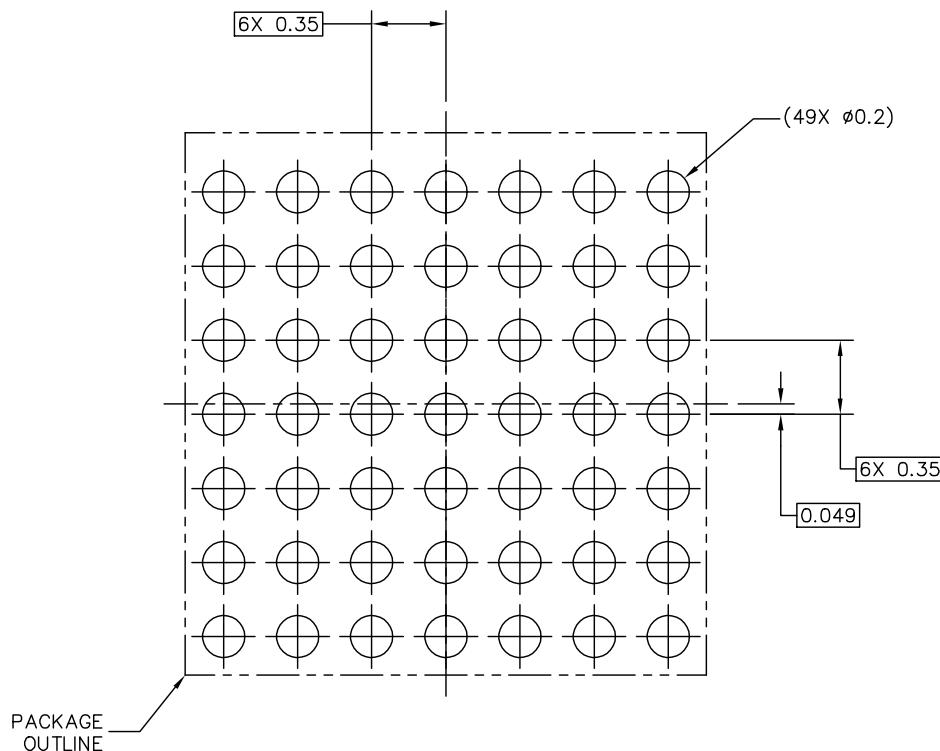
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01596D	REVISION: O	
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**Figure 2. Reflow soldering footprint part1 for WLCSP49 (SOT2060-1)**

**WLCSP49, wafer level chip scale package, 49 terminals, 0.35 mm pitch, 2.56 mm x 2.46 mm x 0.365 mm body (backside coating included)**

WLCSP-49 I/O  
2.56 X 2.46 X 0.365 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

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#### PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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MECHANICAL OUTLINE  
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STANDARD:  
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DRAWING NUMBER:  
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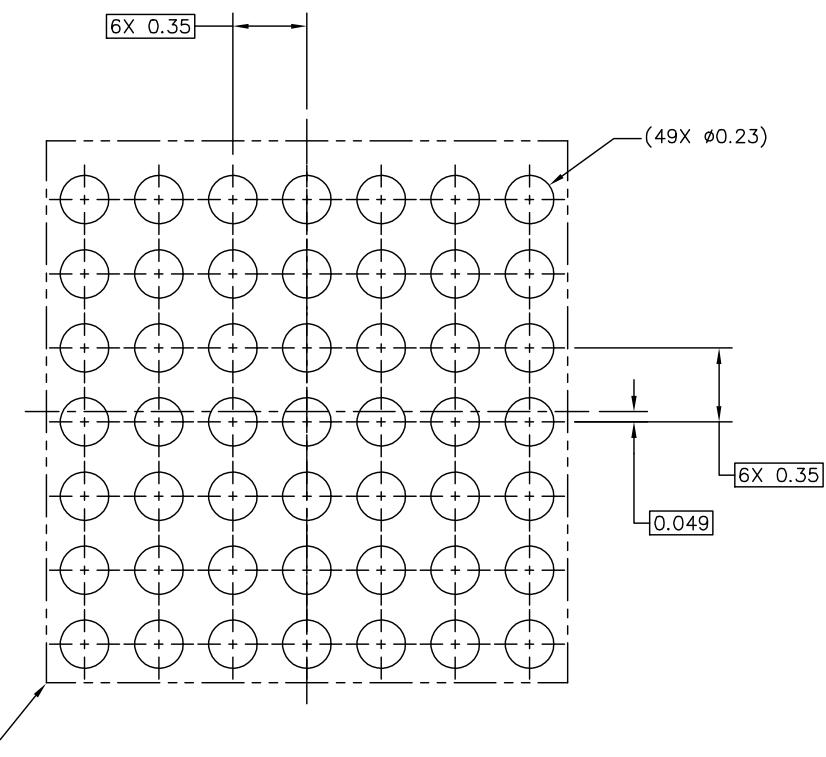
REVISION:  
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**Figure 3. Reflow soldering footprint part2 for WLCSP49 (SOT2060-1)**

**WLCSP49, wafer level chip scale package, 49 terminals, 0.35 mm pitch, 2.56 mm x 2.46 mm x 0.365 mm body (backside coating included)**

 WLCSP-49 I/O  
 2.56 X 2.46 X 0.365 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

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RECOMMENDED STENCIL THICKNESS 0.08

## PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 4. Reflow soldering footprint part3 for WLCSP49 (SOT2060-1)

**WLCSP49, wafer level chip scale package, 49 terminals, 0.35 mm pitch, 2.56 mm x 2.46 mm x 0.365 mm body (backside coating included)**WLCSP-49 I/O  
2.56 X 2.46 X 0.365 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2060-1

## NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALL
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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**Figure 5. Package outline note WLCSP49 (SOT2060-1)**

## 4 Legal information

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