

SOT2125-1

WLCSP79, wafer level chip scale package, 79 terminals, 0.35 mm pitch, 3.58 mm x 3.185 mm x 0.37 mm body (backside coating included)

15 April 2021

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP79
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	31-03-2021
Manufacturer package code	98ASA01585D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	3.55	3.58	3.61	mm
package width	3.155	3.185	3.215	mm
package height	-	0.37	0.4	mm
nominal pitch	-	0.35	-	mm
actual quantity of termination	-	79	-	



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2 Package outline

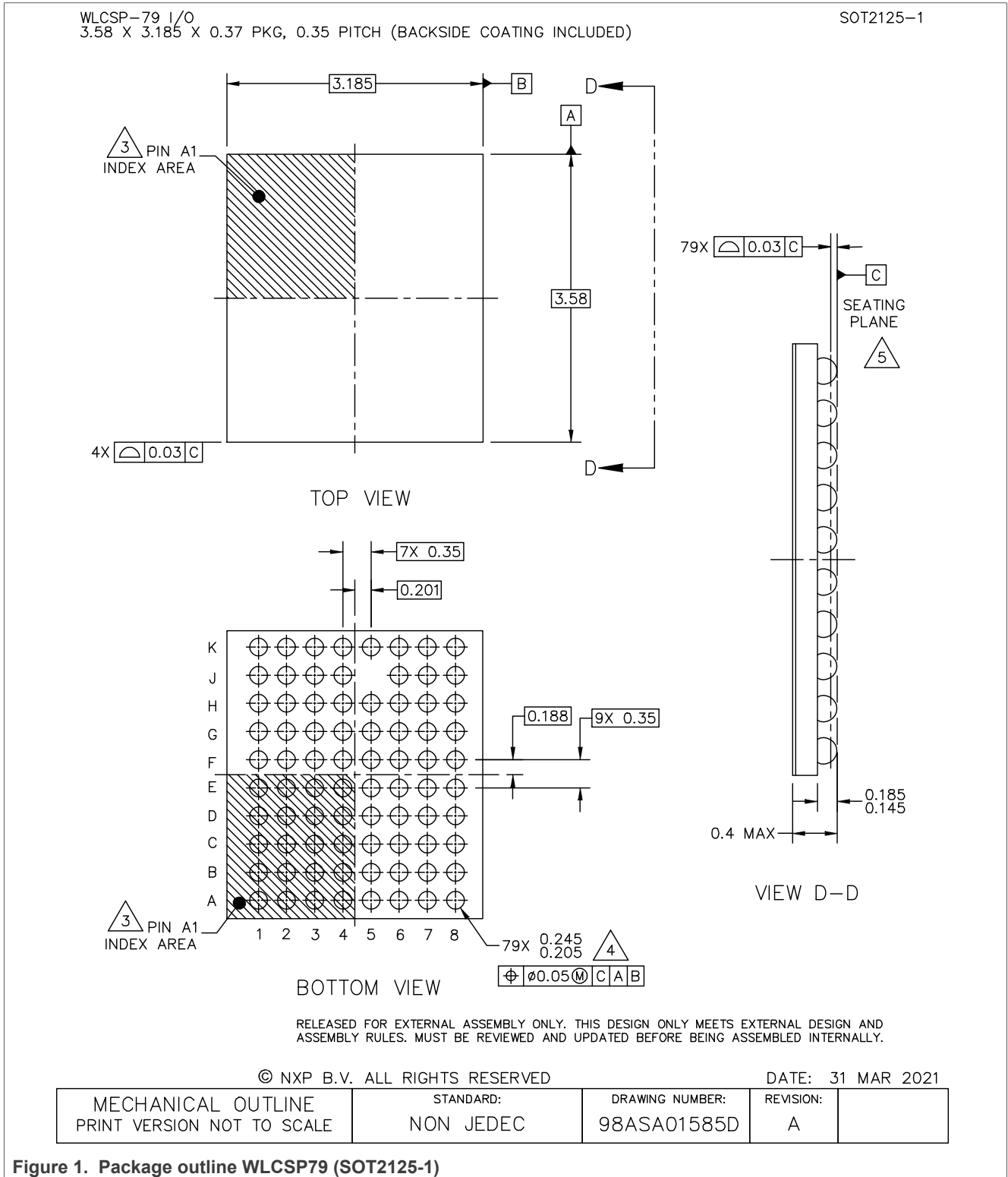
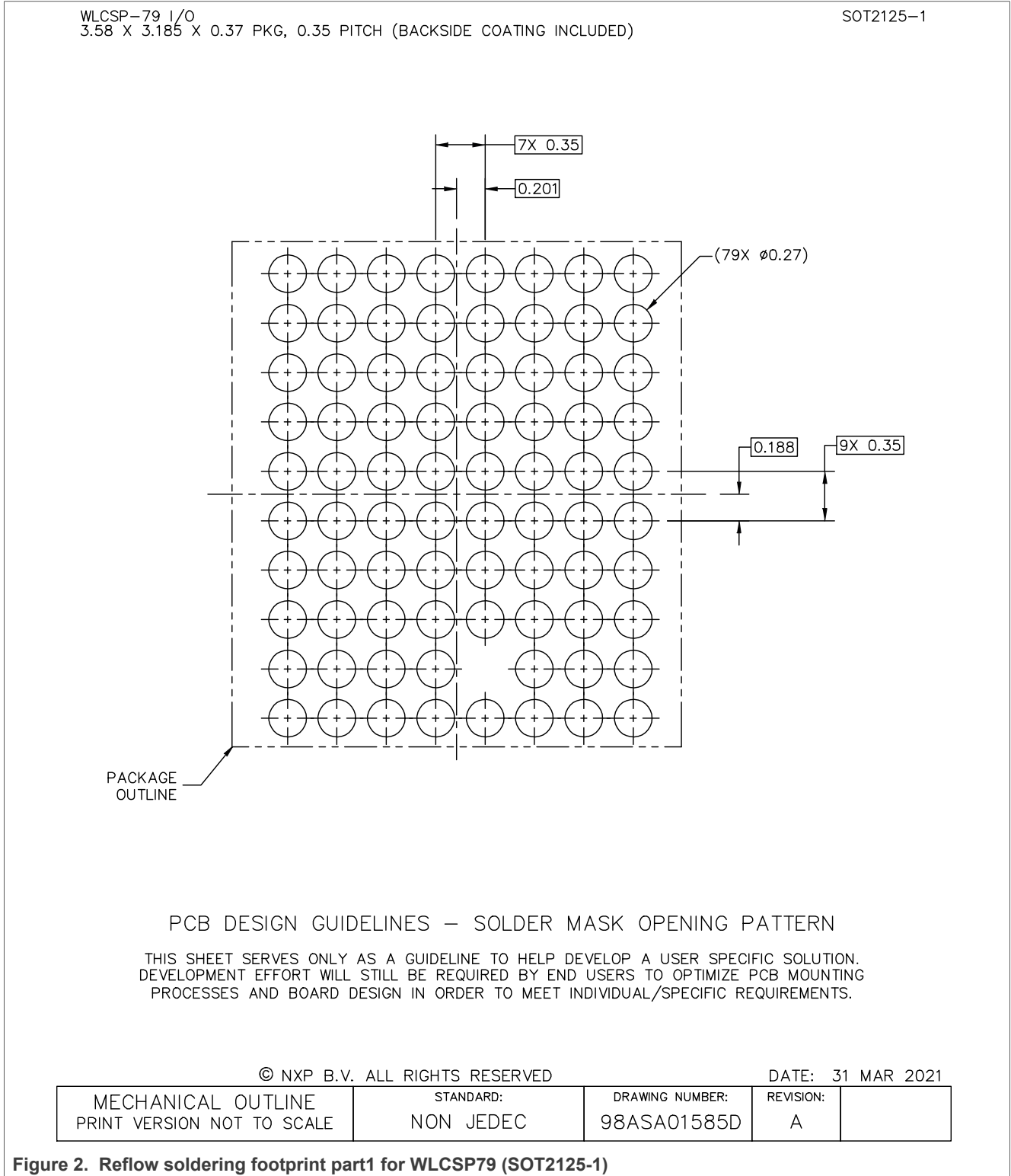


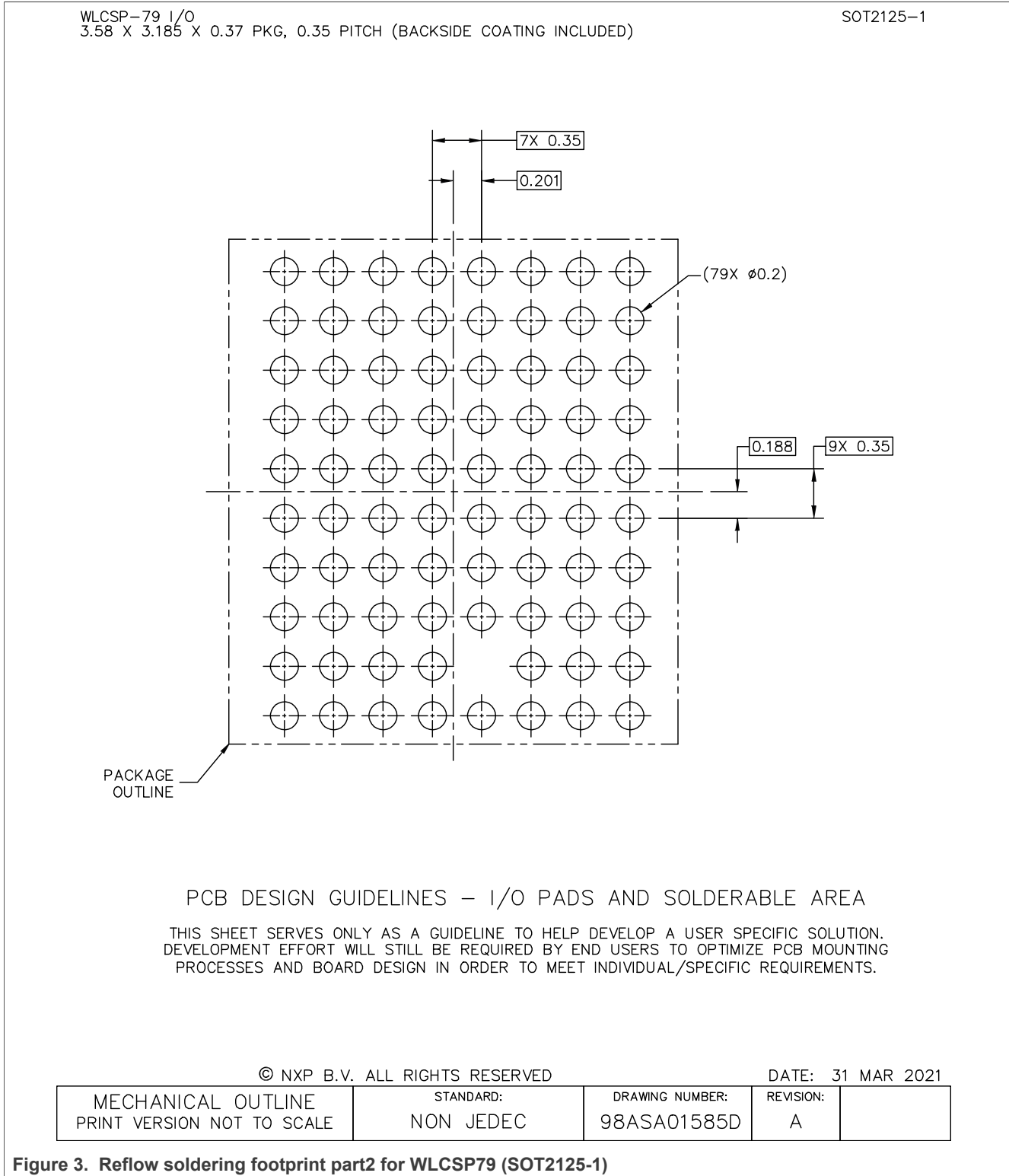
Figure 1. Package outline WLCSP79 (SOT2125-1)

WLCSP79, wafer level chip scale package, 79 terminals, 0.35 mm pitch, 3.58 mm x 3.185 mm x 0.37 mm body (backside coating included)

3 Soldering



WLCSP79, wafer level chip scale package, 79 terminals, 0.35 mm pitch, 3.58 mm x 3.185 mm x 0.37 mm body (backside coating included)



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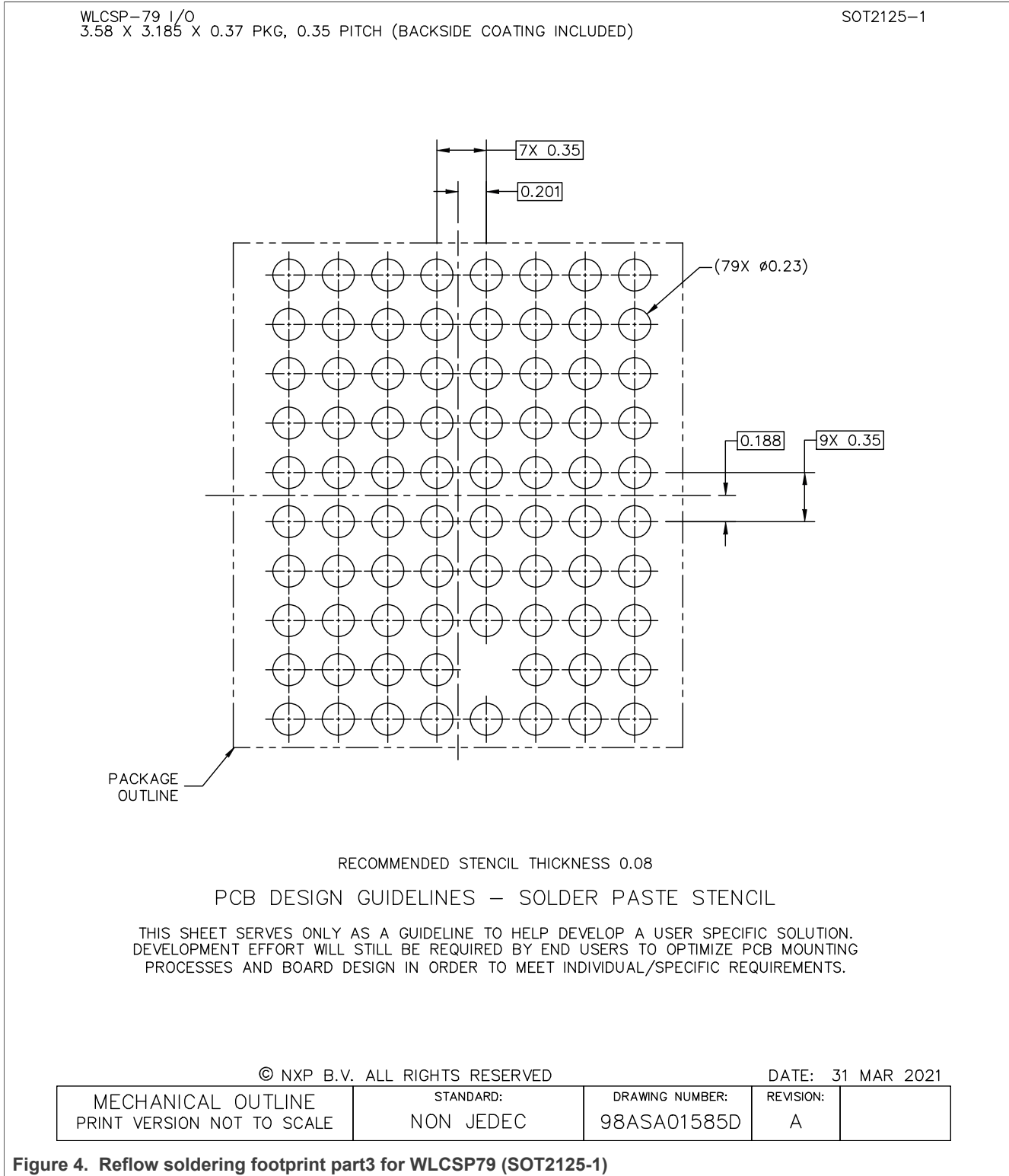


Figure 4. Reflow soldering footprint part3 for WLCSP79 (SOT2125-1)

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WLCSP-79 I/O
3.58 X 3.185 X 0.37 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2125-1

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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DATE: 31 MAR 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01585D	REVISION: A	
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Figure 5. Package outline note WLCSP79 (SOT2125-1)

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4 Legal information

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