

SOT2126-1

WLCSP140, wafer level chip-size package; 140 terminals; 0.3 mm pitch; 4.385 mm x 4.96 mm x 0.455 mm body

5 May 2022

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP140
Package style descriptive code	WLCSP (wafer level chip-size package)
Package body material type	P (plastic)
Mounting method type	S (surface mount)
Issue date	13-01-2022
Manufacturer package code	98ASA01734D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	4.96	-	mm
package width	-	4.385	-	mm
seated height	-	0.455	0.485	mm
nominal pitch	-	0.3	-	mm
actual quantity of termination	-	140	-	



WLCSP140, wafer level chip-size package; 140 terminals; 0.3 mm pitch; 4.385 mm x 4.96 mm x 0.455 mm body

2 Package outline

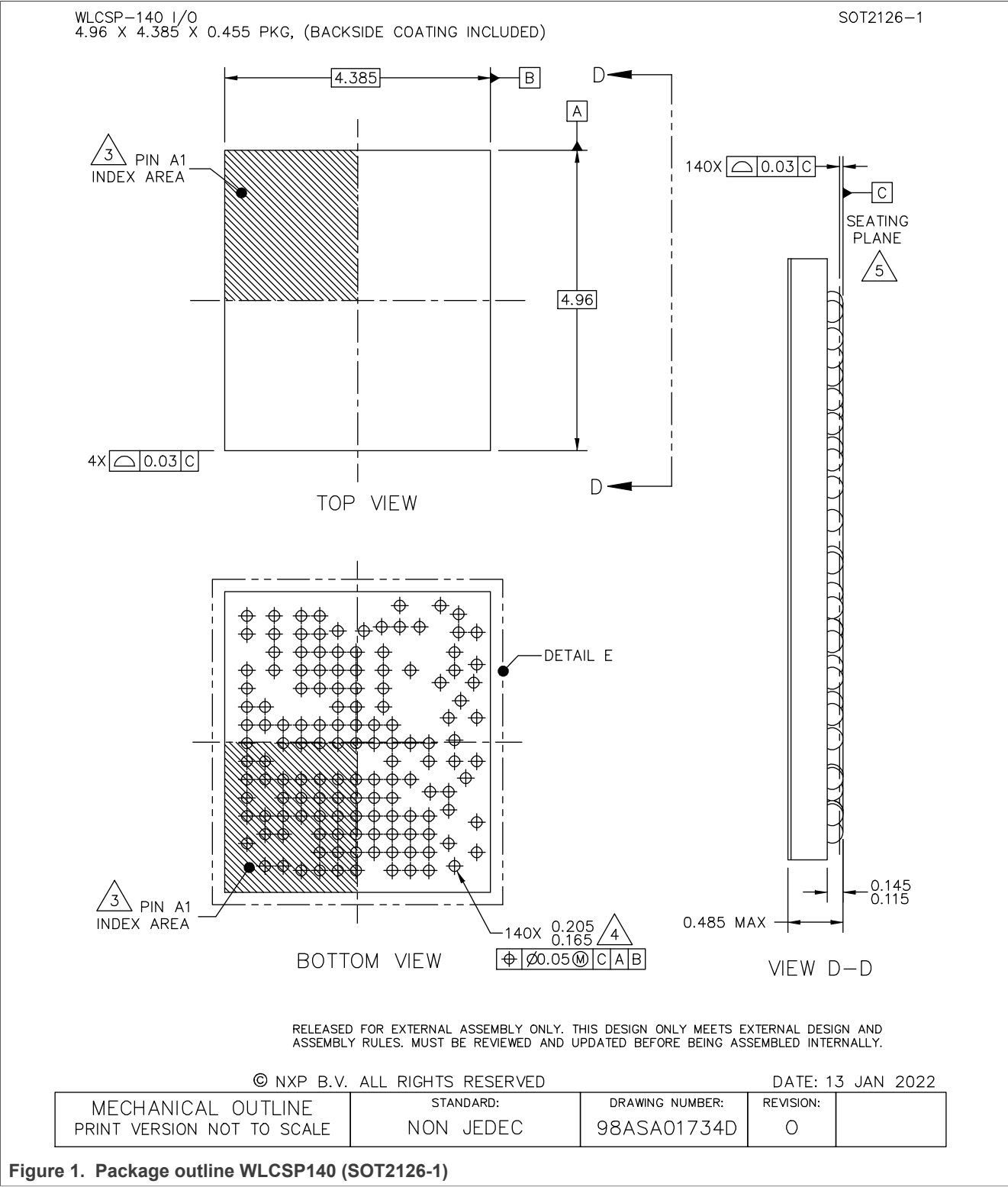
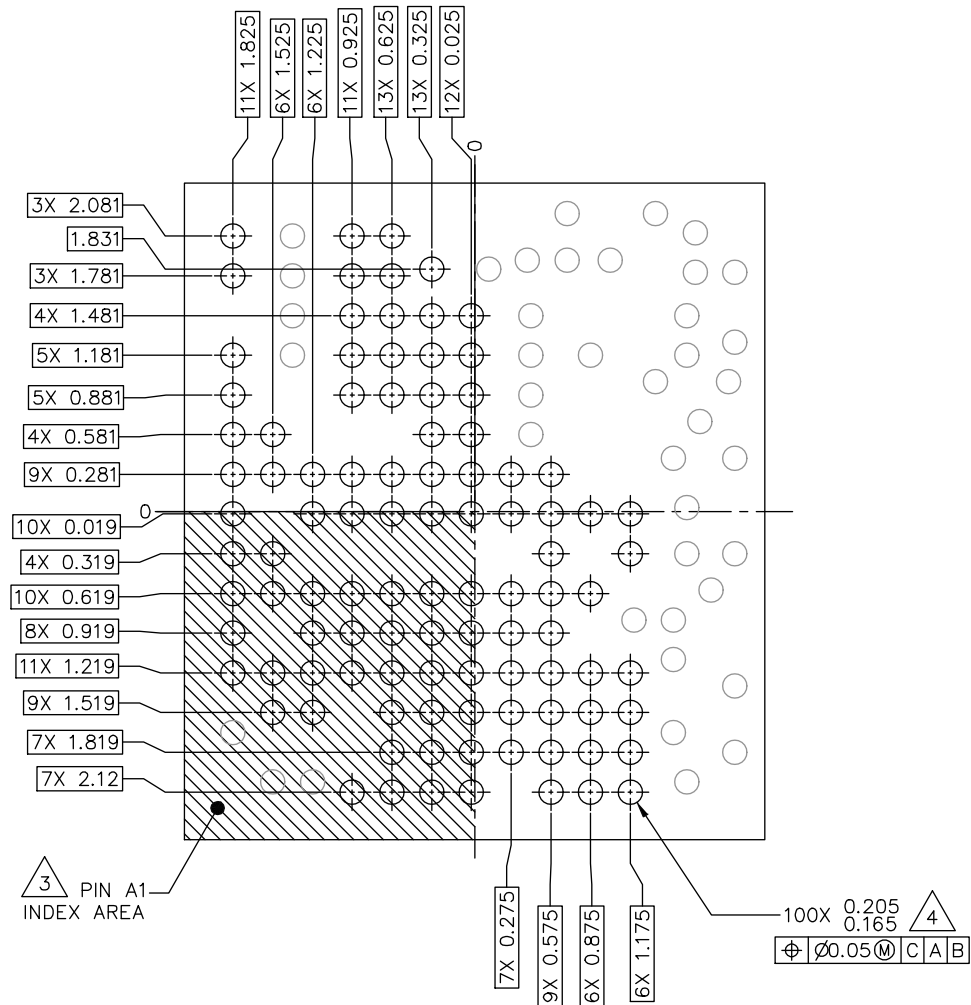


Figure 1. Package outline WLCSP140 (SOT2126-1)

WLCSP140, wafer level chip-size package; 140 terminals; 0.3 mm pitch; 4.385 mm x 4.96 mm x 0.455 mm body

WLCSP-140 I/O
4.96 X 4.385 X 0.455 PKG, (BACKSIDE COATING INCLUDED)

SOT2126-1



DETAIL E (I)
(ARRAY BUMPS (100X))

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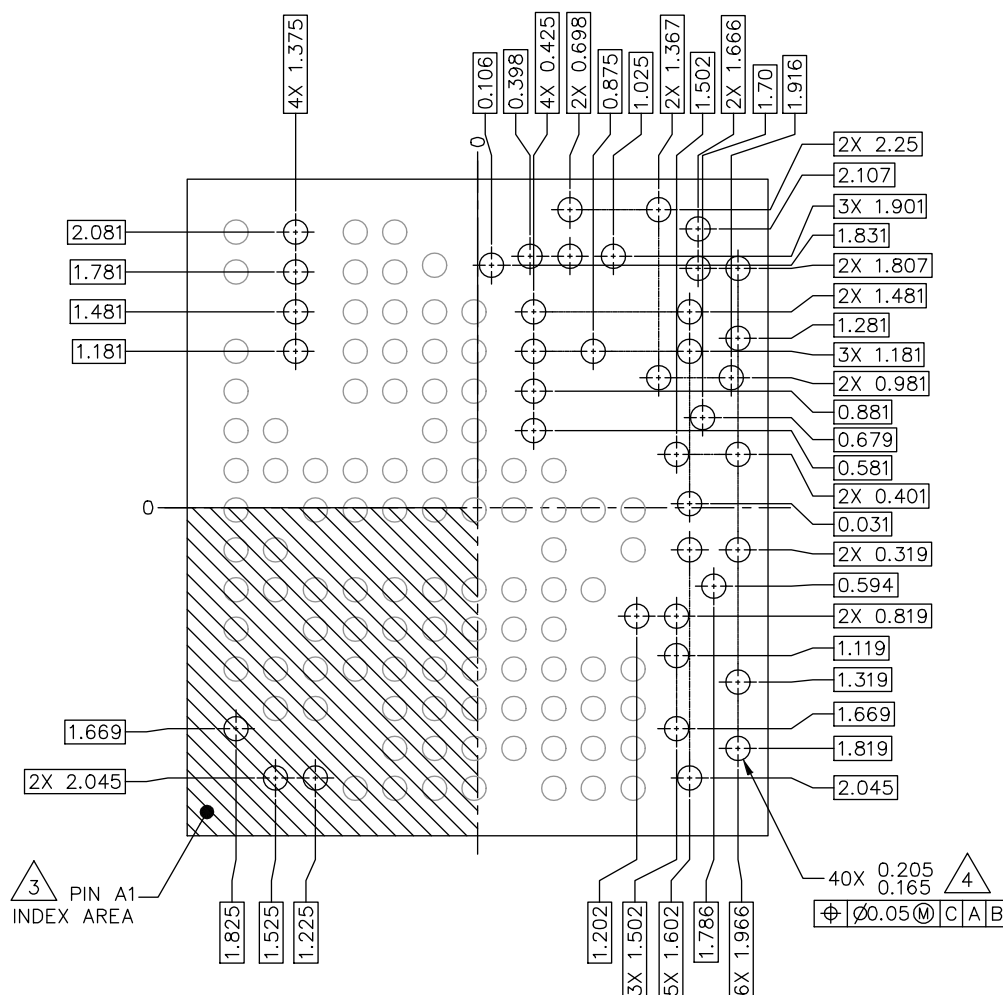
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01734D	REVISION: O	
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Figure 2. Package outline detail E (I) of WLCSP140 (SOT2126-1)

WLCSP140, wafer level chip-size package; 140 terminals; 0.3 mm pitch; 4.385 mm x 4.96 mm x 0.455 mm body

WLCSP-140 I/O
4.96 X 4.385 X 0.455 PKG, (BACKSIDE COATING INCLUDED)

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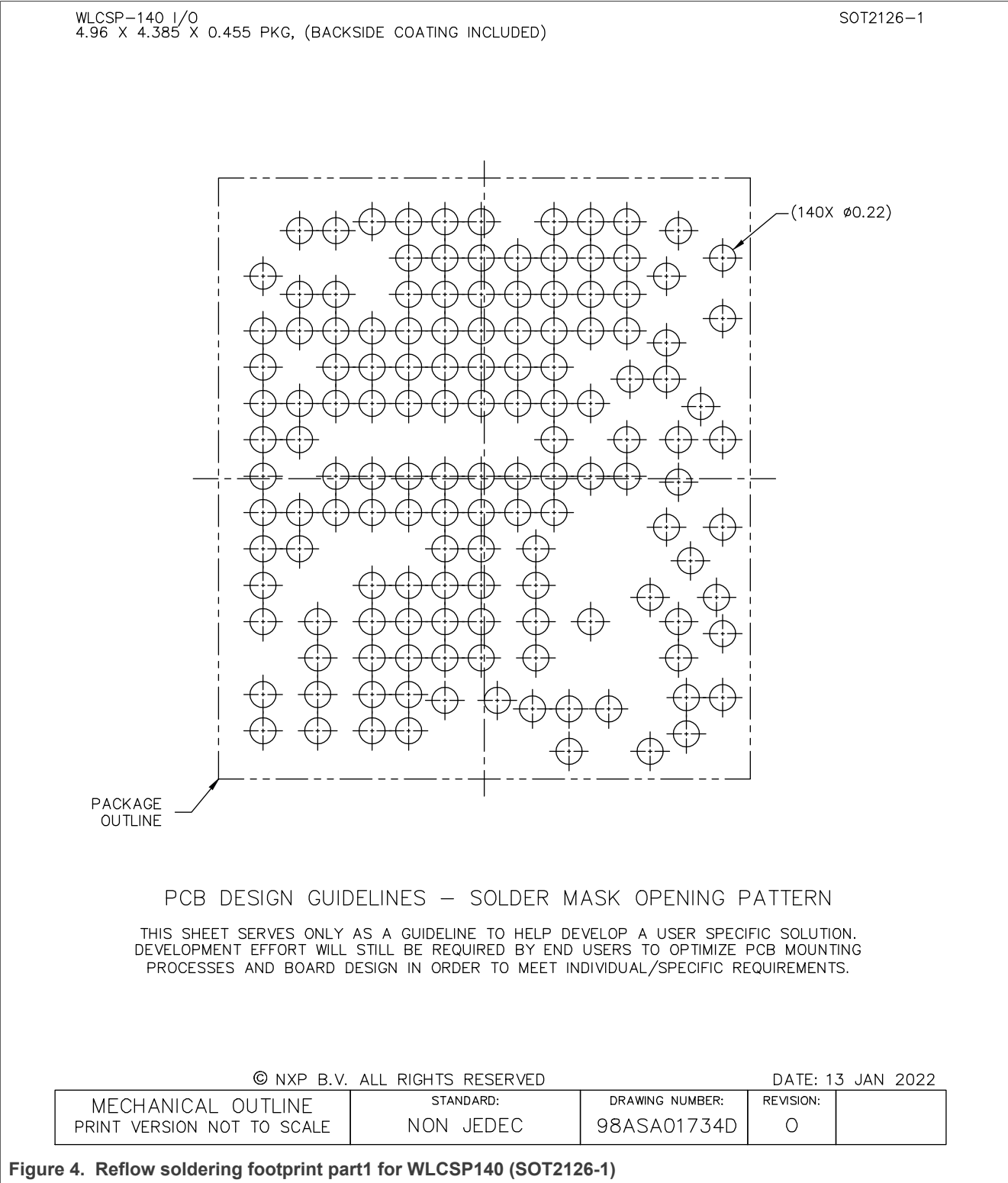
DETAIL E (II)
(NON-ARRAY BUMPS (40X))

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Figure 3. Package outline detail E (II) of WLCSP140 (SOT2126-1)

WLCSP140, wafer level chip-size package; 140 terminals; 0.3 mm pitch; 4.385 mm x 4.96 mm x 0.455 mm body

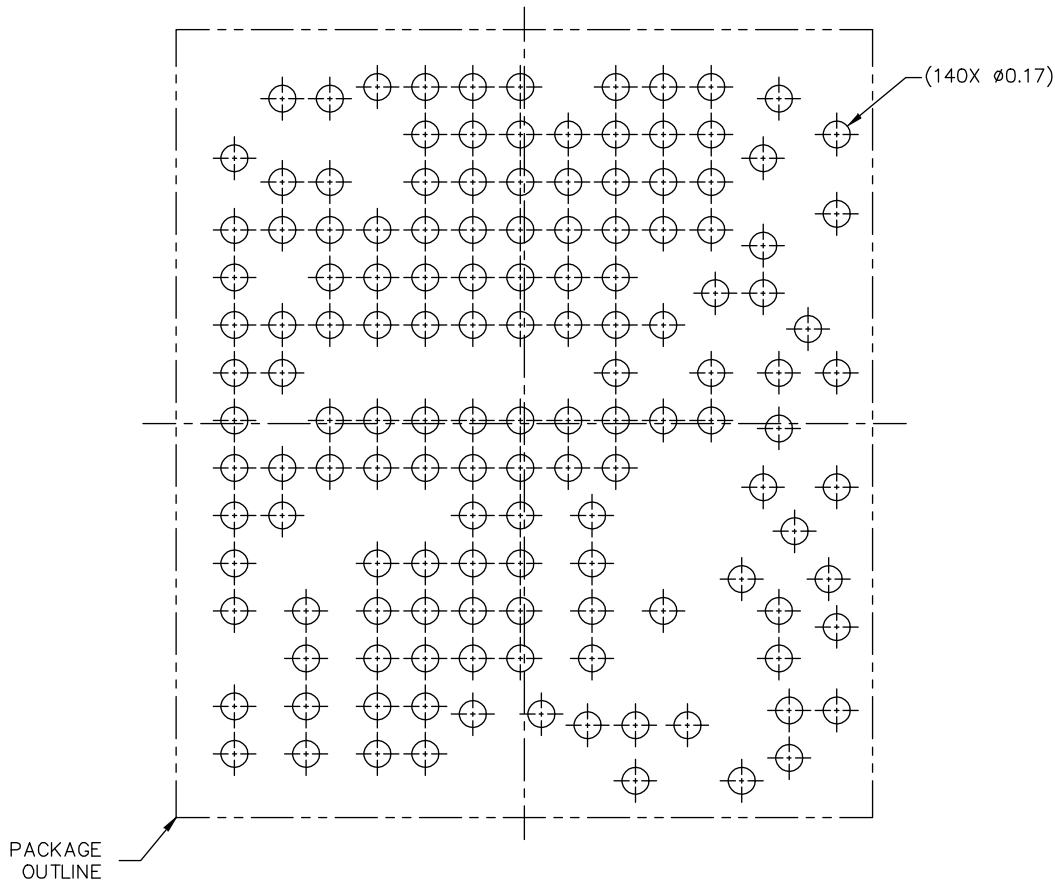
3 Soldering



WLCSP140, wafer level chip-size package; 140 terminals; 0.3 mm pitch; 4.385 mm x 4.96 mm x 0.455 mm
body

WLCSP-140 I/O
4.96 X 4.385 X 0.455 PKG, (BACKSIDE COATING INCLUDED)

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PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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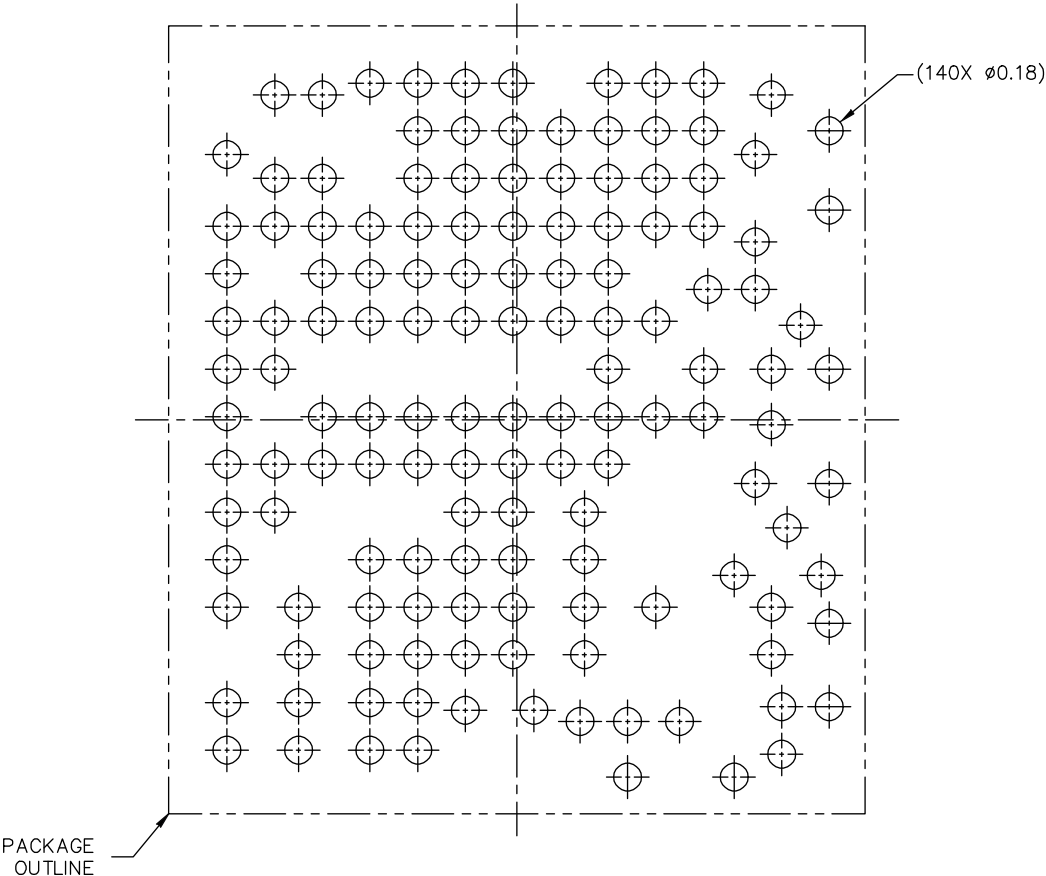
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Figure 5. Reflow soldering footprint part2 for WLCSP140 (SOT2126-1)

WLCSP140, wafer level chip-size package; 140 terminals; 0.3 mm pitch; 4.385 mm x 4.96 mm x 0.455 mm body

WLCSP-140 I/O
4.96 X 4.385 X 0.455 PKG, (BACKSIDE COATING INCLUDED)

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RECOMMENDED STENCIL THICKNESS 0.08

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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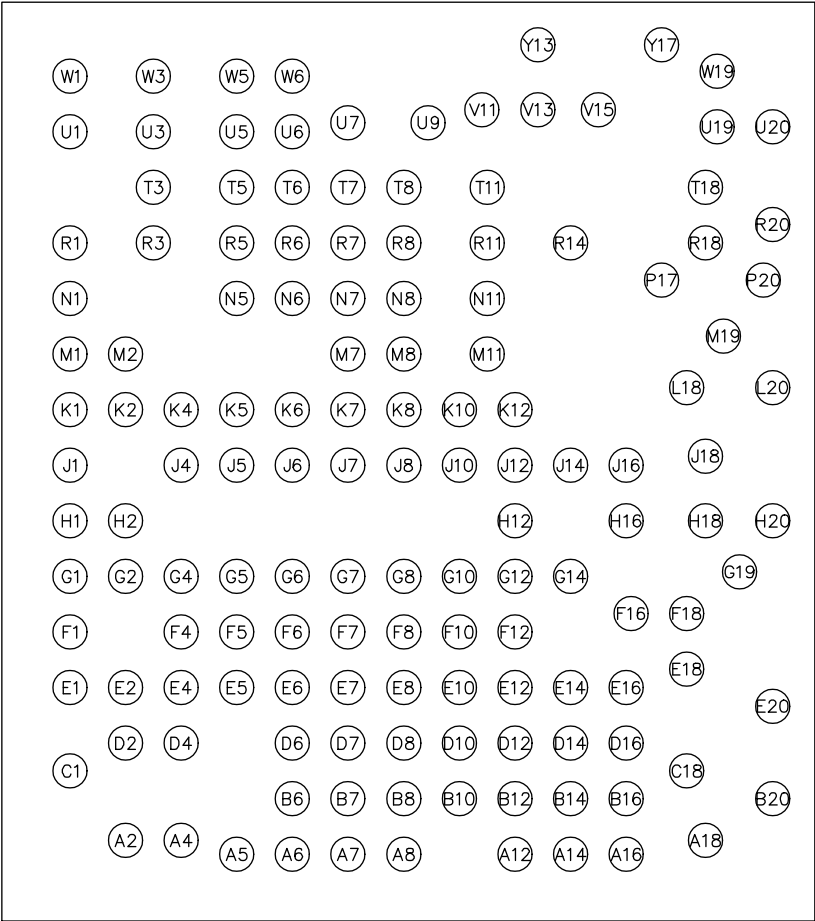
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Figure 6. Reflow soldering footprint part3 for WLCSP140 (SOT2126-1)

WLCSP140, wafer level chip-size package; 140 terminals; 0.3 mm pitch; 4.385 mm x 4.96 mm x 0.455 mm body

WLCSP-140 I/O
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PIN NUMBERS
(VIEWED FROM BOTTOM, SAME AS DETAIL E)

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Figure 7. Reflow soldering footprint part4 for WLCSP140 (SOT2126-1)

WLCSP140, wafer level chip-size package; 140 terminals; 0.3 mm pitch; 4.385 mm x 4.96 mm x 0.455 mm body

WLCSP-140 I/O
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NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
- 4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
- 5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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Figure 8. Package outline note WLCSP140 (SOT2126-1)

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Contents

1	Package summary	1
2	Package outline	2
3	Soldering	5
4	Legal information	10