

# SOT2168-1

HWFLGA60, thermal enhanced very very thin finepitch land grid array package, 0.4 mm pitch, 9.05 mm x 4.05 mm x 0.63 mm body

15 November 2022

Package information

## 1 Package summary

<b>Terminal position code</b>	B (bottom)
<b>Package type descriptive code</b>	HWFLGA60
<b>Package style descriptive code</b>	HWFLGA (thermal enhanced land grid array package)
<b>Package body material type</b>	P (plastic)
<b>Mounting method type</b>	S (surface mount)
<b>Issue date</b>	31-10-2022
<b>Manufacturer package code</b>	98ASA01867D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	9.05	-	mm
package width	-	4.05	-	mm
seated height	-	0.63	0.687	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	60	-	



HWFLGA60, thermal enhanced very very thin finepitch land grid array package, 0.4 mm pitch, 9.05 mm x 4.05 mm x 0.63 mm body

2 Package outline

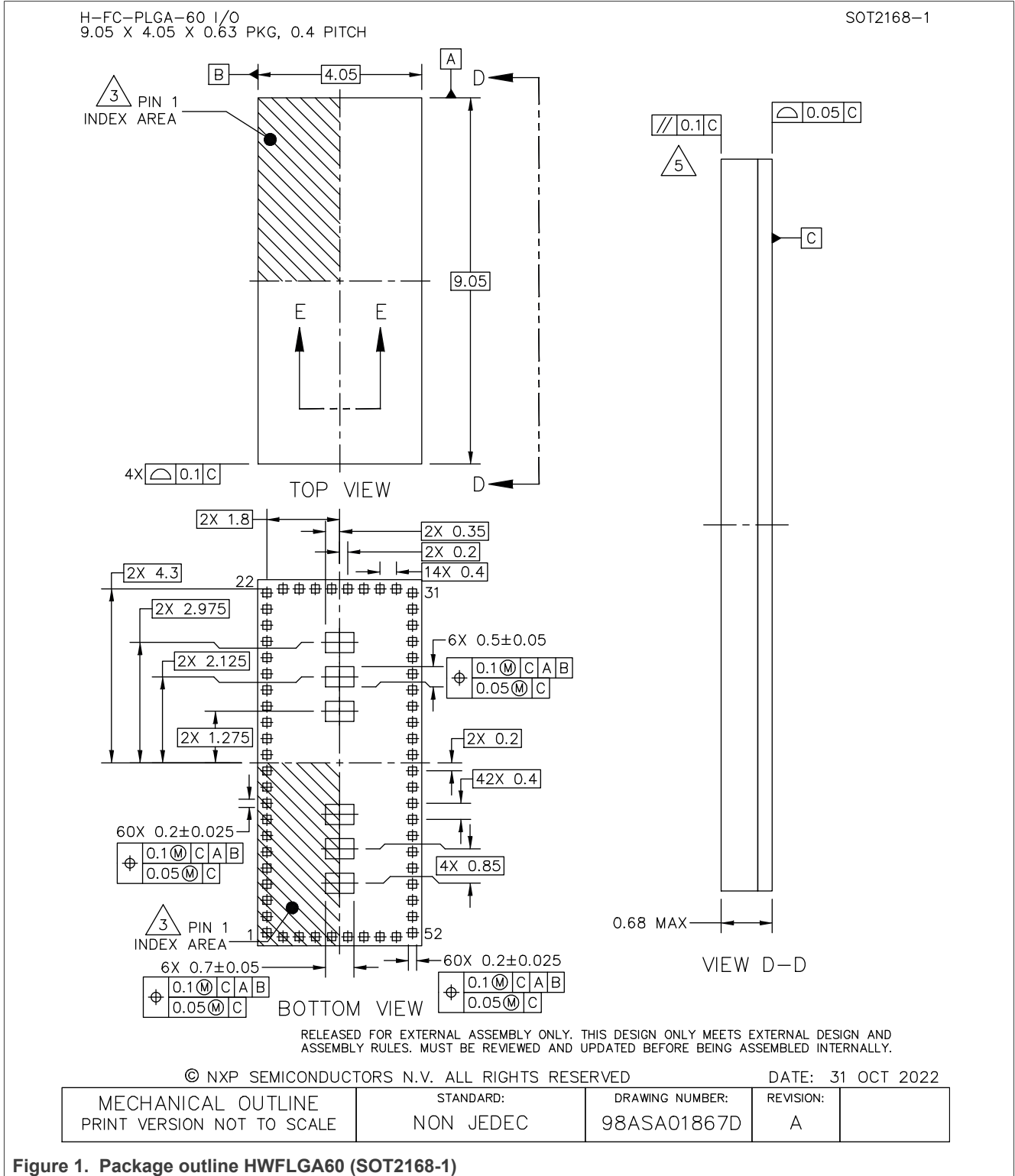
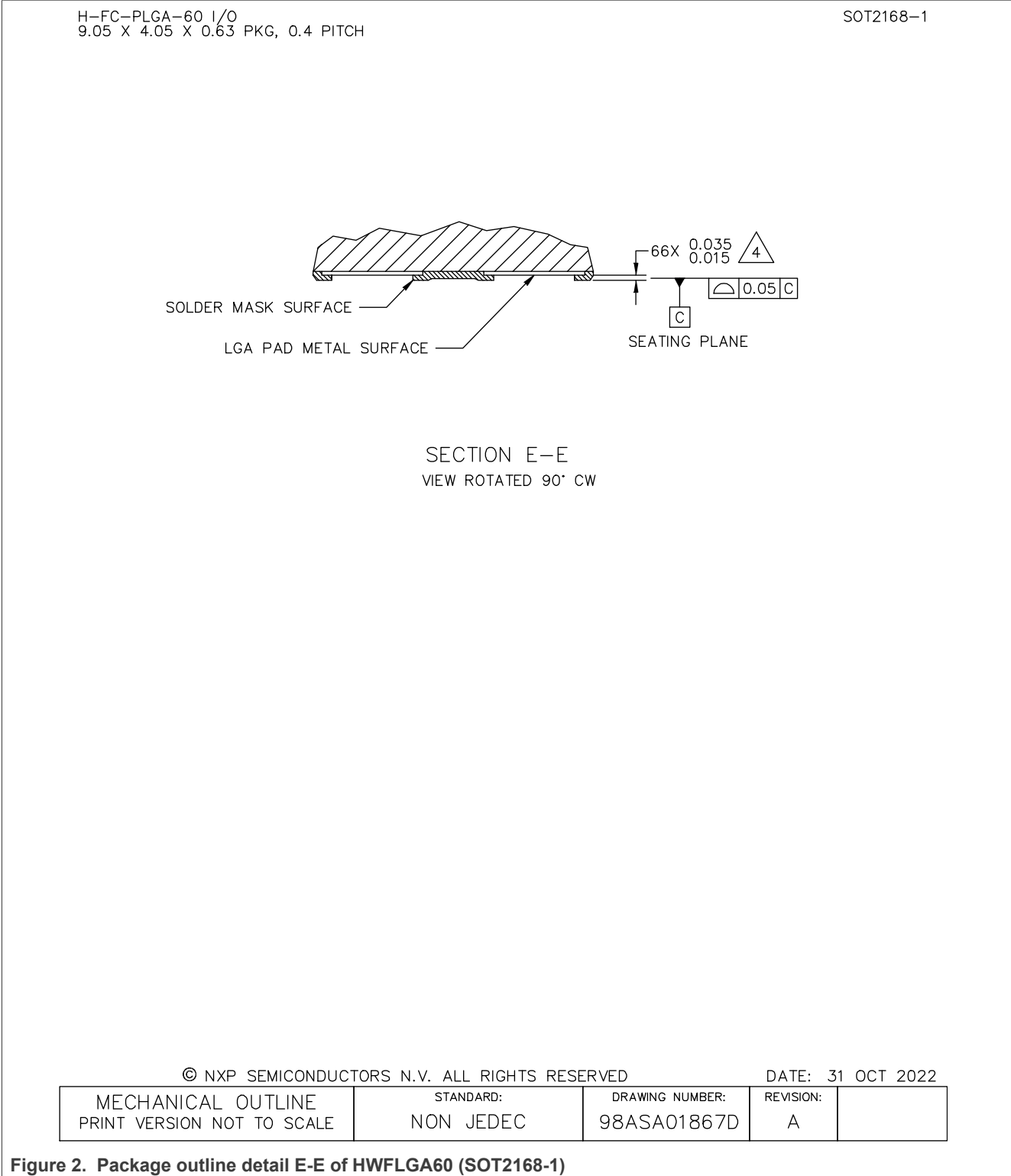
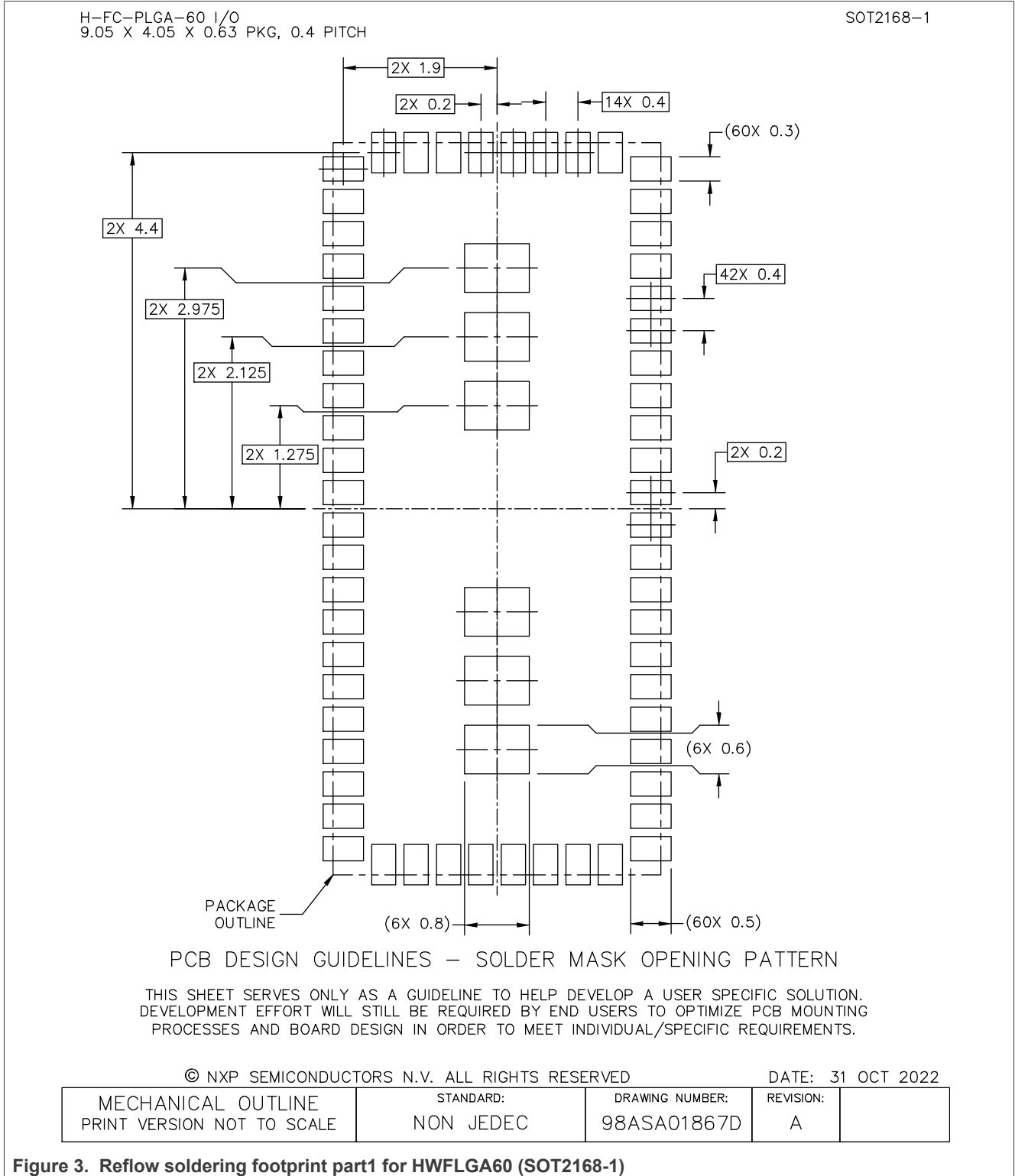


Figure 1. Package outline HWFLGA60 (SOT2168-1)

HWFLGA60, thermal enhanced very very thin finepitch land grid array package, 0.4 mm pitch, 9.05 mm x 4.05 mm x 0.63 mm body



3 Soldering



HWFLGA60, thermal enhanced very very thin finepitch land grid array package, 0.4 mm pitch, 9.05 mm x 4.05 mm x 0.63 mm body

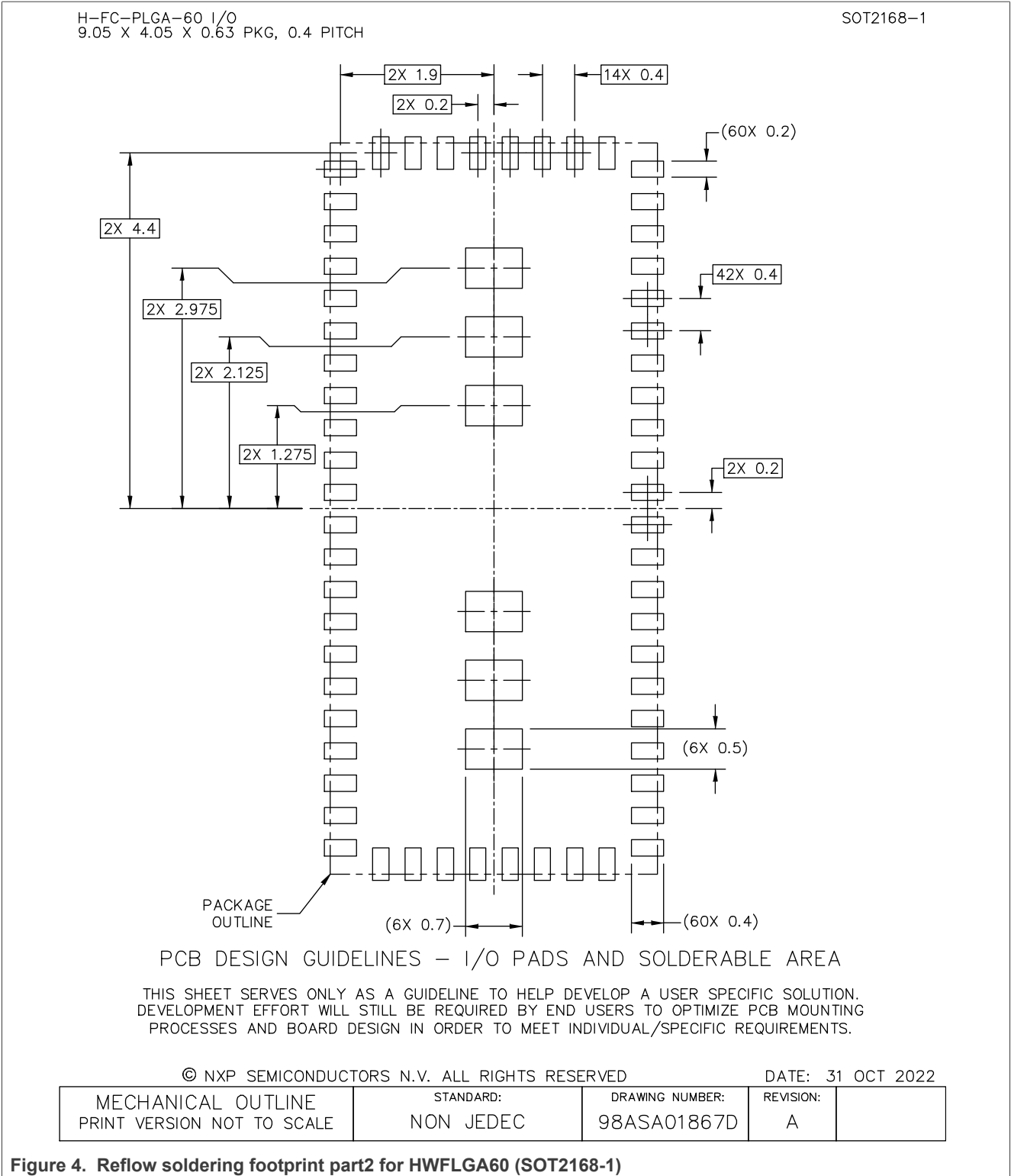


Figure 4. Reflow soldering footprint part2 for HWFLGA60 (SOT2168-1)

HWFLGA60, thermal enhanced very very thin finepitch land grid array package, 0.4 mm pitch, 9.05 mm x 4.05 mm x 0.63 mm body

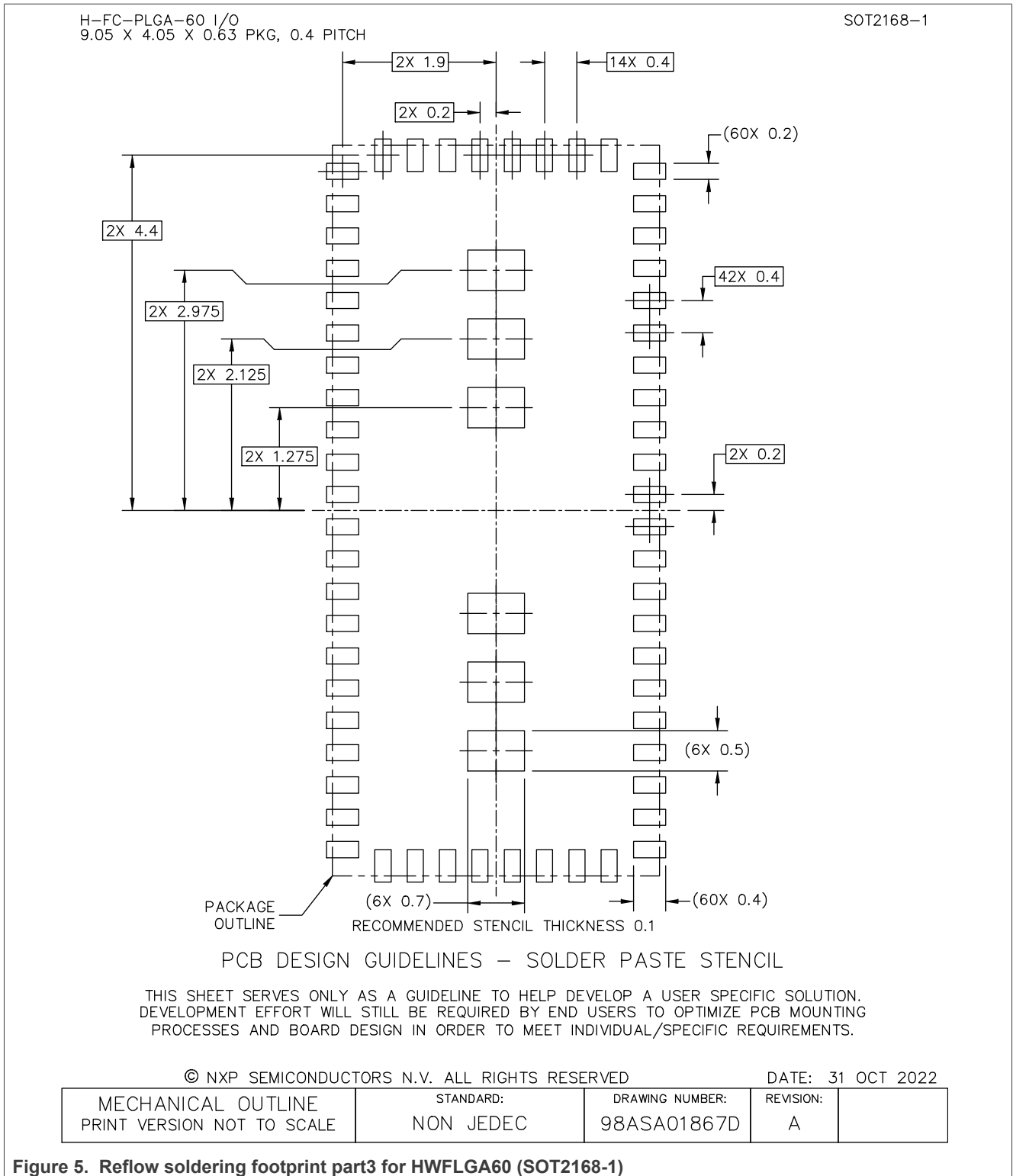


Figure 5. Reflow soldering footprint part3 for HWFLGA60 (SOT2168-1)

HWFLGA60, thermal enhanced very very thin finepitch land grid array package, 0.4 mm pitch, 9.05 mm x 4.05 mm x 0.63 mm body

H-FC-PLGA-60 I/O  
9.05 X 4.05 X 0.63 PKG, 0.4 PITCH

SOT2168-1

NOTES:

- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

4. DIMENSION APPLIES TO ALL LEADS.

5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED

DATE: 31 OCT 2022

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01867D	REVISION: A	
--	------------------------	--------------------------------	----------------	--

Figure 6. Package outline note HWFLGA60 (SOT2168-1)

## 4 Legal information

---

### Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.



**Contents**

---

- 1 Package summary .....1**
- 2 Package outline .....2**
- 3 Soldering .....4**
- 4 Legal information .....8**