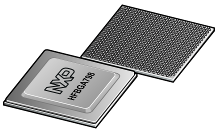
SOT2198-1

H-FC-PBGA798, thermal enhanced - flip chip - plastic ball grid array, 798 terminals, 0.65 mm pitch, 19 mm x 19 mm x 1.94 mm body

24 April 2026 **Package information**



1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	H-FC-PBGA798
Package style descriptive code	H-FC-PBGA (thermal enhanced - flip chip - plastic ball grid array)
Package body material type	P (plastic)
Mounting method type	S (surface mount)
Issue date	07-06-2024
Manufacturer package code	98ASA01985D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	18.9	19	19.1	mm
package width	18.9	19	19.1	mm
package height	1.79	1.94	2.09	mm
nominal pitch	-	0.65	-	mm
actual quantity of termination	-	798	-	

2 Package outline

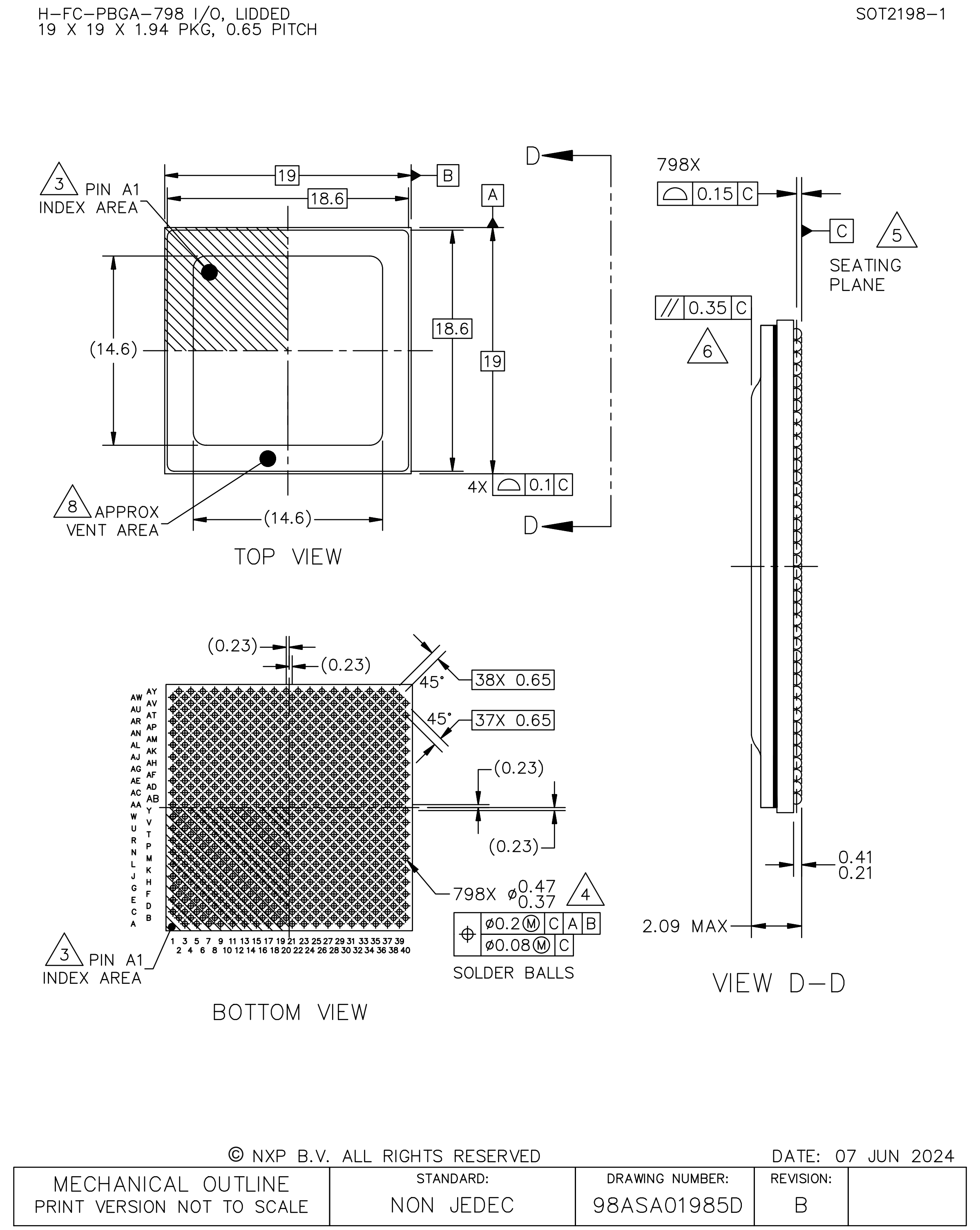
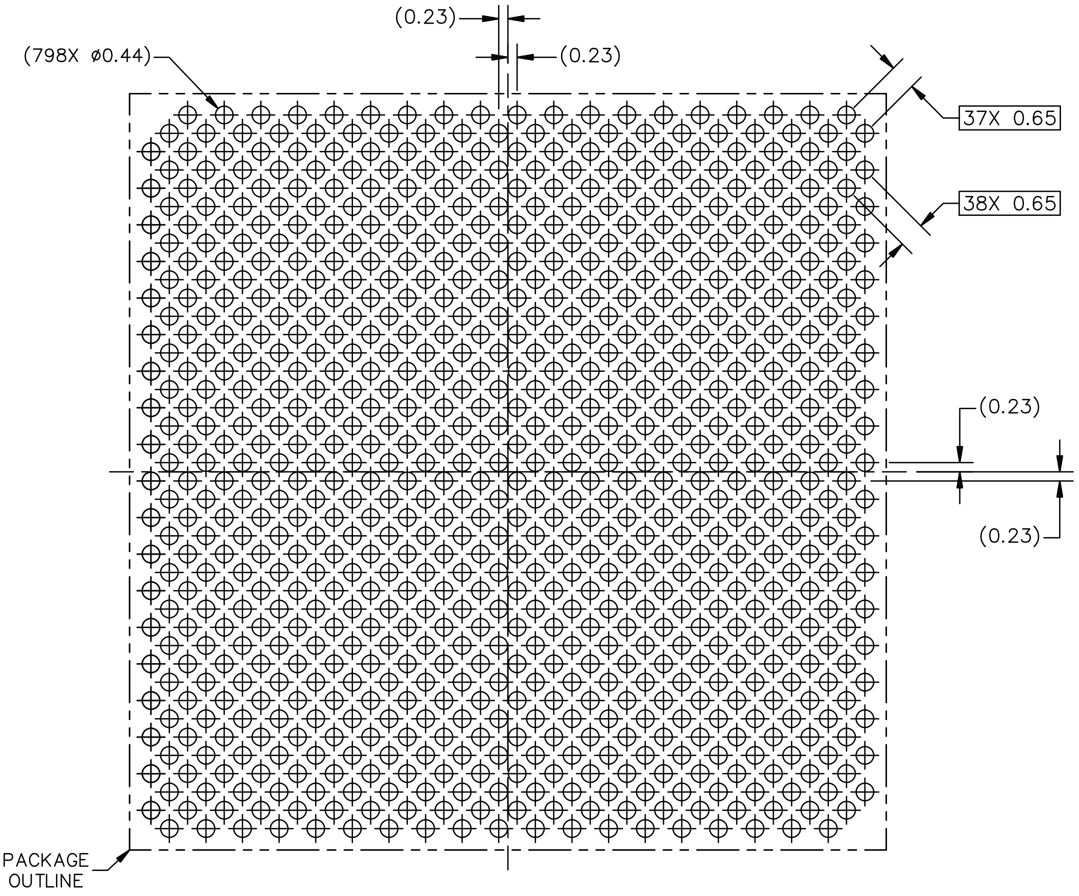


Figure 1. Package outline H-FC-PBGA-798 (SOT2198-1)

3 Soldering

H-FC-PBGA-798 I/O, LIDDED
19 X 19 X 1.94 PKG, 0.65 PITCH

SOT2198-1



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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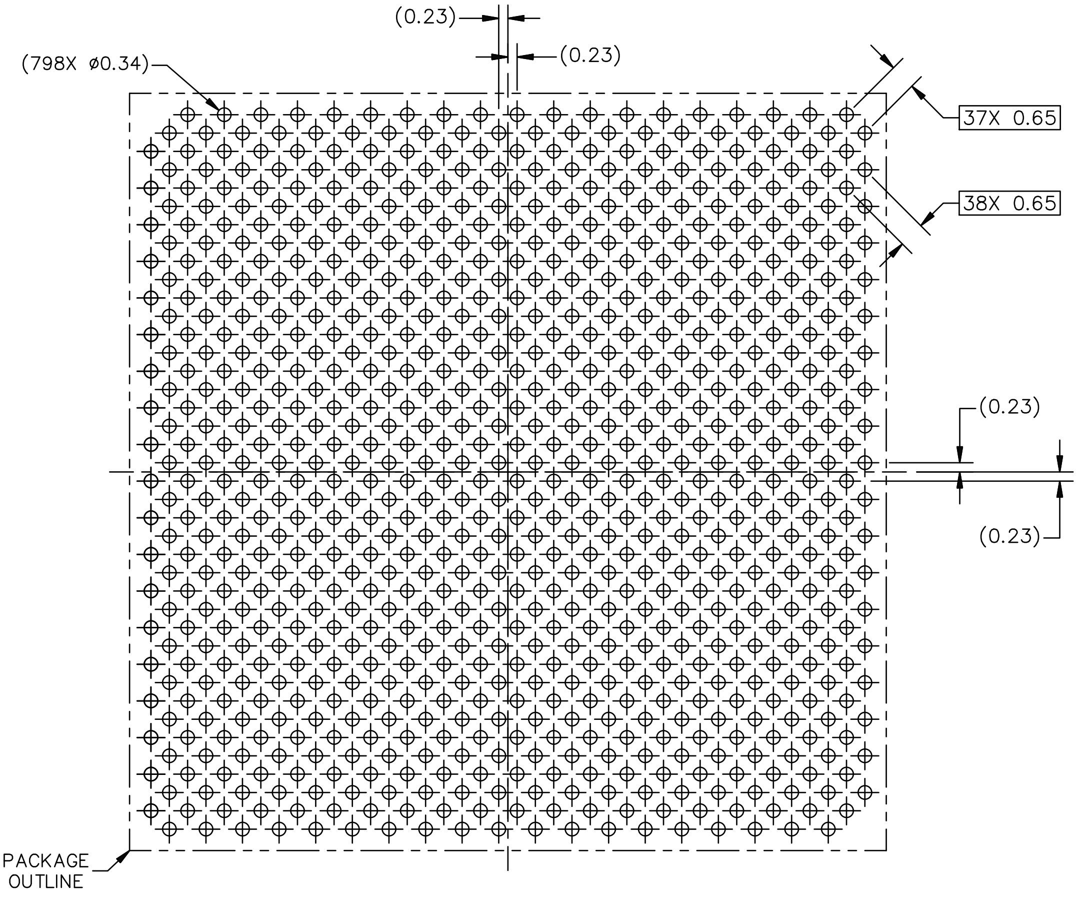
DATE: 07 JUN 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01985D	REVISION: B	

Figure 2. Reflow soldering footprint part1 for H-FC-PBGA-798 (SOT2198-1)

H–FC–PBGA–798 I/O, LIDDED
19 X 19 X 1.94 PKG, 0.65 PITCH

SOT2198–1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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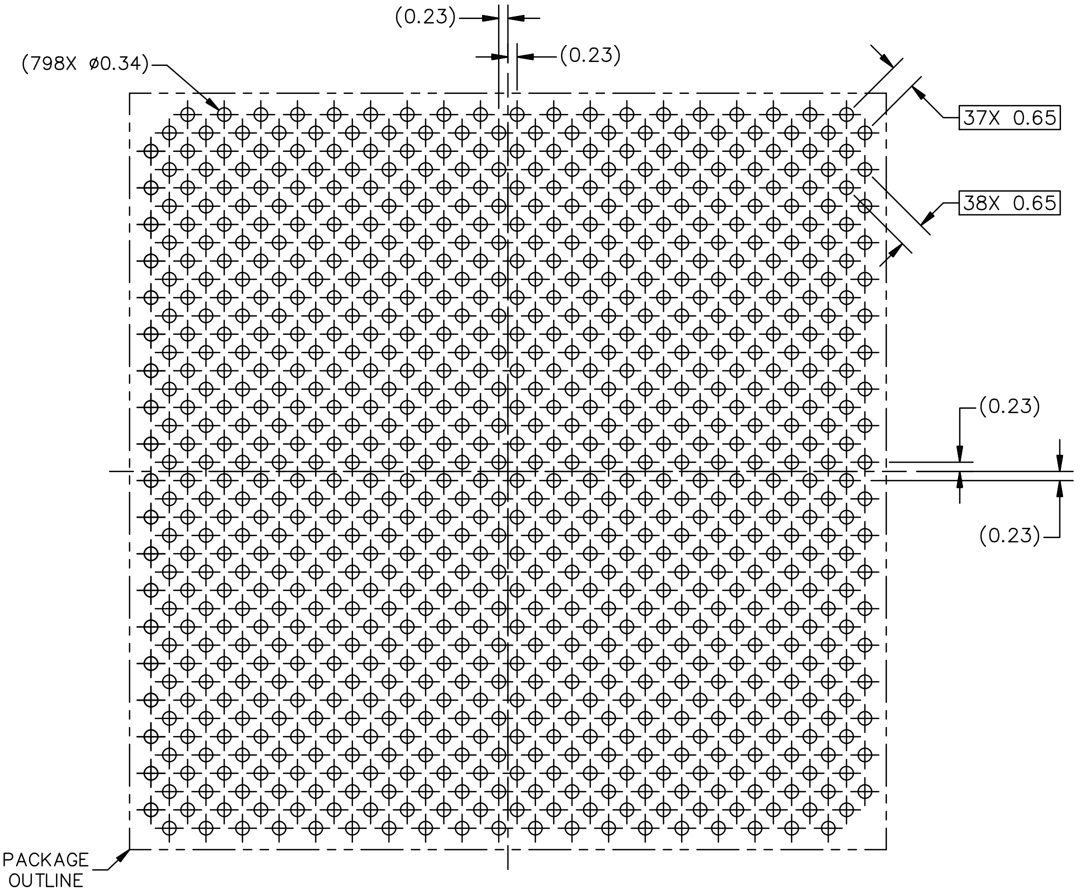
DATE: 07 JUN 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01985D	REVISION: B	

Figure 3. Reflow soldering footprint part2 for H-FC-PBGA-798 (SOT2198-1)

H–FC–PBGA–798 I/O, LIDDED
19 X 19 X 1.94 PKG, 0.65 PITCH

SOT2198–1



RECOMMENDED STENCIL THICKNESS 0.125MM

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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DATE: 07 JUN 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01985D	REVISION: B	

Figure 4. Reflow soldering footprint part3 for H-FC-PBGA-798 (SOT2198-1)

H–FC–PBGA–798 I/O, LIDDED
19 X 19 X 1.94 PKG, 0.65 PITCH

SOT2198–1

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
7. LID OVERHANG ON SUBSTRATE NOT ALLOWED.
8. VENT AREA BETWEEN LID AND SUBSTRATE, SIZE MAY VARY.

DATE: 07 JUN 2024

	STANDARD:	DRAWING NUMBER:	REVISION:	
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	NON JEDEC	98ASA01985D	B	

Figure 5. Package outline note H-FC-PBGA-798 (SOT2198-1)

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