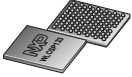


SOT2277-1

WLCSP123, wafer level chip-size package, 123 terminals, 0.4 mm pitch, 4.95 mm x 4.395 mm x 0.525 mm body

25 August 2025

Package information



1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP123
Package style descriptive code	WLCSP (wafer level chip-size package)
Package body material type	S (silicon)
Mounting method type	S (surface mount)
Issue date	05-03-2025
Manufacturer package code	98ASA02243D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	4.95	-	mm
package width	-	4.395	-	mm
seated height	-	0.525	0.565	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	123	-	



WLCSP123, wafer level chip-size package, 123 terminals, 0.4 mm pitch, 4.95 mm x 4.395 mm x 0.525 mm body

2 Package outline

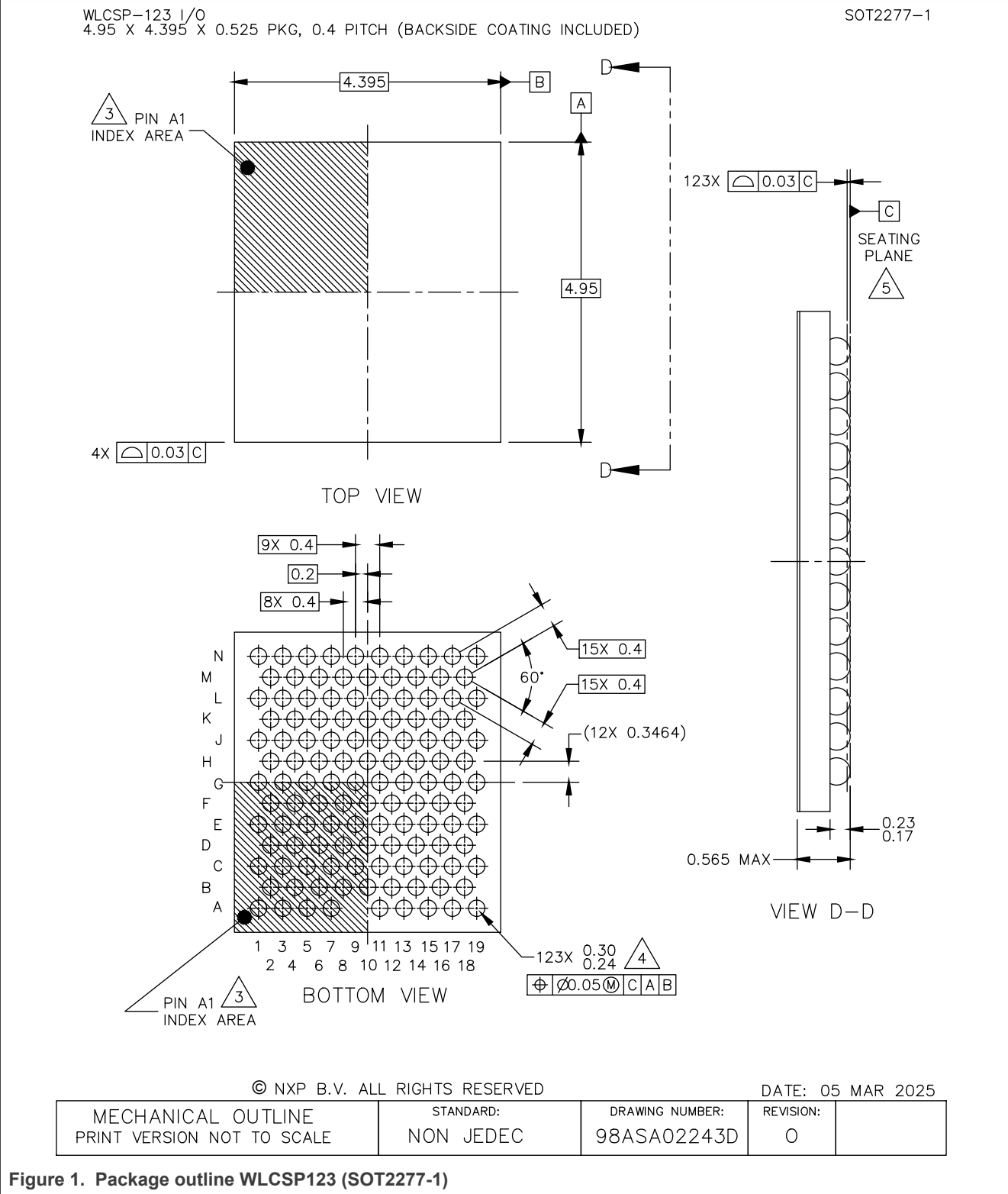
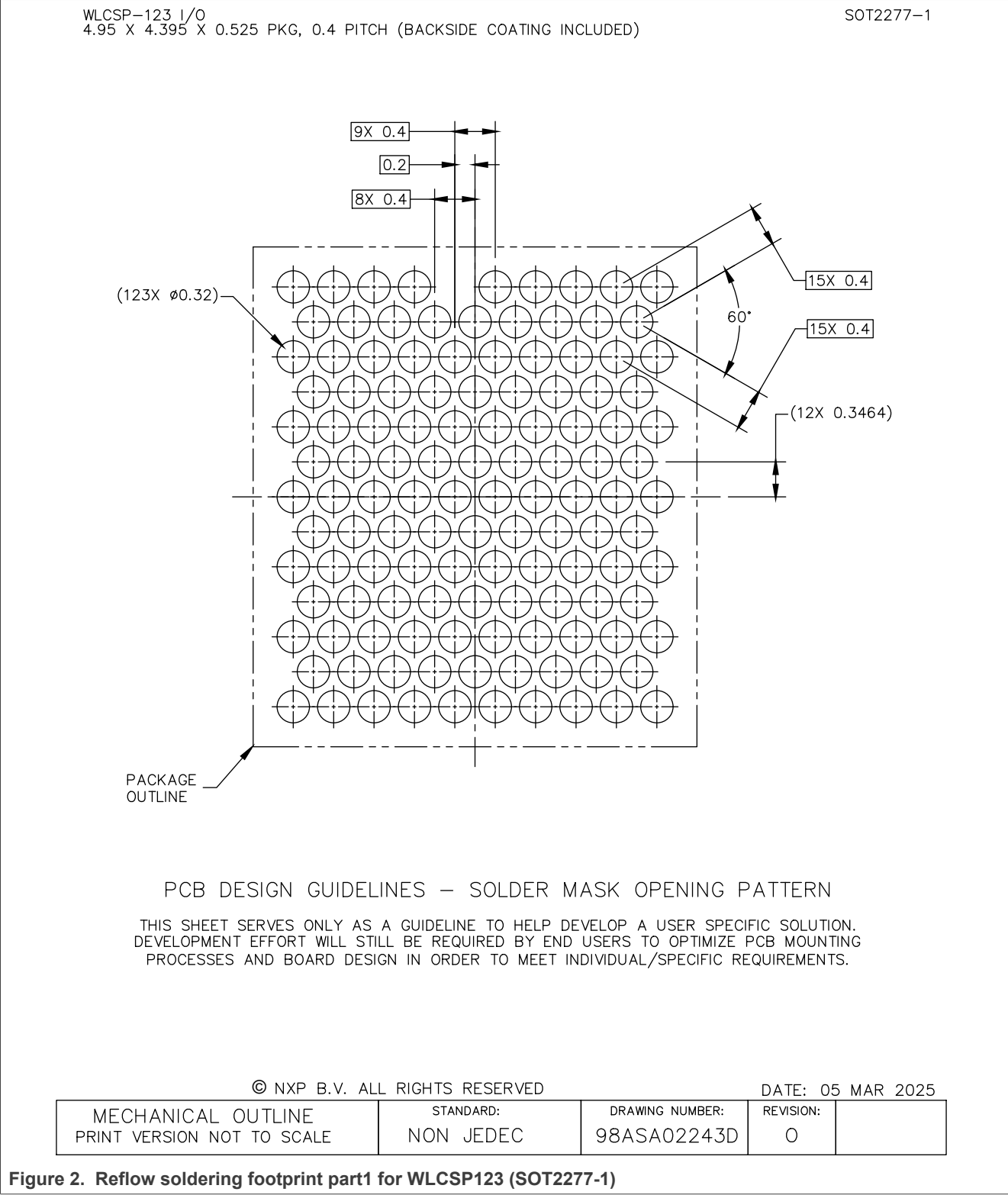


Figure 1. Package outline WLCSP123 (SOT2277-1)

WLCSP123, wafer level chip-size package, 123 terminals, 0.4 mm pitch, 4.95 mm x 4.395 mm x 0.525 mm body

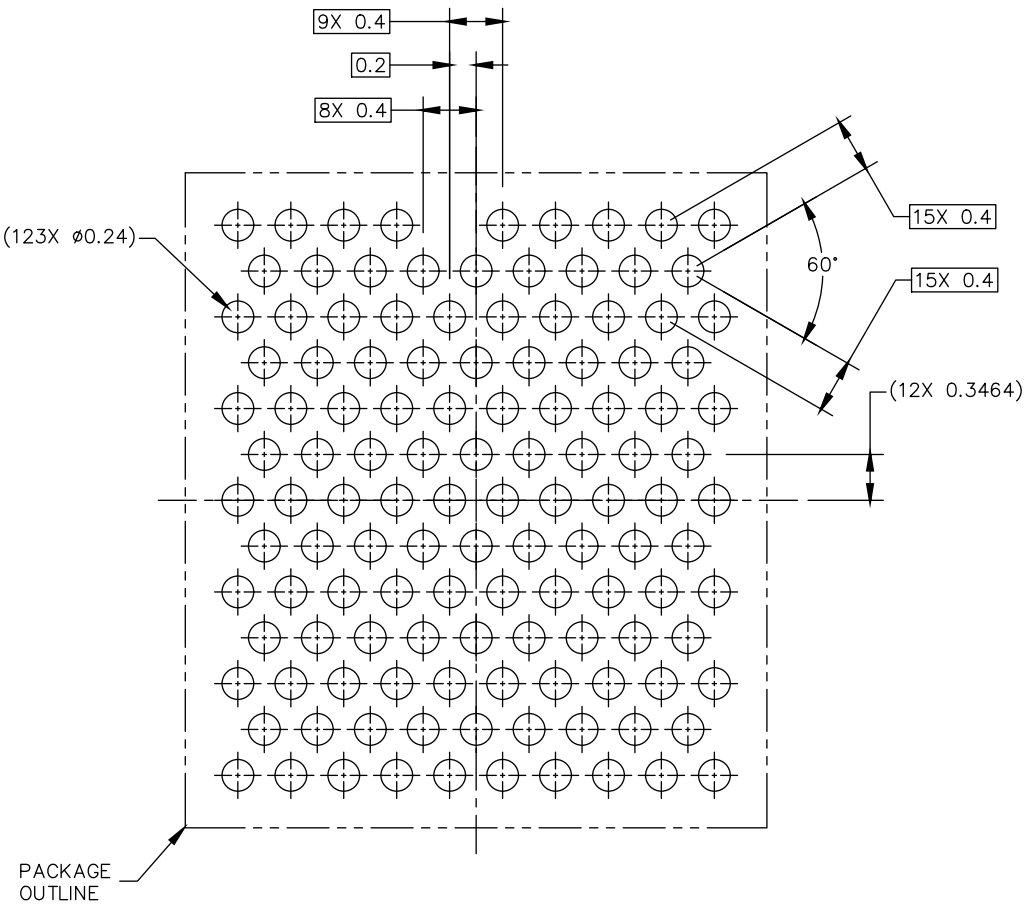
3 Soldering



WLCSP123, wafer level chip-size package, 123 terminals, 0.4 mm pitch, 4.95 mm x 4.395 mm x 0.525 mm body

WLCSP-123 I/O
4.95 X 4.395 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT2277-1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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DATE: 05 MAR 2025

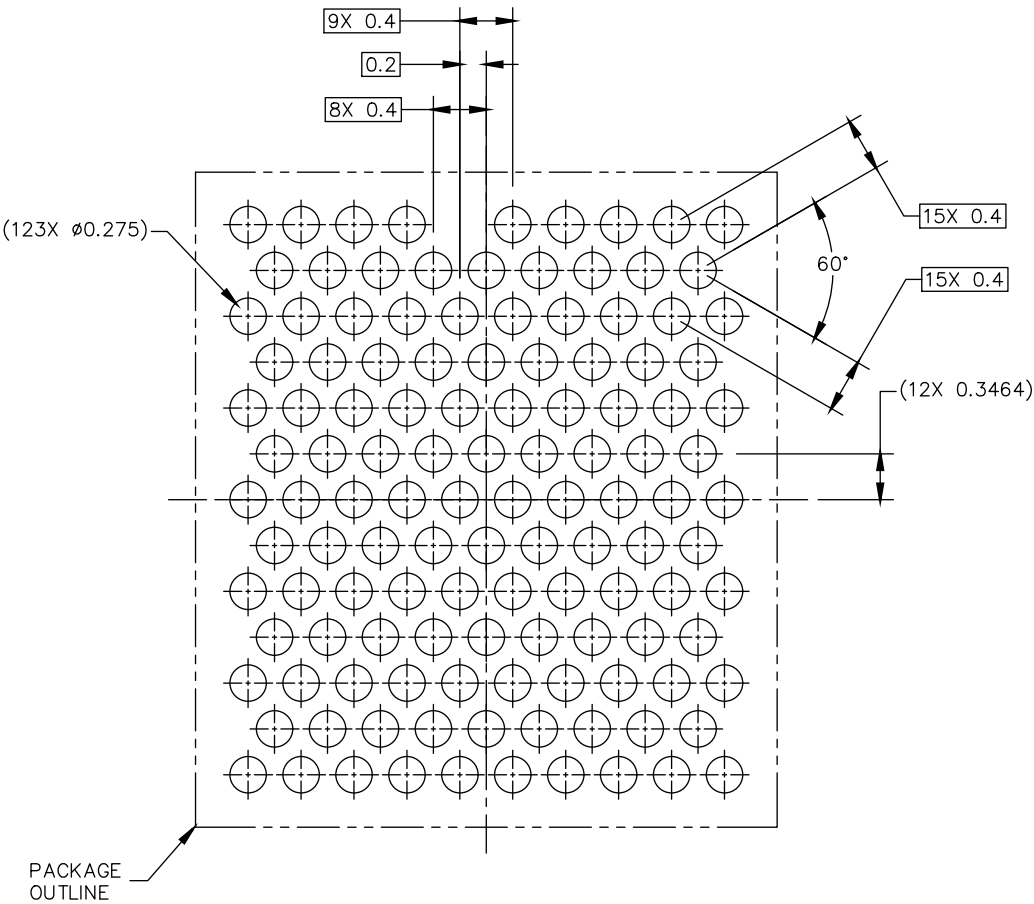
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02243D	REVISION: 0	
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Figure 3. Reflow soldering footprint part2 for WLCSP123 (SOT2277-1)

WLCSP123, wafer level chip-size package, 123 terminals, 0.4 mm pitch, 4.95 mm x 4.395 mm x 0.525 mm body

WLCSP-123 I/O
4.95 X 4.395 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT2277-1



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 4. Reflow soldering footprint part3 for WLCSP123 (SOT2277-1)

WLCSP123, wafer level chip-size package, 123 terminals, 0.4 mm pitch, 4.95 mm x 4.395 mm x 0.525 mm body

WLCSP-123 I/O
4.95 X 4.395 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT2277-1

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
- 4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
- 5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02243D	REVISION: 0	

Figure 5. Package outline note WLCSP123 (SOT2277-1)

4 Legal information

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WLCSP123, wafer level chip-size package, 123 terminals, 0.4 mm pitch, 4.95 mm x 4.395 mm x 0.525 mm body

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