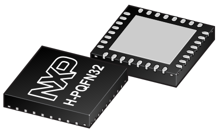
SOT617-29

H-PQFN32, thermal enhanced - plastic quad flat non-lead, 32 terminals, no leads; 0.5 mm pitch, 5 mm x 5 mm x 0.9 mm body

22 January 2026 **Package information**



1 Package summary

Terminal position code	Q (quad)
Package type descriptive code	H-PQFN32
Package style descriptive code	H-PQFN (thermal enhanced - plastic quad flat non-lead)
Package body material type	P (plastic)
Mounting method type	S (surface mount)
Manufacturer package code	98ASA02110D

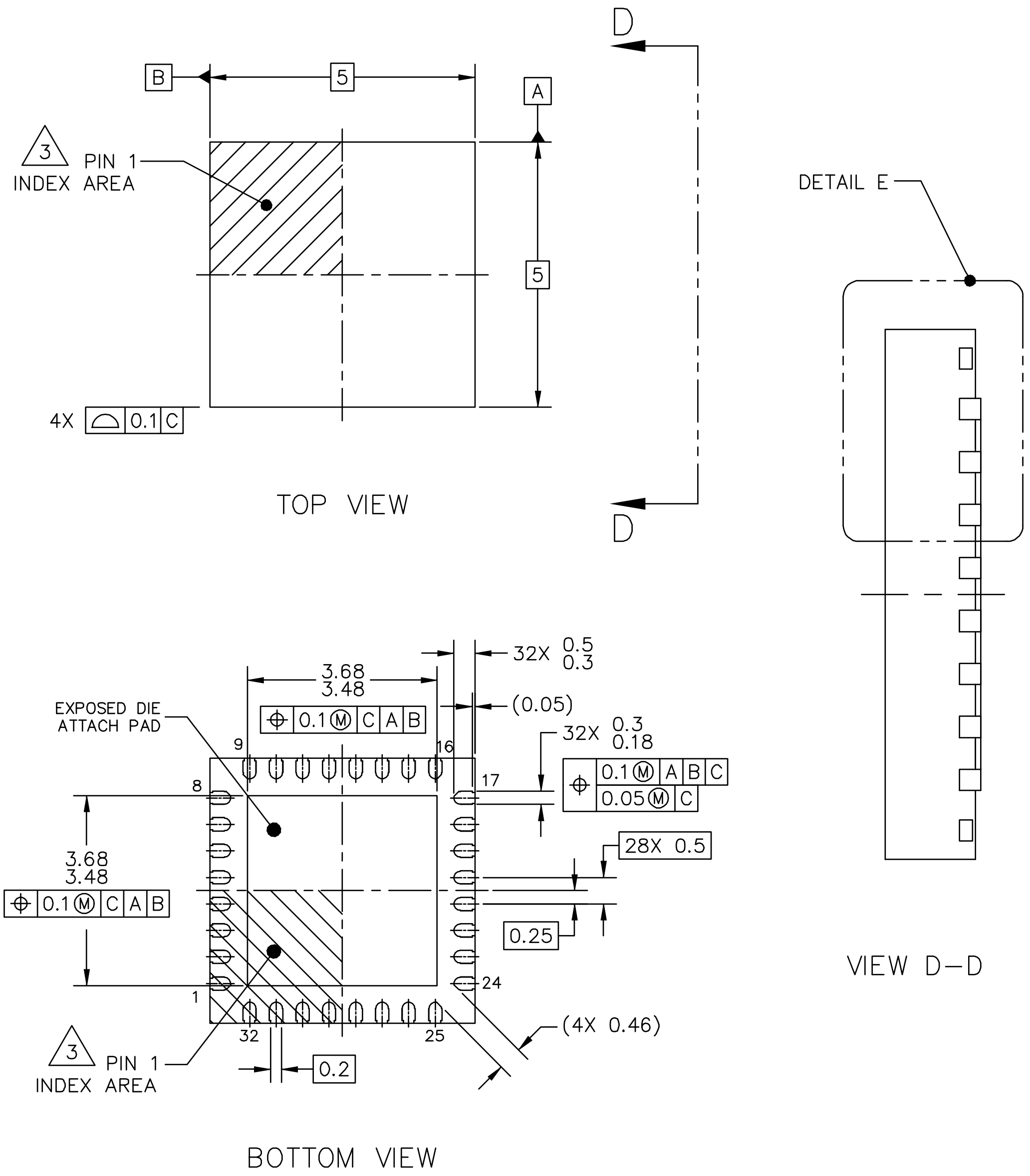
Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	5	-	mm
package width	-	5	-	mm
package height	0.8	0.9	1	mm
nominal pitch	-	0.5	-	mm
actual quantity of termination	-	32	-	

2 Package outline

H–PQFN–32 I/O
5 X 5 X 0.9 PKG, 0.5 PITCH

SOT617–29



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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02110D	REVISION: O	

Figure 1. Package outline H-PQFN32 (SOT617-29)

H-PQFN-32 I/O
5 X 5 X 0.9 PKG, 0.5 PITCH

SOT617-29

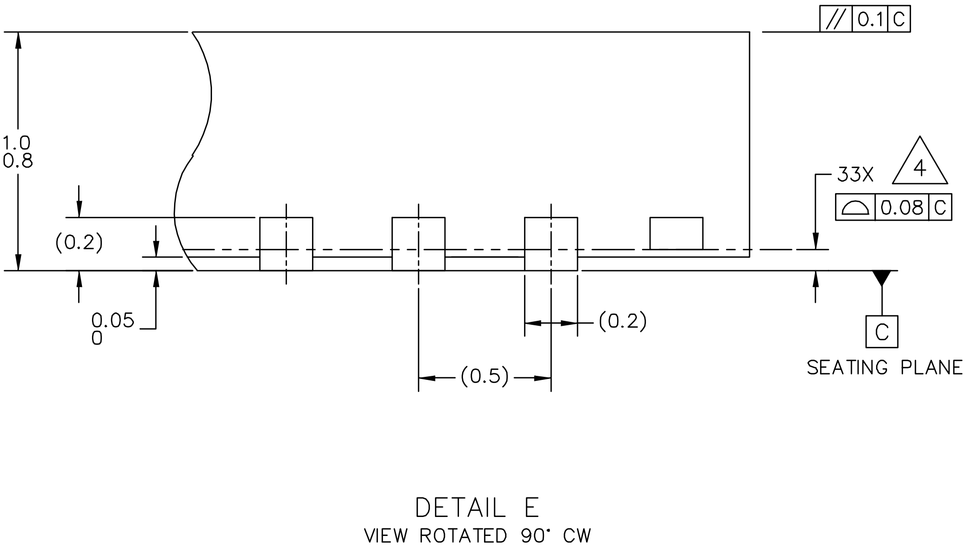

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Figure 2. Package outline detail E of H-PQFN32 (SOT617-29)

3 Soldering

H-PQFN-32 I/O
5 X 5 X 0.9 PKG, 0.5 PITCH

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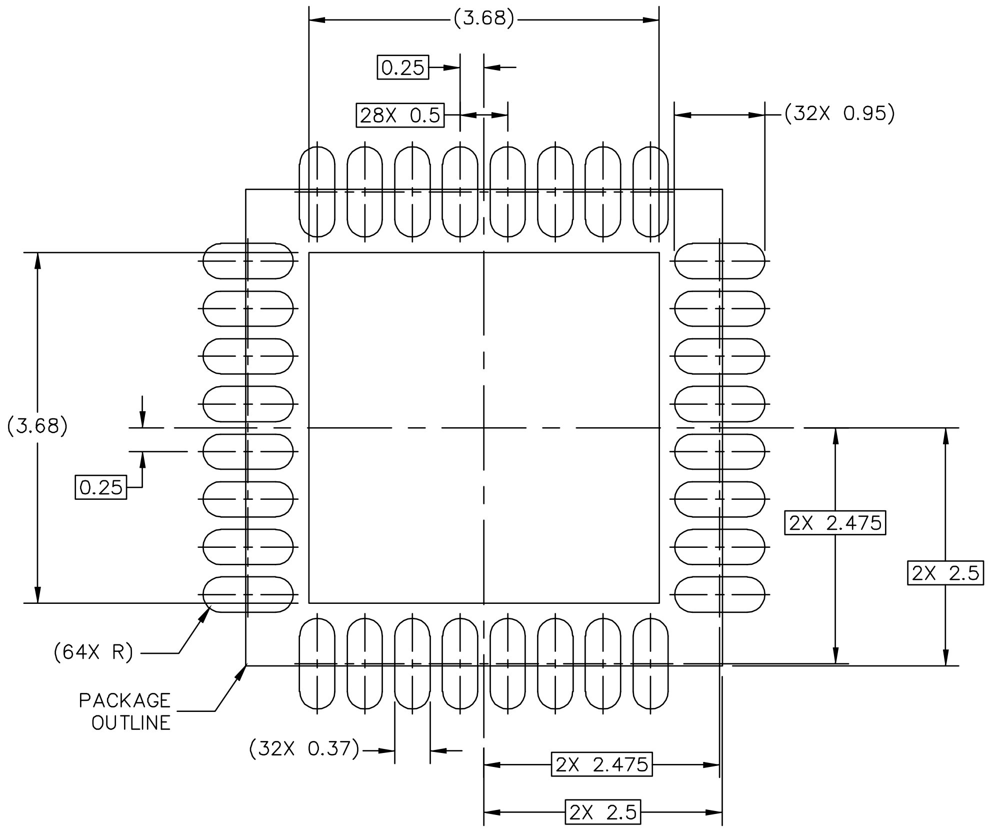

PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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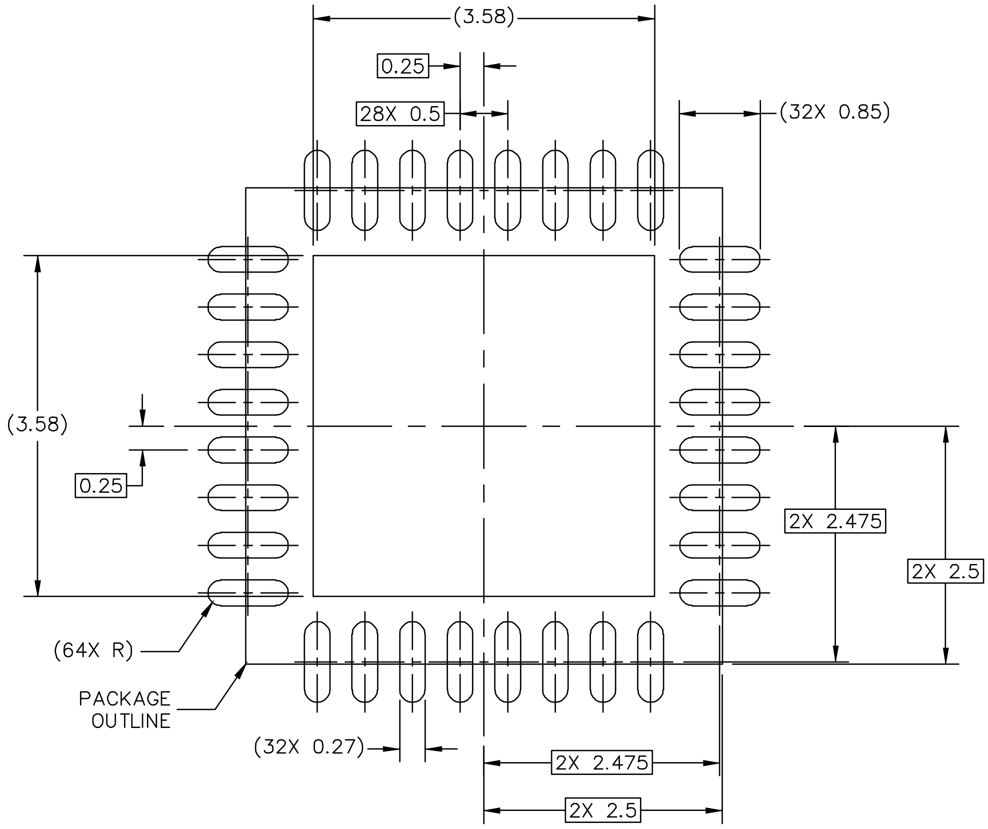
Figure 3. Reflow soldering footprint part 1 for H-PQFN32 (SOT617-29)

H-PQFN-32 I/O
5 X 5 X 0.9 PKG, 0.5 PITCH

SOT617-29



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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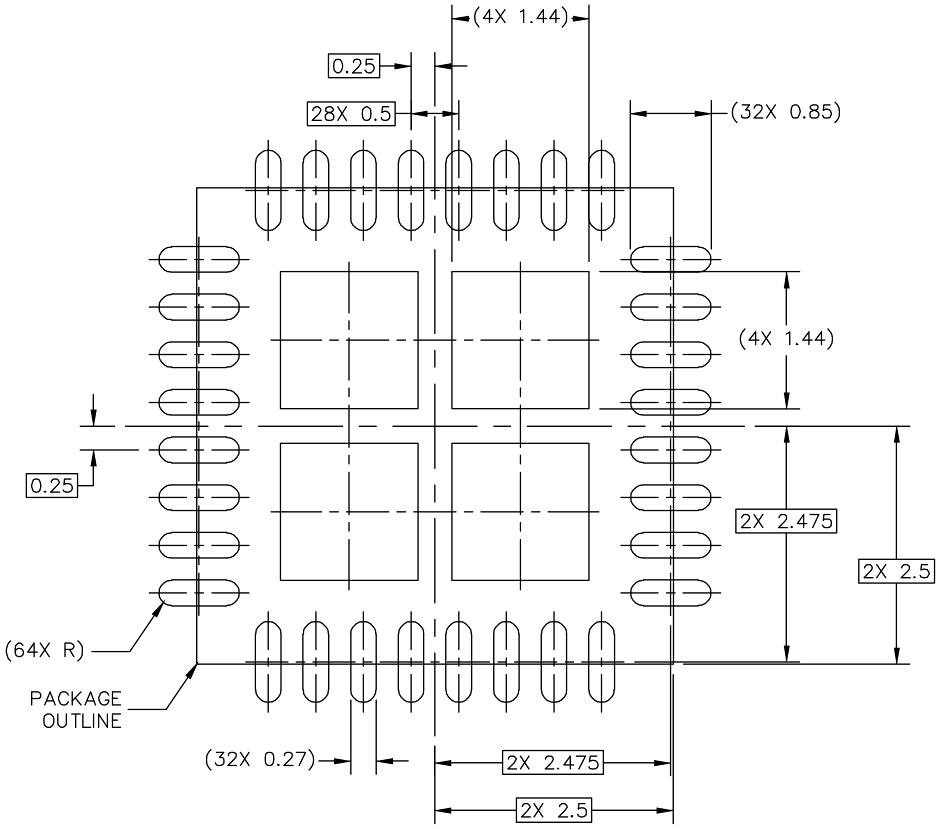
Figure 4. Reflow soldering footprint part 2 for H-PQFN32 (SOT617-29)

H–PQFN–32 I/O
5 X 5 X 0.9 PKG, 0.5 PITCH

SOT617–29



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02110D	REVISION: 0	

Figure 5. Reflow soldering footprint part 3 for H-PQFN32 (SOT617-29)

H-PQFN-32 I/O
5 X 5 X 0.9 PKG, 0.5 PITCH

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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. △ PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. △ COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
5. MIN. METAL GAP FOR LEAD TO EXPORED PAD SHALL BE 0.2 MM.

DATE: 30 MAY 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD:	DRAWING NUMBER:	REVISION:	
	NON JEDEC	98ASA02110D	O	

Figure 6. Package outline note H-PQFN32 (SOT617-29)

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