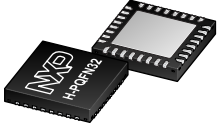


SOT617-30(DD)

H-PQFN32, thermal enhanced - plastic quad flat non-lead, 32 terminals, 0.5 mm pitch, 5 mm x 5 mm x 0.85 mm body

22 June 2026

Package information



1 Package summary

Terminal position code	Q (quad)
Package type descriptive code	H-PQFN32
Package style descriptive code	H-PQFN (thermal enhanced - plastic quad flat non-lead)
Package body material type	P (plastic)
Mounting method type	S (surface mount)
Issue date	30-10-2024
Manufacturer package code	98ASA02234D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	4.9	5	5.1	mm
package width	4.9	5	5.1	mm
seated height	0.8	0.85	1	mm
nominal pitch	-	0.5	-	mm
actual quantity of termination	-	32	-	



H-PQFN32, thermal enhanced - plastic quad flat non-lead, 32 terminals, 0.5 mm pitch, 5 mm x 5 mm
x 0.85 mm body

2 Package outline

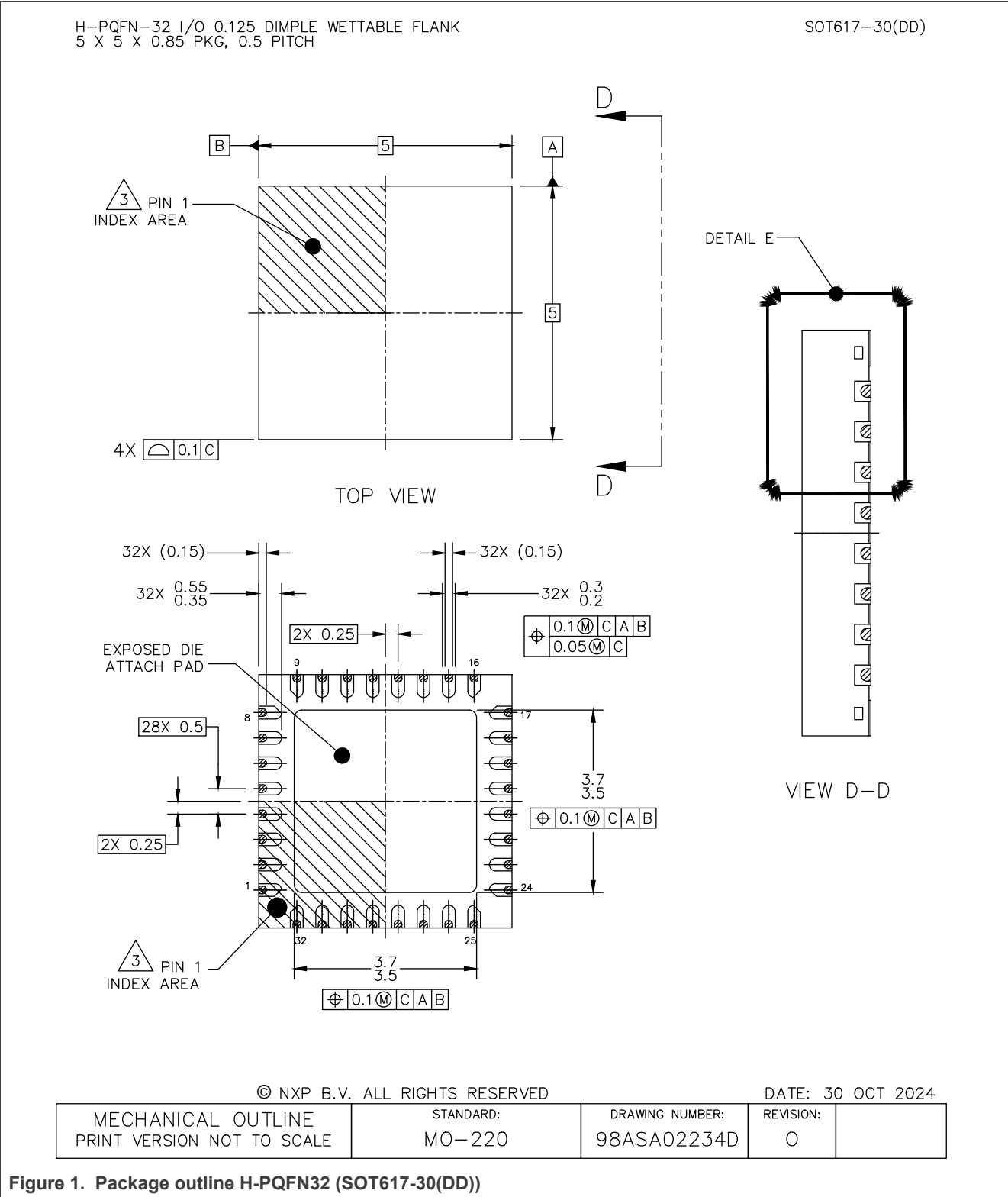
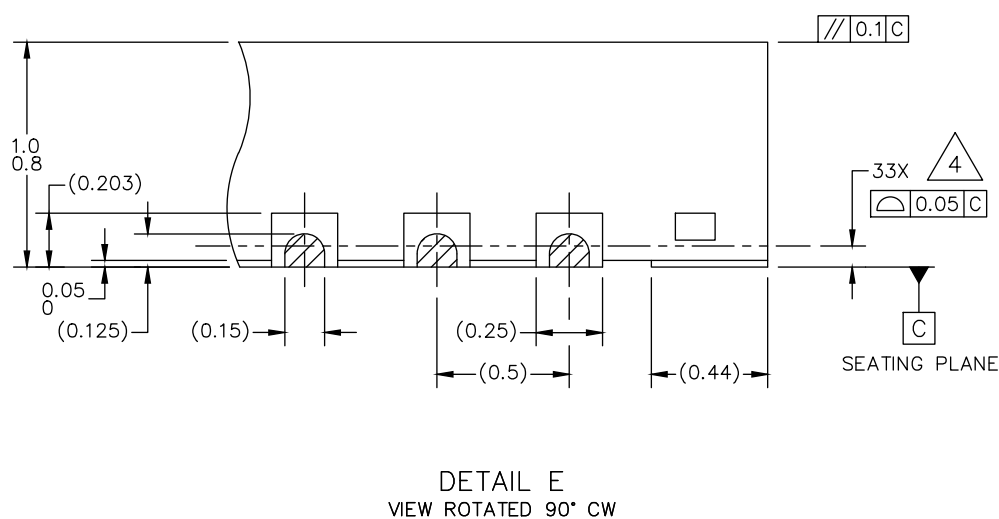


Figure 1. Package outline H-PQFN32 (SOT617-30(DD))

**H-PQFN32, thermal enhanced - plastic quad flat non-lead, 32 terminals, 0.5 mm pitch, 5 mm x 5 mm
x 0.85 mm body**

H-PQFN-32 I/O 0.125 DIMPLE WETTABLE FLANK
5 X 5 X 0.85 PKG, 0.5 PITCH

SOT617-30(DD)



© NXP B.V. ALL RIGHTS RESERVED

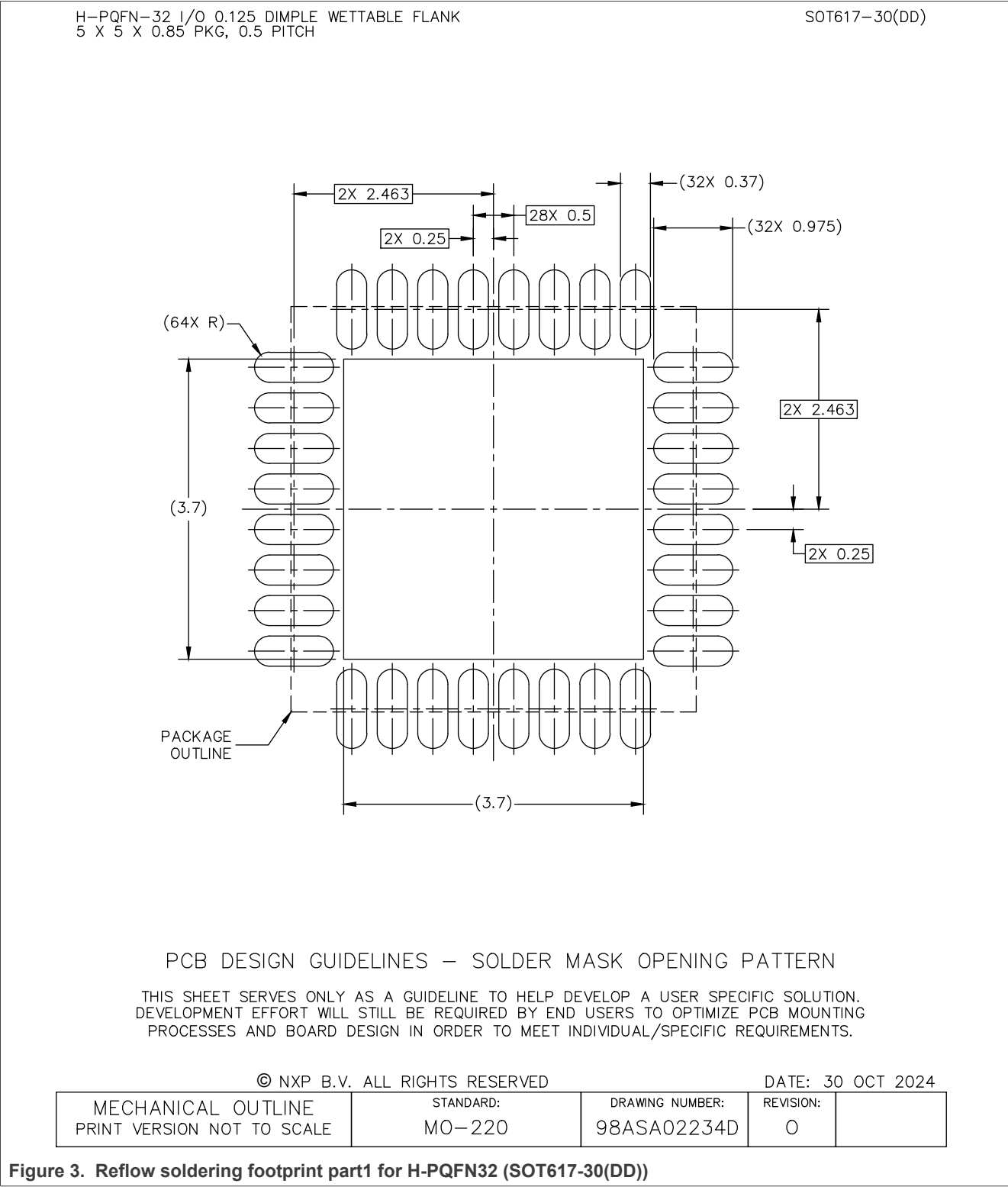
DATE: 30 OCT 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: MO-220	DRAWING NUMBER: 98ASA02234D	REVISION: 0
--	---------------------	--------------------------------	----------------

Figure 2. Package outline detail E of H-PQFN32 (SOT617-30(DD))

H-PQFN32, thermal enhanced - plastic quad flat non-lead, 32 terminals, 0.5 mm pitch, 5 mm x 5 mm
x 0.85 mm body

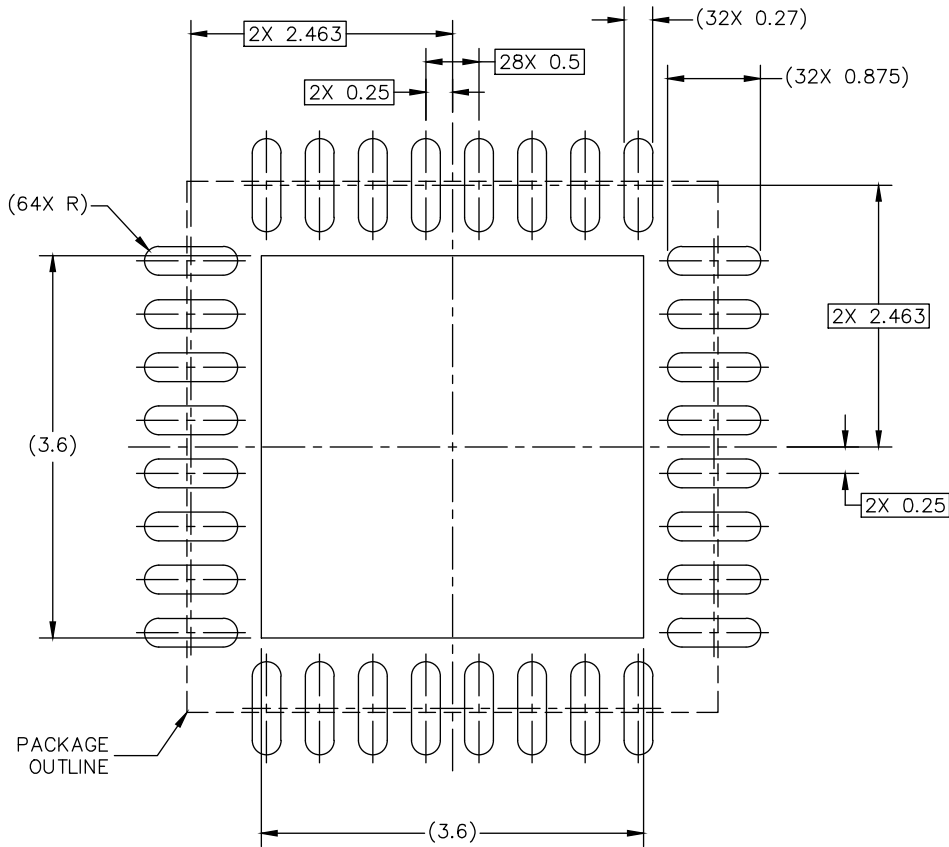
3 Soldering



H-PQFN32, thermal enhanced - plastic quad flat non-lead, 32 terminals, 0.5 mm pitch, 5 mm x 5 mm
x 0.85 mm body

H-PQFN-32 I/O 0.125 DIMPLE WETTABLE FLANK
5 X 5 X 0.85 PKG, 0.5 PITCH

SOT617-30(DD)



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION.
DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING
PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 30 OCT 2024

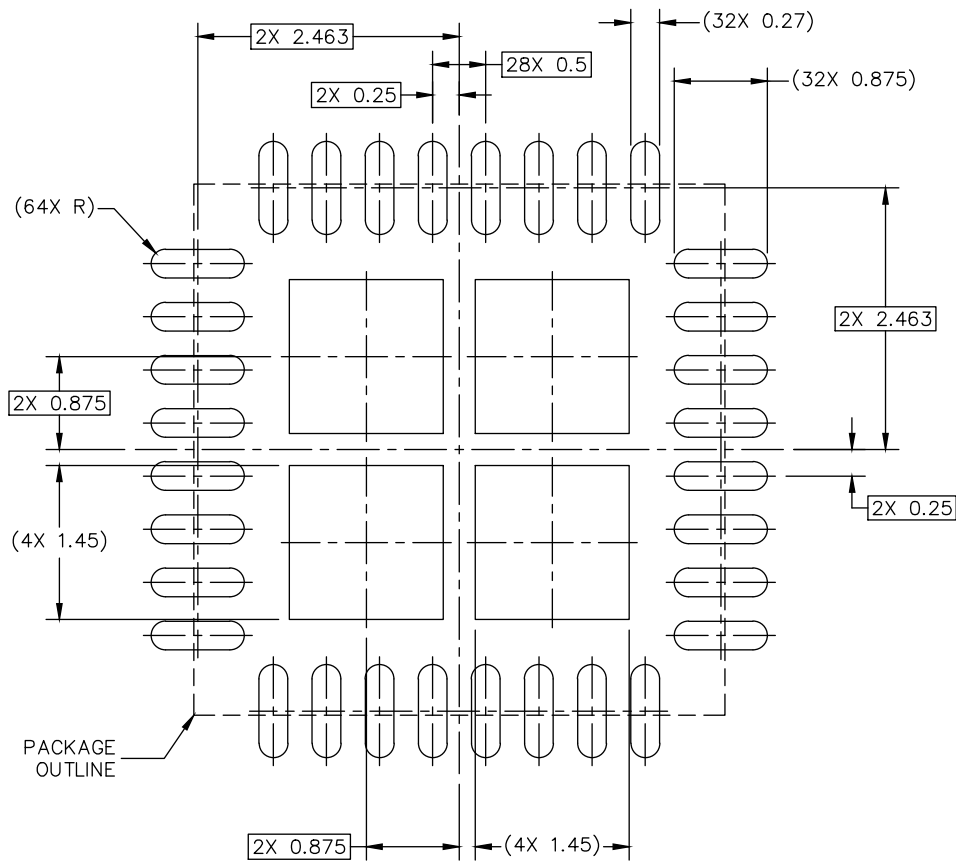
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: MO-220	DRAWING NUMBER: 98ASA02234D	REVISION: O
--	---------------------	--------------------------------	----------------

Figure 4. Reflow soldering footprint part2 for H-PQFN32 (SOT617-30(DD))

H-PQFN32, thermal enhanced - plastic quad flat non-lead, 32 terminals, 0.5 mm pitch, 5 mm x 5 mm
x 0.85 mm body

H-PQFN-32 I/O 0.125 DIMPLE WETTABLE FLANK
5 X 5 X 0.85 PKG, 0.5 PITCH

SOT617-30(DD)



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION.
DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING
PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 30 OCT 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: MO-220	DRAWING NUMBER: 98ASA02234D	REVISION: 0	
--	---------------------	--------------------------------	----------------	--

Figure 5. Reflow soldering footprint part3 for H-PQFN32 (SOT617-30(DD))

H-PQFN32, thermal enhanced - plastic quad flat non-lead, 32 terminals, 0.5 mm pitch, 5 mm x 5 mm
x 0.85 mm body

H-PQFN-32 I/O 0.125 DIMPLE WETTABLE FLANK
5 X 5 X 0.85 PKG, 0.5 PITCH

SOT617-30(DD)

NOTES:

- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
- 4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG.
- 5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 30 OCT 2024

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: MO-220	DRAWING NUMBER: 98ASA02234D	REVISION: 0	
--	---------------------	--------------------------------	----------------	--

Figure 6. Package outline note H-PQFN32 (SOT617-30(DD))

Legal information

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

H-PQFN32, thermal enhanced - plastic quad flat non-lead, 32 terminals, 0.5 mm pitch, 5 mm x 5 mm
x 0.85 mm body

Contents

1	Package summary	1
2	Package outline	2
3	Soldering	4
	Legal information	8

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.