

DSP56652

Advance Information INTEGRATED CELLULAR BASEBAND PROCESSOR

Motorola designed the ROM-based DSP56652 to support the rigorous demands of the cellular subscriber market. The high level of on-chip integration in the DSP56652 minimizes application system design complexity and component count, resulting in very compact implementations. This integration also yields very low-power consumption and cost-effective system performance. The DSP56652 chip combines the power of Motorola's 32-bit M•CORE™ MicroRISC Engine (MCU) and the DSP56600 digital signal processor (DSP) core with on-chip memory, protocol timer, and custom peripherals to provide a single-chip cellular base-band processor. **Figure 1** shows the basic block diagram of the DSP56652.

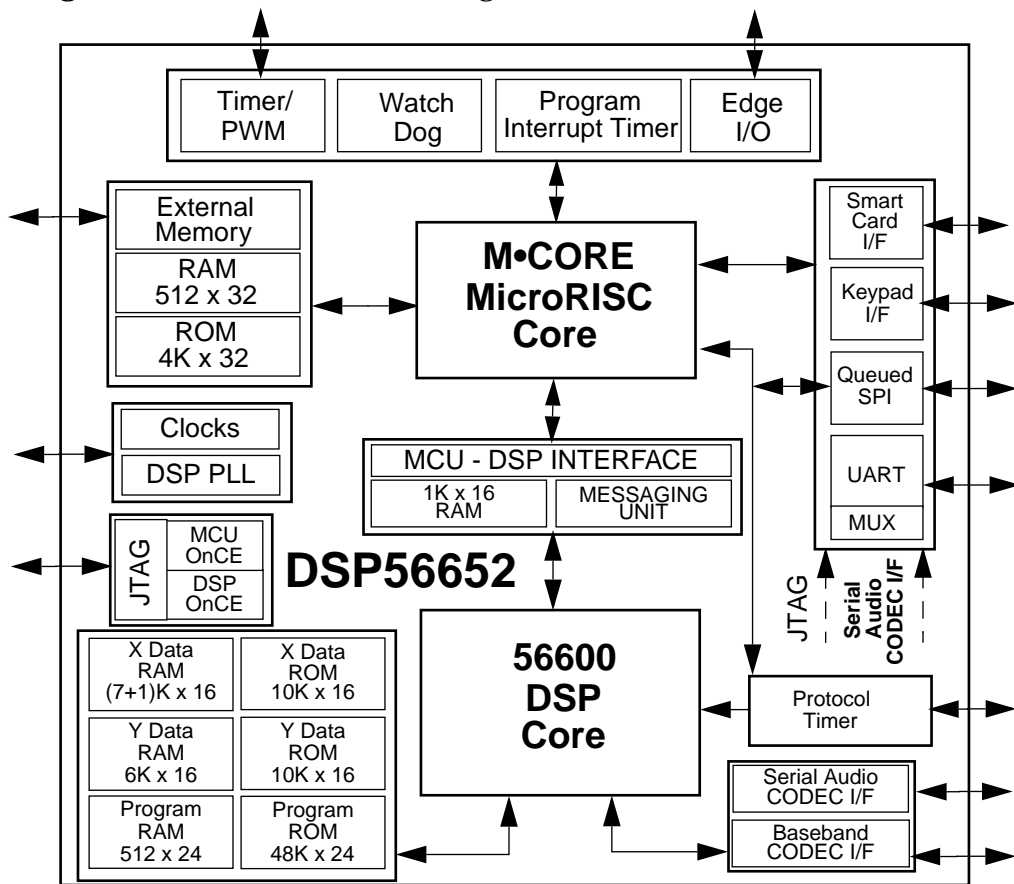


Figure 1 DSP56652 System Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FEATURES

- RISC M•CORE MCU
 - 32-bit load/store RISC architecture
 - Fixed 16-bit instruction length
 - 16-entry 32-bit general-purpose register file
 - 32-bit internal address and data buses
 - Efficient four-stage, fully interlocked execution pipeline
 - Single-cycle execution for most instructions, two cycles for branches and memory accesses
 - Special branch, byte, and bit manipulation instructions
 - Support for byte, half-word, and word memory accesses
 - Fast interrupt support via vectoring/auto-vectoring and a 16-entry dedicated alternate register file
- High-performance DSP56600 core
 - 1 × engine (e.g., 70 MHz = 70 MIPS)
 - Fully pipelined 16 × 16-bit parallel multiplier-accumulator (MAC)
 - Two 40-bit accumulators including extension bits
 - 40-bit parallel barrel shifter
 - Highly parallel instruction set with unique DSP addressing modes
 - Position-independent code support
 - Nested hardware DO loops
 - Fast auto-return interrupts
 - On-chip support for software patching and enhancements
 - Realtime trace capability via external address bus
- On-chip memories
 - 4K × 32-bit MCU ROM
 - 512 × 32-bit MCU RAM
 - 48K × 24-bit DSP program ROM
 - 512 × 24-bit DSP program RAM
 - 20K × 16-bit DSP data ROM, split into 10K x 16-bit each of X and Y data ROM spaces
 - 14K × 16-bit DSP data RAM, split into (7 + 1)K × 16-bit X data RAM and 6K x 16-bit Y data RAM spaces

- On-chip peripherals
 - Fully programmable phase-locked loop (PLL) for DSP clock generation
 - External Interface module (EIM) for glueless system integration
 - External 22-bit address and 16-bit data MCU buses
 - Thirty-two source MCU interrupt controller
 - Intelligent MCU/DSP interface (MDI) dual 1K x 16-bit RAM (shares 1K DSP X data RAM) with messaging status and control
 - Serial audio codec port
 - Serial baseband codec port
 - Protocol timer frees the MCU from radio channel timing events
 - Queued serial peripheral interface (SPI)
 - Keypad port capable of scanning up to an 8 × 8 matrix keypad
 - General-purpose MCU and DSP timers
 - Pulse width modulation (PWM) output
 - Universal asynchronous receiver/transmitter (UART) with FIFO
 - IEEE 1149.1-compliant boundary scan JTAG test access port (TAP)
 - Integrated DSP/M•CORE On-Chip Emulation (OnCE™) module
 - DSP address bus visibility mode for system development
 - ISO 7816-compatible Smart Card port
- Operating features
 - Comprehensive static and dynamic power management
 - M•CORE operating frequency: dc to 16.8 MHz at 1.8 V or dc to 40 MHz at 2.5 V
 - DSP operating frequency: dc to 58.8 MHz at 1.8 V or dc to 70 MHz at 2.5 V
 - Internal operating voltage range: 1.8–2.5 V with 3.3 V-tolerant I/O
 - Operating temperature: –40° to 85°C ambient
 - Package option: 15 × 15 mm, 196-lead PBGA

TARGET APPLICATIONS

The DSP56652 is intended for use in cellular subscriber applications and other applications needing both DSP and control processing.


PRODUCT DOCUMENTATION

The four manuals listed in **Table 1** are required for a complete description of the DSP56652 and are necessary to design with the part properly. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or the World Wide Web.

Table 1 DSP56652 Documentation

Document Name	Description of Contents	Order Number
DSP56600 Family Manual	Detailed description of the DSP56600 family core processor architecture and instruction set	DSP56600FM/AD
M•CORE Reference Manual	Detailed description of the M•CORE MCU and instruction set	MCORERM/AD
DSP56652 User's Manual	Detailed description of DSP56652 memory, peripherals, and interfaces	DSP56652UM/D
DSP56652 Technical Data	DSP56652 pin and package descriptions; electrical and timing specifications	DSP56652/D

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