

MC33777B

Battery junction box monitor integrated circuit

Rev. 1.0 — 23 January 2026

Product brief

1 General description

The MC33777B is a battery junction box controller integrated circuit (IC) designed for automotive applications, such as hybrid electric vehicles (HEV) and electric vehicles (EV), and industrial applications, such as energy storage systems (ESS).

The device performs multiple redundant current, voltage and temperature measurements. It includes a configurable event manager and integrates pyrotechnic switch drivers.

It locally processes the measurement results and autonomously detects application fault events (for example, short circuit, crash signals), to trigger fast reactions without a microcontroller intervention (GPIOs, pyrotechnic switch).

The current measurement interfaces support both shunt and Hall sensor measurements.

The two unique integrated pyrotechnic switch drivers operate independently and include a large set of diagnostic capabilities.

The supported interface options include an isolated daisy chain (TPL3) or a serial peripheral interface (SPI) for communication with the microcontroller.

The MC33777B supports the highest automotive safety integrity level (ASIL D) for all its features.



2 Features and benefits

- Current measurement
 - Four current measurement inputs (supporting two ASIL D current measurements)
 - One precise ADC per input (27 bit, 2 kHz)
 - One fast ADC per input (16 bit, 125 kHz, 8 μ s data rate)
 - Supports Hall sensor measurement (5 V range)
 - Measurement compliant with stringent EMC requirements (for example, portable transmitter immunity)
 - Shunt temperature drift compensation with external temperature sensor
 - One coulomb counter per channel
 - Overcurrent detection (threshold, di/dt calculation, melting fuse emulation)
 - Switchable architecture support (2 x 400 V/800 V) with real-time calculation of current between packs
- General-purpose measurement
 - 16 measurement inputs, supporting up to eight redundant measurements (16 bit, 1 kHz)
 - Overvoltage and undervoltage detection
 - Multiplexed with 2 x 8 GPIOs
- Event manager
 - Set of input events from other modules (for example, overcurrent detection, fuse emulation, overvoltage detection, digital input for crash signal monitoring, and so on)
 - Configurable logical processing of the events (for example, debouncing, OR, custom logic functions, and so on)
 - Triggering reactions (for example, pyrotechnic switch controller, MCU wake-up, GPIOs, and so on)
 - Fastest overcurrent protection method (less than 30 μ s from overcurrent event to detection and reaction triggering)
- Pyrotechnic switch controller (PSC)
 - Two independent controllers including driver stage
 - AK-LV16 and USCAR28 compliant
 - 1.2 A/2 ms or 1.75 A/0.5 ms driving capability per controller
 - Seemingly instantaneous triggering by the event manager without MCU processing
 - Extensive set of diagnostics (capacitor measurement, ESR measurement, igniter measurement, and so on)
- SPI controller interface and I²C controller interface to control peripherals
- MCU interface supporting SPI or isolated daisy-chain protocol TPL3
 - SPI (up to 4 Mbit/s)
 - TPL3 (2 Mbit/s, 62 nodes, transformer, or capacitive isolation)
- Power management
 - Direct supply from the pyrotechnic switch supply voltage
 - Redundant analog supplies
- Wake-up support (by communication, GPIO, or internal events)
- Supports ASIL D safety goals with redundant measurements, redundant signal processing, redundant pyrotechnic switch controller
- Unique device ID
- Thermally enhanced LQFP64-EP package with 0.5 mm pitch
- AEC-Q100 grade 1 qualification: Ta = -40 °C to 125 °C

3 Applications

Automotive:

- (Plug in) HEV battery management systems
- EV battery management systems

Industrial:

- Stationary energy storage system (ESS)
- Other current or voltage sense applications

4 Ordering information

This section describes the available part numbers.

Table 1. Part numbers

Part number	Communication	2 x 8 IOs	2 x ISENSE inputs	2 x VISENSE inputs	2 x pyrotechnic switch controllers
Full feature set					
MC33777BTA1AE	TPL	Yes	Yes	Yes	Yes
MC33777BSA1AE	SPI	Yes	Yes	Yes	Yes
Optimized feature set					
MC33779BTA1AE	TPL	Yes	Yes	No	Yes
MC33779BSA1AE	SPI	Yes	Yes	No	Yes
MC33778BTA1AE	TPL	Yes	Yes	No	PRM_PSC only
MC33778BSA1AE	SPI	Yes	Yes	No	PRM_PSC only
MC33776BTA1AE	TPL	Yes	Yes	No	No
MC33776BSA1AE	SPI	Yes	Yes	No	No

5 Block diagram

Figure 1 shows the general architecture of the MC33777B.

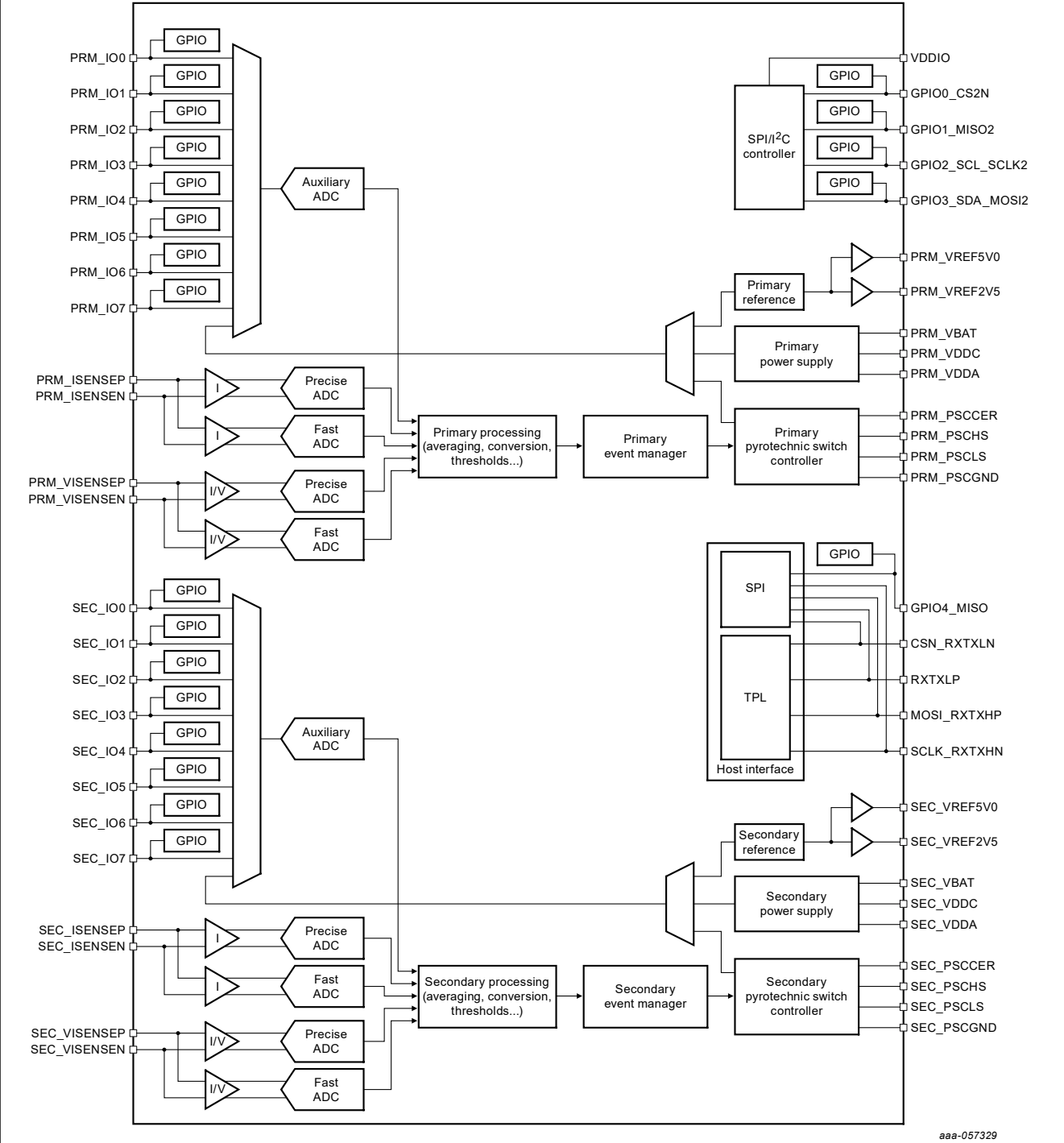


Figure 1. Block diagram

6 Pinning information

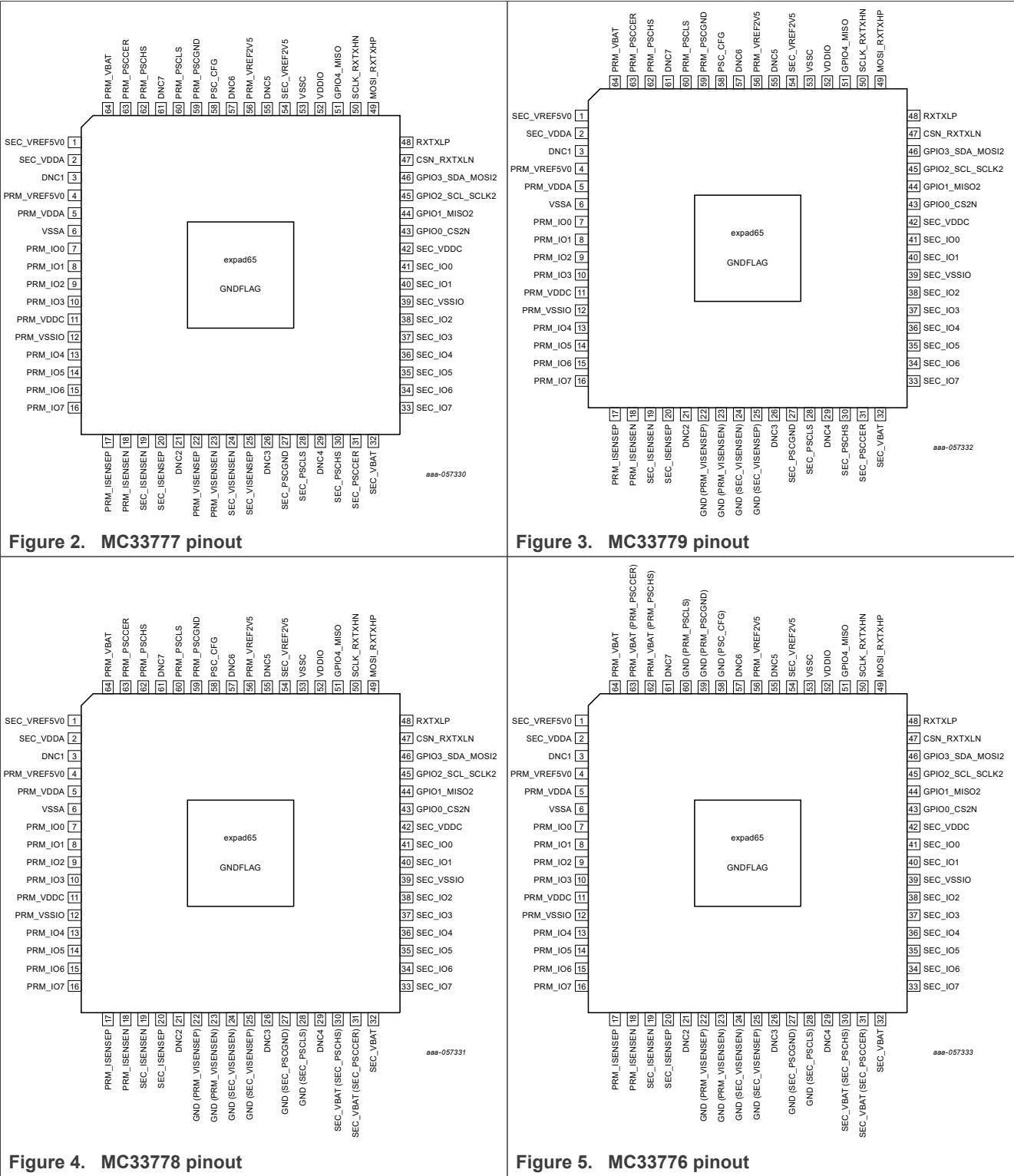


Table 2. Pinout LQFP64_EP*Ordered lists describe alternative functions.*

Symbol	Pin	Description
SEC_VREF5V0	1	Secondary 5 V reference voltage.
SEC_VDDA	2	Secondary internal analog supply.
DNC1	3	Do not connect. Keep floating in the application.
PRM_VREF5V0	4	Primary 5 V reference voltage.
PRM_VDDA	5	Primary internal analog supply.
VSSA	6	Internal analog ground reference.
PRM_IO0	7	<ul style="list-style-type: none"> Primary digital input/output 0. Primary analog measurement input 0.
PRM_IO1	8	<ul style="list-style-type: none"> Primary digital input/output 1. Primary analog measurement input 1.
PRM_IO2	9	<ul style="list-style-type: none"> Primary digital input/output 2. Primary analog measurement input 2.
PRM_IO3	10	<ul style="list-style-type: none"> Primary digital input/output 3. Primary analog measurement input 3.
PRM_VDDC	11	Primary VDDC supply output.
PRM_VSSIO	12	Primary IO ground reference and VDDD ground reference.
PRM_IO4	13	<ul style="list-style-type: none"> Primary digital input/output 4. Primary analog measurement input 4.
PRM_IO5	14	<ul style="list-style-type: none"> Primary digital input/output 5. Primary analog measurement input 5.
PRM_IO6	15	<ul style="list-style-type: none"> Primary digital input/output 6. Primary analog measurement input 6.
PRM_IO7	16	<ul style="list-style-type: none"> Primary digital input/output 7. Primary analog measurement input 7.
PRM_ISENSEP	17	Primary positive analog input for current measurement.
PRM_ISENSEN	18	Primary negative analog input for current measurement.
SEC_ISENSEN	19	Secondary negative analog input for current measurement.
SEC_ISENSEP	20	Secondary positive analog input for current measurement.
DNC2	21	Do not connect. Keep floating in the application.
PRM_VISENSEP	22	<ul style="list-style-type: none"> Primary positive analog input for current/voltage measurement. For MC33776, MC33778, and MC33779 connect to GND.
PRM_VISENSEN	23	<ul style="list-style-type: none"> Primary negative analog input for current/voltage measurement. For MC33776, MC33778, and MC33779 connect to GND.
SEC_VISENSEN	24	<ul style="list-style-type: none"> Secondary negative analog input for current/voltage measurement. For MC33776, MC33778, and MC33779 connect to GND.
SEC_VISENSEP	25	<ul style="list-style-type: none"> Secondary positive analog input for current/voltage measurement. For MC33776, MC33778, and MC33779 connect to GND.
DNC3	26	Do not connect. Keep floating in the application.
SEC_PSCGND	27	<ul style="list-style-type: none"> Secondary pyrotechnic switch controller ground. For MC33776 and MC33778 connect to GND.
SEC_PSCLS	28	<ul style="list-style-type: none"> Secondary pyrotechnic switch controller low-side switch input. For MC33776 and MC33778 connect to GND.
DNC4	29	Do not connect. Keep floating in the application.

Table 2. Pinout LQFP64_EP...continued*Ordered lists describe alternative functions.*

Symbol	Pin	Description
SEC_PSCHS	30	<ul style="list-style-type: none"> Secondary pyrotechnic switch controller high-side switch output. For MC33776 and MC33778 connect to SEC_VBAT
SEC_PSCCER	31	<ul style="list-style-type: none"> Secondary pyrotechnic switch controller capacitor. For MC33776 and MC33778 connect to SEC_VBAT
SEC_VBAT	32	Device supply voltage and secondary pyrotechnic switch controller charge input.
SEC_IO7	33	<ul style="list-style-type: none"> Secondary digital input/output 7. Secondar analog measurement input 7.
SEC_IO6	34	<ul style="list-style-type: none"> Secondary digital input/output 6. Secondar analog measurement input 6.
SEC_IO5	35	<ul style="list-style-type: none"> Secondary digital input/output 5. Secondar analog measurement input 5.
SEC_IO4	36	<ul style="list-style-type: none"> Secondary digital input/output 4. Secondar analog measurement input 4.
SEC_IO3	37	<ul style="list-style-type: none"> Secondary digital input/output 3. Secondar analog measurement input 3.
SEC_IO2	38	<ul style="list-style-type: none"> Secondary digital input/output 2. Secondar analog measurement input 2.
SEC_VSSIO	39	Secondary I/O ground reference.
SEC_IO1	40	<ul style="list-style-type: none"> Secondary digital input/output 1. Secondar analog measurement input 1.
SEC_IO0	41	<ul style="list-style-type: none"> Secondary digital input/output 0. Secondar analog measurement input 0.
SEC_VDDC	42	Secondary VDDC supply output.
GPIO0_CS2N	43	<ul style="list-style-type: none"> General-purpose logic input/output 0. SPI controller chip select output (CS2N).
GPIO1_MISO2	44	<ul style="list-style-type: none"> General-purpose logic input/output 1. SPI controller data input (MISO2).
GPIO2_SCL_SCLK2	45	<ul style="list-style-type: none"> General-purpose logic input/output 2. I²C controller clock input or output (SCL). SPI controller clock output (SCLK2).
GPIO3_SDA_MOSI2	46	<ul style="list-style-type: none"> General-purpose logic input/output 3. I²C controller data input or output (SDA). SPI controller data output (MOSI2).
CSN_RXTXLN	47	<ul style="list-style-type: none"> SPI target chip select input (CSN). TPL RX negative input from lower node. TPL TX negative output to lower node.
RXTXLP	48	<ul style="list-style-type: none"> TPL RX positive input from lower node. TPL TX positive output to lower node.
MOSI_RXTXHP	49	<ul style="list-style-type: none"> SPI target data input (MOSI). TPL RX positive input from upper node. TPL TX positive output to upper node.
SCLK_RXTXHN	50	<ul style="list-style-type: none"> SPI target clock input (SCLK). TPL RX negative input from upper node. TPL TX negative output to upper node.
GPIO4_MISO	51	<ul style="list-style-type: none"> SPI target data output (MISO). General-purpose logic input/output 4.

Table 2. Pinout LQFP64_EP...continued*Ordered lists describe alternative functions.*

Symbol	Pin	Description
VDDIO	52	External VDDIO supply input.
VSSC	53	VDDC ground reference.
SEC_VREF2V5	54	Secondary 2.5 V reference voltage.
DNC5	55	Do not connect. Keep floating in the application.
PRM_VREF2V5	56	Primary 2.5 V reference voltage.
DNC6	57	Do not connect. Keep floating in the application.
PSC_CFG	58	<ul style="list-style-type: none">Pyrotechnic switch controllers capacitor charging configuration pin.For MC33776 connect to GND.
PRM_PSCGND	59	<ul style="list-style-type: none">Primary pyrotechnic switch controller ground.For MC33776 connect to GND.
PRM_PSCLS	60	<ul style="list-style-type: none">Primary pyrotechnic switch controller low-side switch input.For MC33776 connect to GND.
DNC7	61	Do not connect. Keep floating in the application.
PRM_PSCHS	62	<ul style="list-style-type: none">Primary pyrotechnic switch controller high-side switch output.For MC33776 connect to PRM_VBAT.
PRM_PSCCER	63	<ul style="list-style-type: none">Primary pyrotechnic switch controller capacitor.For MC33776 connect to PRM_VBAT.
PRM_VBAT	64	<ul style="list-style-type: none">Device supply voltage and primary pyrotechnic switch controller charge input.
GNDFLAG	GNDFLAG	Grounded exposed pad.

7 Limiting values

Table 3. Limiting values

All voltages are defined relatively to the ground.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage and current ratings						
V_{BAT}	PRM_VBAT and SEC_VBAT input voltage	—	-0.3	—	35	V
V_{DDA}	PRM_VDDA and SEC_VDDA voltage	—	-0.3	—	1.65	V
V_{DDC}	PRM_VDDC and SEC_VDDC voltage	—	-0.3	—	5.5	V
V_{REF5V0}	PRM_VREF5V0 and SEC_VREF5V0 voltage	—	-0.3	—	5.5	V
V_{REF2V5}	PRM_VREF2V5 and SEC_VREF2V5 voltage	—	-0.3	—	3	V
$V_{I(IO)}$	General-purpose voltage measurement input voltage (PRM_IOx and SEC_IOx) (x = 0 to 7)	—	-0.3	—	5.5	V
$V_{I(GPIO)}$	Digital general-purpose input output (GPIO0_CS2N, GPIO1_MISO2, GPIO2_SCL_SCLK2, GPIO3_SDA_MOSI2, GPIO4_MISO)	—	-0.3	—	5.5	V
$V_{I(ISENSE)}$	PRM_ISENSEP, PRM_ISENSEN, SEC_ISENSEP, SEC_ISENSEN precision current measurement input voltage	—	-0.4	—	5.5	V
$V_{I(VISENSE)}$	PRM_VISENSEP, PRM_VISENSEN, SEC_VISENSEP, SEC_VISENSEN precision voltage and current measurement input voltage	—	-0.4	—	5.5	V
$V_{I(PSC)}$	PRM_PSCHS, PRM_PSCLS, SEC_PSCHS, and SEC_PSCLS voltage	—	-0.3	—	25	V
$V_{I(CER)}$	PRM_PSCCER and SEC_PSCCER voltage	—	-0.3	—	25	V
$V_{I(CFG)}$	PSC_CFG input voltage	—	-0.3	—	5.5	V
$I_{reverse(ccl)}$	Current from PRM_PSCCER to PRM_VBAT or from SEC_PSCCER to SEC_VBAT	Reverse current through the PSC charge current limiter diode in case of power loss	—	—	100	mA
$V_{I(DDIO)}$	VDDIO voltage	—	-0.3	—	5.5	V
$V_{bus(TPL)}$	Voltage on TPL communication bus pins (RXTXHP, RXTXHN, RXTXLP, RXTXLN)	—	-27	—	40	V
ESD ratings						
V_{ESD1}	Electrostatic discharge voltage	At any pin; human body model (HBM): according to AEC-Q100-002 (100 pF, 1.5 kΩ)	-2	—	2	kV
V_{ESD2}	Electrostatic discharge voltage	CSN_RXTXLN, RXTXLP, MOSI_RXTXHP, SCLK_RXTXHN	-4	—	4	kV
V_{ESD3-2}	Electrostatic discharge voltage	At all pins; charged device model (CDM): according to JEDEC JS-002-2018	-500	—	500	V
V_{ESD4-2}	Electrostatic discharge voltage	At corner pins; CDM: according to JEDEC JS-002-2018	-750	—	750	V
Thermal ratings						
T_j	Junction temperature	—	-40	—	150	°C
$T_{reflow(peak)}$	Peak reflow temperature	Pin soldering temperature limit is for 30 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.	—	—	260	°C
T_{stg}	Storage temperature	—	-55	—	150	°C

8 Revision history

Table 4. Revision history

Document ID	Release date	Description
MC3377B_PB	23 January 2026	Initial version

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