MC9S12C-Family
16-Bit Microcontroller

Based on Freescale’s market-leading flash technology, members of the MC9S12C-Family deliver the power and flexibility of our 16 Bit core (CPU12) family to a whole new range of cost and space sensitive, general purpose Industrial and Automotive network applications. MC9S12C-Family members are comprised of standard on-chip peripherals including a 16-bit central processing unit (CPU12), up to 128K bytes of Flash EEPROM or ROM, up to 4K bytes of RAM, an asynchronous serial communications interface (SCI), a serial peripheral interface (SPI), an 8-channel 16-bit timer module (TIM), a 6-channel 8-bit pulse width modulator (PWM), an 8-channel, 10-bit analog-to-digital converter (ADC) and up to one CAN 2.0 A, B software compatible module (MSCAN12). The MC9S12C-Family has full 16-bit data paths throughout. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. In addition to the I/O ports available in each module, up to 10 dedicated I/O port bits are available with Wakeup capability from STOP or WAIT mode. The MC9S12C-Family is available in 48-pin and 52-pin LQFP, and in 80-pin QFP packages (all RoHS Compliant J-STD-020C); the 80-pin version is pin-compatible with the HCS12B- and D-Family derivatives.

The C-Family includes ROM versions MC3S12C128/96/64/32/16 of all devices which provide a further cost reduction path for applications with high volume and stable code.

1 Features

- 16-Bit HCS12 CORE
  - HCS12 CPU
  - MMC (memory map and interface)
  - INT (interrupt control)
  - BDM (background debug mode)
  - DBG12 (enhanced debug12 module including breakpoints and change-of-flow trace buffer)
  - Multiplexed Expansion Bus (available only in 80-pin package version)
Features

• 16-Bit HCS12 CPU
  — Upward compatible with M68HC11 instruction set
  — Interrupt stacking and programmer’s model identical to M68HC11
  — Instruction queue
  — Enhanced indexed addressing

• Wake-up Interrupt Inputs
  — Up to 10-port bits available for wake up interrupt function

• Memory Options
  — 16K, 32K, 64K, 96K and 128K Byte Flash EEPROM (erasable in 512-byte sectors) or
  — 16K, 32K, 64K, 96K and 128K Byte ROM
  — 1K, 2K, and 4K Byte RAM

• Analog-to-Digital Converters
  — One 8-channel module with 10-bit resolution.
  — External conversion trigger capability

• Up to One 1M Bit Per Second, CAN 2.0 A, B Software Compatible Modules
  — Five receive and three transmit buffers
  — Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  — Four separate interrupt channels for receive, transmit, error and wake-up
  — Low-pass filter wake-up function
  — Loop-back for self test operation

• Timer Module (TIM)
  — 16-bit Counter with 7-bit Prescaler
  — 8 programmable input capture or output compare channels
  — Simple PWM Mode
  — Modulo Reset of Timer Counter
  — 16-Bit Pulse Accumulator
  — External Event Counting
  — Gated Time Accumulation

• 6 PWM Channels
  — Programmable period and duty cycle
  — 8-bit 6-channel or 16-bit 3-channel
  — Separate control for each pulse width and duty cycle
  — Center-aligned or left-aligned outputs
  — Programmable clock select logic with a wide range of frequencies
  — Fast emergency shutdown input
• **Serial Interfaces**
  — One asynchronous serial communications interface (SCI)
  — One synchronous serial peripheral interface (SPI)

• **CRG (Clock Reset Generator Module)**
  — Windowed COP watchdog,
  — Real time interrupt,
  — Clock monitor,
  — Clock generation
  — Reset Generation
  — Phase-locked loop clock frequency multiplier
  — Limp home mode in absence of external clock
  — Low power 0.5 to 16 MHz crystal oscillator reference clock

• **Operation Frequency**
  — 32MHz equivalent to 16MHz Bus Speed for single chip
  — 32MHz equivalent to 16MHz Bus Speed in expanded bus modes
  — Option: 50MHz equivalent to 25MHz Bus Speed
  — Internal 2.5V Regulator
  — Supports an input voltage range from 3.3V-10% to 5.5V
  — Low power mode capability
  — Includes low voltage reset (LVR) circuitry
  — Includes low voltage interrupt (LVI) circuitry

• **48-pin LQFP, 52-pin LQFP, or 80-pin QFP Package (all RoHS Compliant J-STD-020C)**
  — Up to 58 I/O lines with 5V input and drive capability
  — Up to 2 dedicated 5V input only lines (IRQ, XIRQ)
  — 5V A/D converter inputs and 5V I/O

• **Development Support**
  — Single-wire background debug™ mode (BDM)
  — On-chip hardware breakpoints
  — Enhanced DBG12 debug features
# MC9S12C-Family Members

## Table 1. List of MC9S12C-Family Members

<table>
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<tr>
<th>Flash</th>
<th>ROM</th>
<th>RAM</th>
<th>Package</th>
<th>Device</th>
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3 Pin Out Explanations

I/O is the sum of ports capable to act as digital input or output.

- For 80 Pin Versions:
  - Port A = 8, B = 8, E = 6 + 2 input only, J = 2, M = 6, P = 8, S = 4, T = 8, PAD = 8.
  - 12 inputs provide Interrupt capability (P = 8, J = 2, IRQ, XIRQ)

- For 52 Pin Versions:
  - Port A = 3, B = 1, E = 2 + 2 input only, M = 6, P = 3, S = 2, T = 8, PAD = 8.
  - 5 inputs provide Interrupt capability (P = 3, IRQ, XIRQ)

- For 48 Pin Versions:
  - Port A = 1, B = 1, E = 2 + 2 input only, M = 6, P = 1, S = 2, T = 8, PAD = 8.
  - 3 inputs provide Interrupt capability (P = 1, IRQ, XIRQ)
Figure 1. Block Diagram

Signals shown in **Bold** are not available on the 52 or 48 Pin Package

Signals shown in **Bold Italic** are available in the 52, but not the 48 Pin Package
5 User Configurable Memory Maps

The figure shows a useful map, which is not the map out of reset. After reset the map is:

- $0000 - $03FF: Register Space
- $0000 - $0FFF: 4K RAM (only 3K visible $0400 - $0FFF)
- Flash Erase Sector Size is 1024 Bytes

Figure 2. MCxS12C128 User Configurable Memory Map
The figure shows a useful map, which is not the map out of reset. After reset the map is:

- $0000 - $03FF: Register Space
- $0000 - $0FFF: 4K RAM (only 3K visible $0400 - $0FFF)

Flash Erase Sector Size is 1024 Bytes

**Figure 3. MCxS12C96 User Configurable Memory Map**
The figure shows a useful map, which is not the map out of reset. After reset the map is:

- $0000 - $03FF: Register Space
- $0000 - $0FFF: 4K RAM (only 3K visible $0400 - $0FFF)

Flash Erase Sector Size is 512 Bytes

**Figure 4. MCxS12C64 User Configurable Memory Map**
The figure shows a useful map, which is not the map out of reset. After reset the map is:

- $0000 - $03FF: Register Space
- $0800 - $0FFF: 2K RAM

Flash Erase Sector Size is 512 Bytes

**Figure 5. MCxS12C32 User Configurable Memory Map**
Figure 6. MCxS12C16 User Configurable Memory Map

The figure shows a useful map, which is not the map out of reset. After reset the map is:

- $0000 - $03FF: Register Space
- $0800 - $0FFF: 2K RAM

Flash Erase Sector Size is 512 Bytes
The figure shows a useful map, which is not the map out of reset. After reset the map is:

- $0000 - $03FF: Register Space
- $0C00 - $0FFF: 1K RAM

Flash Erase Sector Size is 512 Bytes

**Figure 7. MCxS12GC16 User Configurable Memory Map**
### 6 Pin Assignments

**Figure 8. Pin Assignments for 80-pin QFP for MC9S12C-Family**

!!! Pin-out is Subject to Change !!!

**MC9S12C-Family, Rev. 5**
**Pin Assignments**

* Signals shown in **Bold** are not available on the 48 Pin Package

**Figure 9. Pin Assignments for 52-pin LQFP for MC9S12C-Family**
Figure 10. Pin Assignments for 48-pin LQFP for MC9S12C-Family
7 Package Mechanical Information

Refer to the following pages for detailed package dimensions.
NOTES:


2. CONTROLLING DIMENSION: MILLIMETER.

3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.

5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE AC.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.

7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350.

8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.

9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
### NOTES


2. CONTROLLING DIMENSION: MILLIMETER.

3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4. DATUMS L, M, AND N TO BE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE T.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.48 MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OF PROTRUSION 0.07.

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DETAIL "A"

SECTION B-B
VIEW ROTATED 90°

DETAIL "C"
NOTES:

2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
   ▲ DIMENSIONS TO BE DETERMINED AT SEATING PLANE -C-.
   ▲ DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
   ▲ DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.