

QorIQ™ P1022/P1013

Energy-Efficient Communications Processor

Product Brief

The QorIQ™ P1022 is a new low-power, high-performance communications processor that combines a computation-intensive, super-scalar Power Architecture™ processor core with high-performance system peripherals and advanced power management techniques. It delivers high-performance computing in low-power envelopes required for media, communications, and industrial applications.

The integration of vector and double-precision floating point processing engines makes the P1022 ideal for mathematically- and data-intensive applications such as printing, imaging, and industrial computing. The P1022 offers audio and visual interfaces for a variety of media applications requiring a human-machine interface (HMI). Additionally, the P1022 is optimized for control and data-plane intensive processing applications, such as storage and data networks, where the benefits of processing and moving large amounts of data can be leveraged. The P1022 integrates SATA, USB, multi-lane PCI Express, Gigabit Ethernet, and DDR memory to increase data bandwidth at low power consumption.

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1 Application Examples

The following section provides block diagrams of different P1022 applications. The P1022 is a very flexible device and can be configured to meet many system application needs.

Both cores can operate in a symmetric multiprocessing mode to achieve higher performance, or they can run independent operating systems that each perform separate tasks. This flexibility enables application developers to assign distinct processing resources to distinct tasks that need guaranteed performance. For example, one core can manage a data plane and the other a control plane.

The value proposition of a dual-core device is further enhanced by a high degree of peripheral integration of system controllers such as DDR controllers. A device with faster internal buses can entirely replace the system controller where a discrete processor without integration was used previously.

The P1022 is primarily targeted to the following applications, which are described in further detail in this section:

- Multifunction printers supporting color print, scan, copy, fax, and LCD display with slow graphics
- Digital signage with audio and external video decode on Power PC
- Network attached storage with Raid5 support

1.1 Multifunction Printer Application

Figure 1 shows how to use an integrated dual-core device, such as the P1022, in a multifunction printer (MFP). The device interfaces to external ASICs, which perform scan, print, and control functions on the PCI Express. However, print functions such as PDL (page description language) parsing, rasterizing the page, resize, color format conversion, and half-toning are expected to be performed by the software running on the cores.

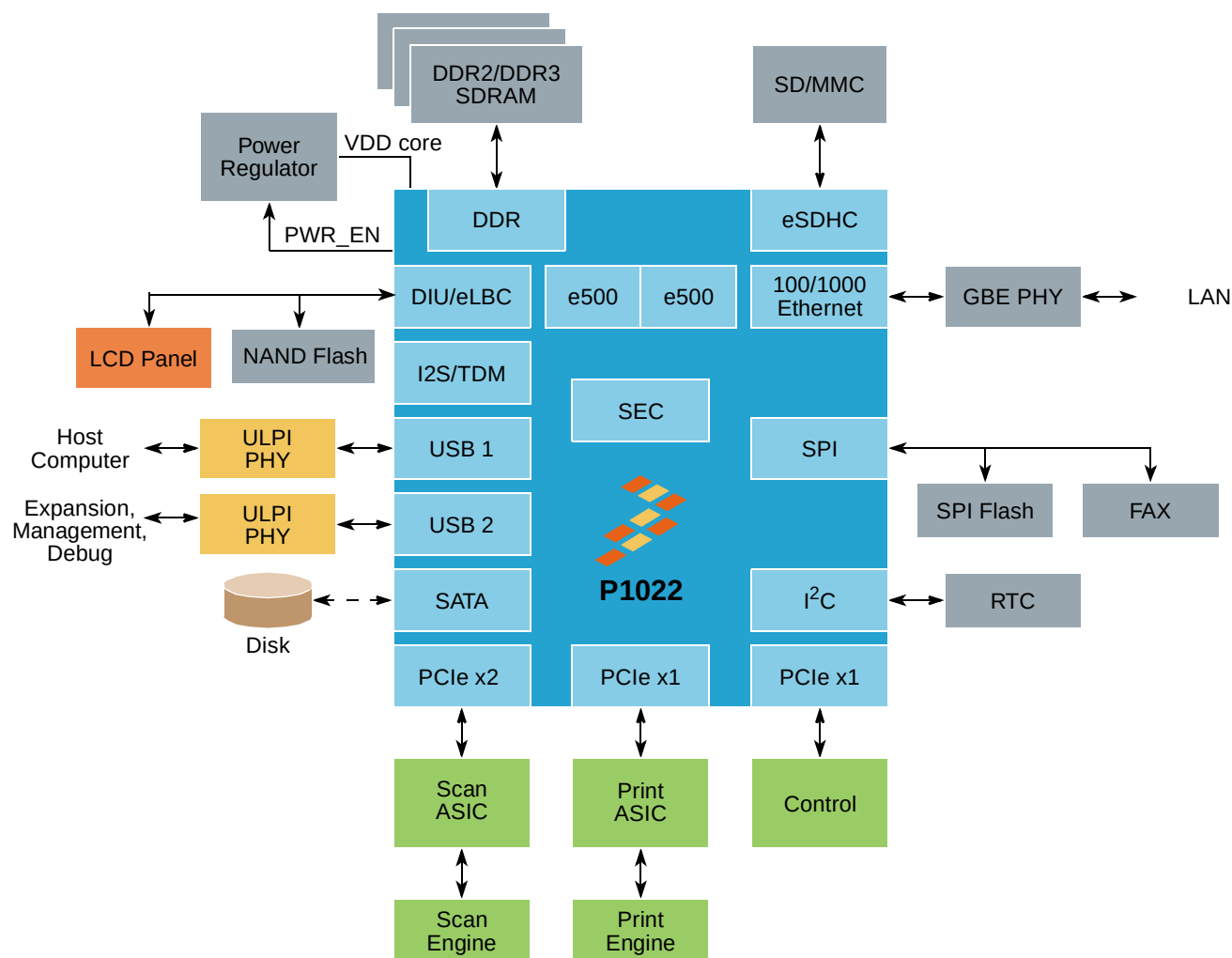


Figure 1. Multifunction Printer Application

An Ethernet port, supporting RMII, RGMII, and SGMII interfaces, is provided on the P1022. By combining the networking functions with the hardware security acceleration, line-speed secure throughput can be achieved.

The LCD interface, also called the display interface unit (DIU), on the MFP is driven by a glueless interface on the P1022. The DIU is designed for displaying graphics and slow-moving images, but not real-time video. These graphics on the LCD are composited by the software running on the CPU cores.

In this MFP application, one USB port acts as a USB device and connects to the external host computer; the other USB port can either act as a USB host to connect to devices such as a USB mouse or keyboard, or it can be available for management or debug. The MFP functions would be implemented as device functions on the USB port connected to the host computer.

Application Examples

For additional memory space, an external hard disk can be connected on the SATA interface. Print pages can be stored on the hard disk and printed at a later time, for example if the MFP has password security or for queueing print jobs.

Finally, the P1022 has external FAX ASIC support through the SPI and TDM interfaces. The P1022 has a 64-bit DDR interface and can boot from NOR, NAND, SPI, and SD/MMC devices.

1.2 Digital Signage Application

Figure 2 shows an example of a digital signage application. In this example, real-time video is decoded by the system built around the P1022. The actual video decoding, such as MPEG4 or H264, is performed by the ASICS connected to a PCI Express port.

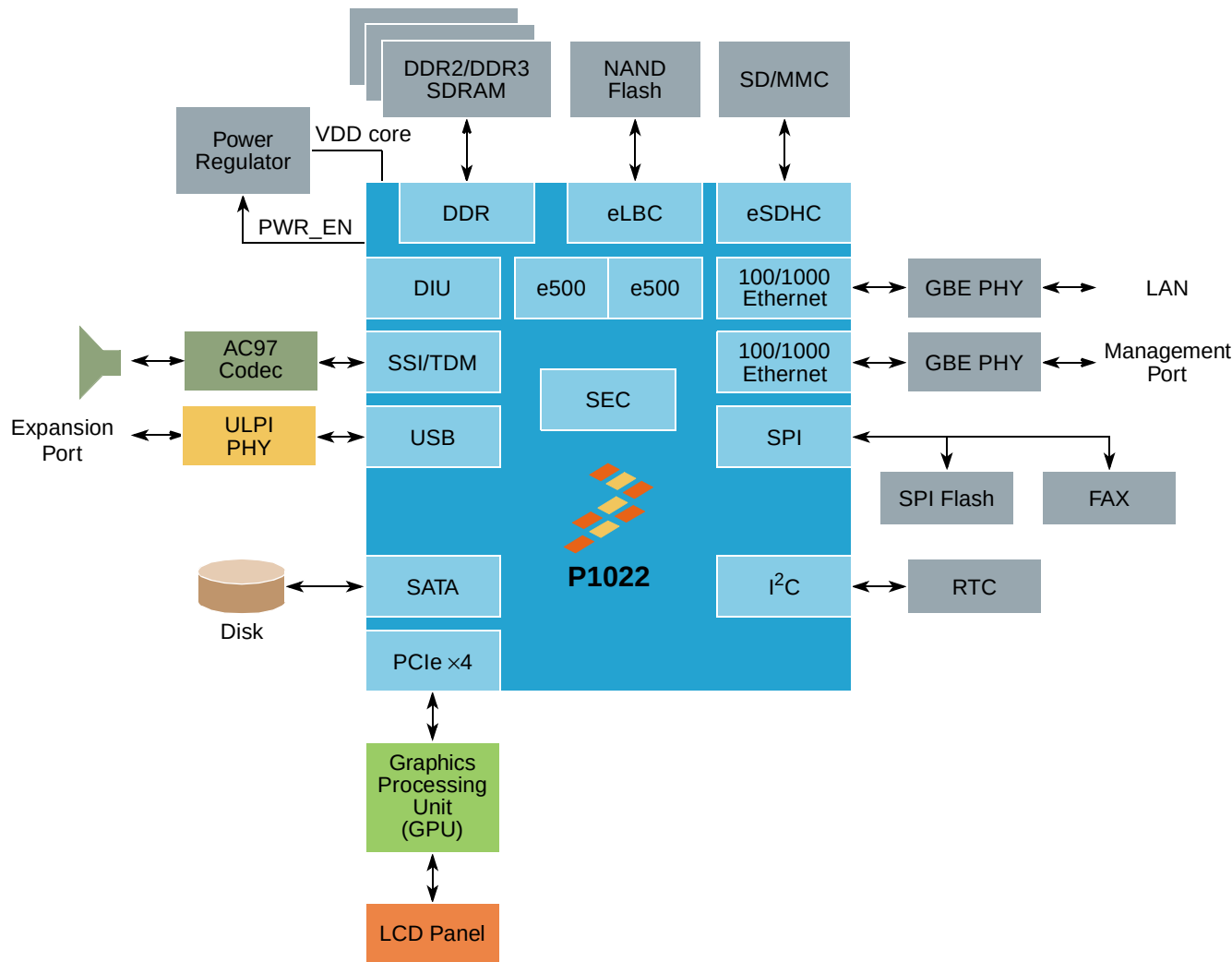


Figure 2. Digital Signage Application

Compressed video streams and overlay graphics information are streamed into a graphics processing unit (GPU) connected to one of the PCI Express ports. The GPU decodes the video stream and composes the raster with the overlay graphics to display the composed picture on the LCD panel.

For audio streaming, the audio decoding is performed on the P1022 CPU cores. The decoded audio samples are fed to an off-chip audio codec through the on-chip I2S interface, which converts the digital audio samples to analog signals, amplifies them, and feeds the audio signals to the speakers.

In this example, the P1022 acts as a USB host, where additional devices or a hub can be connected to a USB port of the digital signage box. Additionally, one of the Ethernet ports can be used for network connectivity to download the AV streams decoded and displayed. The secondary Ethernet port can be used for management.

An HDD can be connected to the SATA interface to house the encoded AV stream. Moreover, the P1022 supports a 64-bit DDR interface and can boot from NOR, NAND, SPI, and SD/MMC interfaces.

1.3 NAS/NVR Applications

Figure 3 shows an example of a network attached storage (NAS) or a network video recorder (NVR) application. The NAS/NVR application built around the P1022 can support two file systems, either with the same operating system or different operating systems running on each processor.

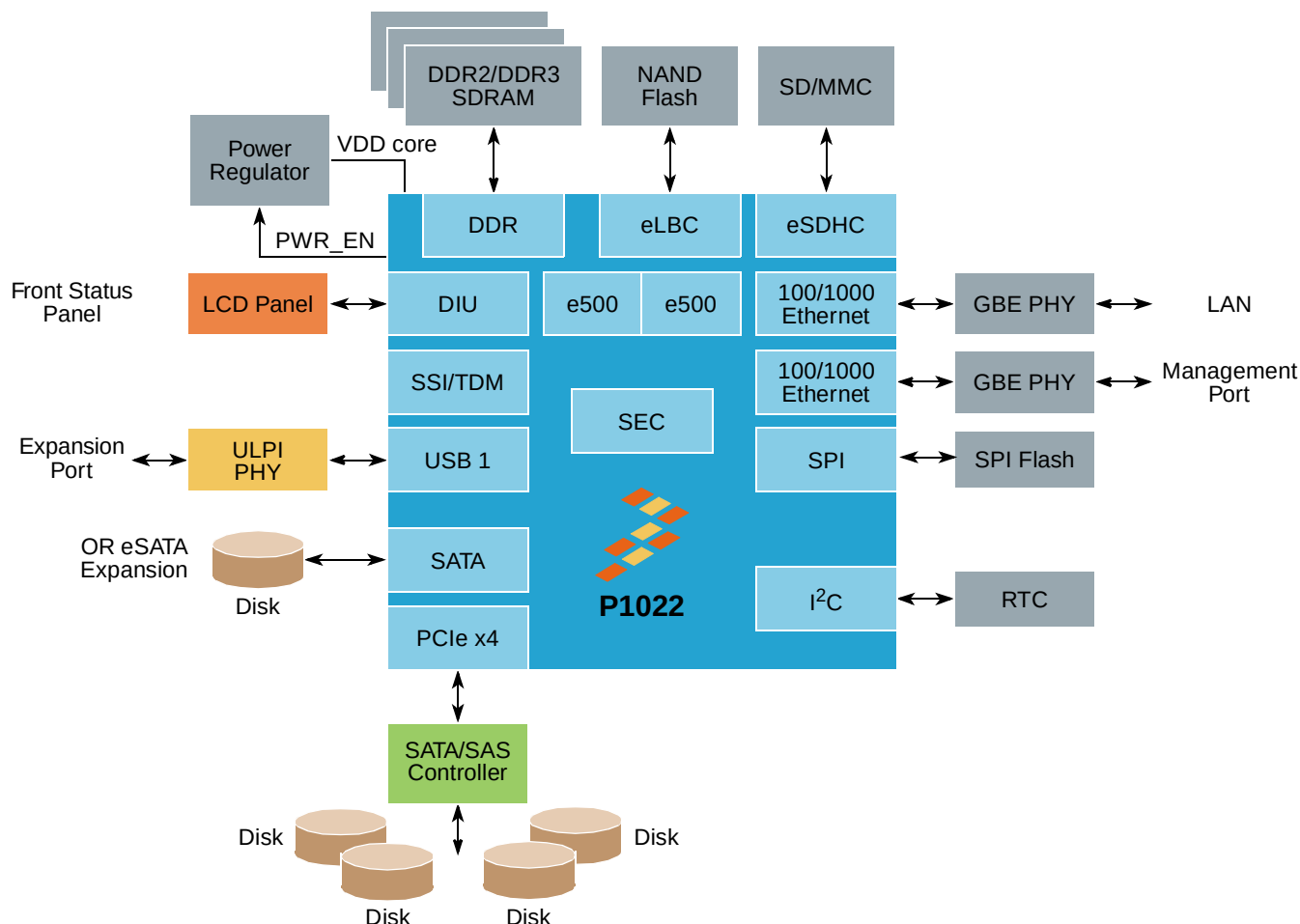


Figure 3. Network Attached Storage/Network Video Recorder Application

A hardware accelerator RAID5 acceleration is available on the P1022. Software can use the hardware assist for calculating parity. The RAID stack runs on either one or both of the cores, depending on the application. The software can also use the on-chip security hardware assist to support security functions. Additionally, the NAS/NVR application is a USB host, with the option to connect devices or hubs. Finally, the NAND Flash, DDR, and Ethernet interfaces have the same function as the previous applications for MFP and digital signage.

2 Features

This section describes the features of the P1022.

2.1 Block Diagram

Figure 4 shows the major functional units within the P1022/P1013.

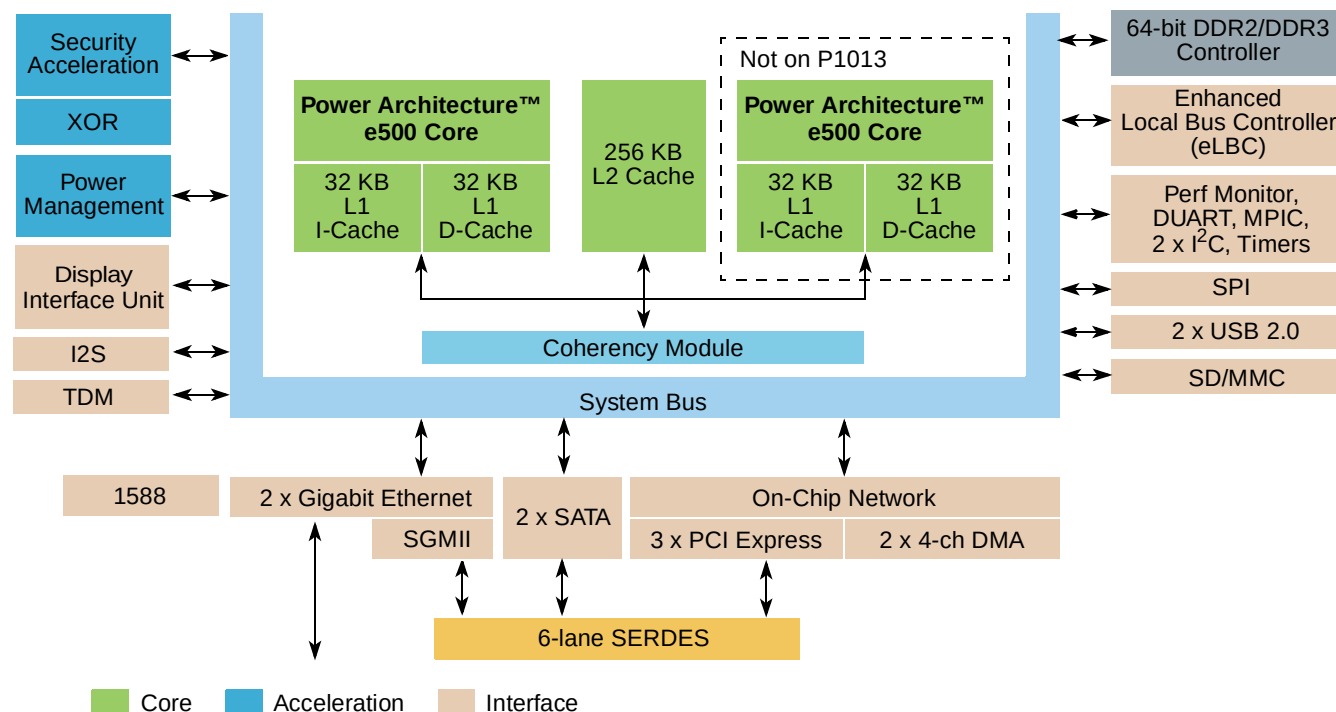


Figure 4. P1022 Block Diagram

2.2 Critical Performance Parameters

Critical performance parameters are as follows:

- e500v2 core frequency of up to 1066 MHz
- Typical power consumption of less than 3.0 W dual core and logic at 1 GHz core speed
- 45-nm SOI process technology
- Data rate of up to 800 Mbps/pin for DDR2 and DDR3
- Supply voltages as follows:
 - Ethernet: 2.5 V or 3.3 V (subject to protocol)
 - Enhanced local bus: 1.8 V, 2.5 V, 3.3 V
 - DDR: 1.8 V for DDR2, 1.5 V for DDR3 (conforms to JEDEC standard)
- Operating junction temperature (T_j) range: 0–125°C and –40–125°C (extended temperature)
- 31 × 31 mm 689-pin TEPBGA II (temperature-enhanced plastic BGA)

2.3 Chip-Level Features

Key features of the P1022 include:

- Dual (P1022) or single (P1013) high-performance Power Architecture e500v2 cores
 - 36-bit physical addressing
 - Double-precision floating-point support
 - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache for each core
 - 600 MHz to 1066 MHz core clock frequency
- 256-Kbyte L2 cache with ECC, also configurable as SRAM and stashing memory
- Two 10/100/1000 Mbps enhanced three-speed Ethernet controllers (eTSECs)
 - TCP/IP acceleration and classification capabilities
 - Support for the IEEE 1588™ standard
 - Lossless flow control
 - RMII, RGMII, SGMII
- High-speed interfaces (not all available simultaneously):
 - Six SerDes lanes running up to 2.5 GHz (multiplexed across controllers)
 - One ×4 and two ×1 PCI Express interfaces
 - Two serial ATA (SATA) interfaces
 - Two SGMII interfaces
- Audio Visual Interfaces
 - LCD interface supporting a display of 1280 × 1024P at 60 Hz, 24 bits per pixel
 - I2S interface with maximum sampling frequency of 192 Khz
 - VoIP TDM supporting up to 128 time slots
- Two high-speed USB controllers (USB 2.0)
 - Host and device support
 - Enhanced host controller interface (EHCI)
 - ULPI interface to PHY
- Enhanced secure digital host controller (SD/MMC)
- Serial peripheral interface
- Integrated security engine (SEC) with XOR acceleration
- 64-bit DDR2/DDR3 SDRAM memory controller with ECC support
- Programmable interrupt controller (PIC) compliant with Open-PIC standard
- Dual four-channel DMA controllers
- Dual I²C controllers, DUART, timers
- Enhanced local bus controller (eLBC)
- TDM interface supporting up to 128 channels

- Up to 87 general-purpose I/O or O signals
- Advanced power and energy management controller, supporting run, jog, doze, nap, sleep, and packet-lossless deep sleep modes

These features are described in greater detail in subsequent sections.

NOTE

The P1022 is also available without a security engine. All specifications other than those relating to security apply to the non-security version exactly as described in this document.

2.4 Module Features

This section contains a high-level view of the P1022 architecture.

2.4.1 e500v2 Cores and Memory Unit

The P1022 contains two high-performance 32-bit e500v2 cores that implement the Power Architecture. In addition to 36-bit physical addressing, this version of the e500 core includes:

- SPE double-precision floating-point instruction set using 64-bit operands
- SPE embedded vector and scalar single-precision floating-point instruction set using 32- or 64-bit operands
- 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection

The device also contains 256 Kbytes of L2 cache/SRAM, as follows:

- Eight-way set-associative cache organization with 32-byte cache lines
- Flexible configuration (can be configured as part cache, part SRAM)
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing)
- SRAM features include the following:
 - I/O devices access SRAM regions by marking transactions as snooperable (global)
 - Regions can reside at any aligned location in the memory map
 - Byte-accessible ECC uses read-modify-write transaction accesses for smaller-than-cache-line accesses

2.4.2 e500 Coherency Module (ECM) and Address Map

The e500 coherency module (ECM) provides a mechanism for I/O-initiated transactions to snoop the bus between the e500v2 cores and the integrated L2 cache in order to maintain coherency across local cacheable memory. It also provides a flexible switch-type structure for core- and I/O-initiated transactions to be routed or dispatched to target modules on the device.

The P1022 supports a flexible 36-bit physical address map. Conceptually, the address map consists of local space and external address space. The local address map is supported by 12 local access windows that define mapping within the local 36-bit (64-Gbyte) address space.

The P1022 can be made to be part of a larger system address space through the mapping of translation windows. This functionality is included in the address translation and mapping units (ATMUs). Both inbound and outbound translation windows are provided. The ATMUs allows the P1022 to be part of larger address maps, such as those of PCI Express.

2.4.3 Integrated Security Engine (SEC)

The SEC 3.0 offloads computationally intensive security functions, such as key generation and exchange, authentication, and bulk encryption from the processor cores of the P1022. It is optimized to process all cryptographic algorithms associated with IPsec, IKE, SSL/TLS, iSCSI, SRTP, IEEE Std. 802.11i™, 3G, A5/3 for GSM and EDGE, and GEA3 for GPRS. The SEC 3.0 derives from integrated security cores in other members of the PowerQUICC family, including the SEC 2.1 in the MPC8548E and the SEC 1.0 in the MPC8272E.

Components of the SEC are as follows:

- XOR engine for parity checking in RAID storage applications. Also, the exclusive OR (XOR) operation to generate parity data in RAID applications can be accelerated. XOR operations use SEC descriptors and offload both parity generation and data movement from the e500 core.
- Four crypto-channels, each supporting multi-command descriptor chains.
- Eight cryptographic execution units:
 - Advanced Encryption Standard unit (AESU)
 - ARC four execution unit (AFEU)
 - Cyclic redundancy check accelerator (CRCA)
 - Data Encryption Standard execution unit (DEU)
 - Kasumi execution unit (KEU)
 - Message digest execution unit (MDEU)
 - Public key execution unit (PKEU)
 - Random number generator (RNGB)

2.4.4 Enhanced Three-Speed Ethernet Controllers (eTSECs)

The P1022 has two on-chip enhanced eTSECs. The eTSECs incorporate a media access control (MAC) sublayer that supports 10- and 100-Mbps and 1-Gbps Ethernet/802.3 networks with RMII, RGMII, and SGMII physical interfaces. The eTSECs include 2-Kbyte receive and 10-Kbyte transmit DMA functions.

The P1022 eTSECs support programmable CRC generation and checking, RMON statistics, and jumbo frames of up to 9.6 Kbytes. Frame headers and buffer descriptors can be forced into the L2 cache to speed classification or other frame processing. They are designed to comply with IEEE Std. 802.3™, 802.3u, 802.3x, 802.3z, 802.3ac, and 802.3ab. Each eTSEC provides hardware support for accelerating TCP/IP packet transmission and reception.

Key features of these controllers include:

- Flexible configuration for multiple PHY interface configurations. The SGMII interface is available for any combination of eTSECs, regardless of the configuration of any other eTSEC.
- TCP/IP acceleration and QoS features:
 - IP v4 and IP v6 header recognition on receive
 - IP v4 header checksum verification and generation
 - TCP and UDP checksum verification and generation
 - Per-packet configurable acceleration
 - Recognition of VLAN, stacked (queue in queue) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
 - Transmission from up to eight physical queues
 - Reception to up to eight physical queues
- Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex)
 - IEEE Std. 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
- IEEE Std. 802.1 virtual local area network (VLAN) tags and priority
- VLAN insertion and deletion
 - Per-frame VLAN control word or default VLAN for each eTSEC
 - Extracted VLAN control word passed to software separately
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition
- Ability to force allocation of header information and buffer descriptors into L2 cache
- Enhanced for wake-up from deep sleep

2.4.4.1 IEEE 1588 Integration

The eTSEC's IEEE 1588 integration allows extremely precise clock synchronization, with accuracy in the sub-microsecond range. This precision is achieved using regular Ethernet connectivity with standard Ethernet frames.

Benefits of the IEEE 1588 protocol include:

- Rapid convergence to sub-microsecond time synchronization between heterogeneous devices with different clocks, resolution, and stability
- Automatic configuration and segmentation
- Very simple configuration and operation with low computation resource and bandwidth consumption

2.4.5 High-Speed Interface Blocks (SerDes)

The P1022 offers two high-speed SerDes interface blocks. These blocks, offering a total of six SerDes lanes, are connected to the SGMII, PCI Express, and SATA interfaces.

Features

The four-lane SerDes allows use of the three PCI Express controllers and SGMII. One of the configurations in [Table 1](#) can be selected during power-on reset.

Table 1. Supported SerDes 1 Configurations

Signal/Lane				Max Gbaud per Lane			
0	1	2	3	0	1	2	3
SGMII	SGMII	PEX ×1	PEX ×1	1.25	1.25	2.5	2.5
SGMII	SGMII	PEX ×2		1.25	1.25	2.5	2.5
SGMII	PEX ×1	PEX ×1	PEX ×1	1.25	2.5	2.5	2.5
PEX ×2		PEX ×1	PEX ×1	2.5	2.5	2.5	2.5
PEX ×2		PEX ×2		2.5	2.5	2.5	2.5
PEX ×4				2.5	2.5	2.5	2.5

The two-lane SerDes allows use of the PCI Express, the SATA controllers, or the SGMII interfaces of the eTSEC controllers (selected at power-on reset). Both lanes must be either SATA or SGMII. One of the configurations in [Table 2](#) can be selected during power-on reset.

Table 2. Supported SerDes 2 Configurations

Signal/Lane		Max Gbaud per Lane	
0	1	0	1
PEX ×1	PEX ×1	2.5	2.5
PEX ×2		2.5	2.5
SATA ×1	SATA ×1	1.5/3.0	1.5/3.0
SGMII	SGMII	1.25	1.25

2.4.6 Display Interface Unit (DIU)

The DIU is a display controller designed to handle TFT LCD displays. The DIU does not have internal frame buffers; it reads the data from main memory at the same rate at which it refreshes the display. Besides generating all the signals required to drive the display, the DIU handles the real-time blending of up to three planes onto the display. Alpha blending is performed between the planes. Chroma key support is also present to help relieve the host processor from all the very computational and bandwidth-consuming blending tasks while simultaneously allowing the users to maintain the graphics quality required by many applications.

2.4.7 Synchronous Serial Interface (SSI)

The synchronous serial interface (SSI) is a full-duplex, serial port that allows the chip to communicate with a variety of serial devices. These serial devices can be standard coder-decoder (codecs), digital signal processors (DSPs), microprocessors, peripherals, and popular industry audio codecs that implement the inter-IC sound bus standard (I²S) and Intel AC97 standard.

2.4.8 Universal Serial Bus (USB) 2.0

The P1022 USB 2.0 controller provides point-to-point connectivity complying with the *Universal Serial Bus Revision 2.0 Specification*. The USB controller can be configured to operate as a stand-alone host, stand-alone device, or both host and device functions operating simultaneously. The host and device functions are configured to support the following types of USB transfers:

- Bulk
- Control
- Interrupt
- Isochronous

The USB 2.0 controller supports the following:

- USB dual-role operation and configurability as host or device
- Operation as a stand-alone USB device supporting the following
 - One upstream facing port
 - Six programmable USB endpoints
- Operation as a stand-alone USB host controller supporting the following
 - USB root hub with one downstream-facing port
 - Compatibility with enhanced host controller interface (EHCI)
- High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- External PHY with UTMI+ low-pin interface (ULPI)

2.4.9 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the device to exchange data between other PowerQUICC family devices, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit. It has the ability to boot from an SPI serial flash device.

The SPI receiver and transmitter each have a FIFO of 32 bytes to support more efficient transfers to and from SPI devices. The SPI interface supports high-speed devices with full clock cycle operation, as well as devices which support two bits in parallel for reads.

2.4.10 DDR SDRAM Controller

The P1022 supports DDR2 and DDR3 SDRAM. The memory interface controls main memory accesses and provides for a maximum of 8 Gbytes of main memory.

The P1022 supports a variety of SDRAM configurations. SDRAM banks can be built using DIMMs or directly-attached memory devices. Sixteen multiplexed address signals provide for device densities from 64 Mbits to 8 Gbits. Four chip-select signals support up to four banks of memory. The P1022 supports

Features

bank sizes from 8 Gbytes to 32 Gbytes. Nine column address strobes ($\overline{\text{MDM}}[0:8]$) are used to provide byte selection for memory bank writes.

The P1022 can be configured to retain the currently active SDRAM page for pipelined burst accesses. Page mode support of up to 32 simultaneously open pages can dramatically reduce access latencies for page hits. Depending on the memory system design and timing parameters, using page mode can save 3 to 4 clock cycles from subsequent burst accesses that hit in an active page.

Using ECC, the P1022 detects and corrects all single-bit errors and detects all double-bit errors and all errors within a nibble.

The P1022 can invoke a level of system power management by asserting the MCKE SDRAM signal on-the-fly to put the memory into a low-power sleep mode.

The P1022 offers both hardware and software options to support battery-backed main memory. In addition, the DDR controller offers an initialization bypass feature which system designers may use to prevent re-initialization of main memory during system power-on following abnormal shutdown.

2.4.11 Power Management Controller (PMC)

The P1022 is designed for low power consumption benefitting equipment manufacturers wishing to support ENERGY STAR standards. Dynamic power management locally minimizes power consumption in the doze, nap, or sleep modes. Additional static power saving can be accomplished by using deep sleep mode.

A jog mode feature is provided on the P1022. In jog mode, the e500 core frequency can be adjusted dynamically while the platform frequency remains unchanged, resulting in optimal device temperature and power dissipation.

The power management controller (PMC) is responsible for maintaining the device in various low power modes. The PMC has the following features:

- Low standby power
- Jog mode support—Adjusts core frequency to optimize power consumption
- Support for dynamic and static power management to minimize power consumption of idle blocks:
 - Doze, nap, and sleep modes for dynamic power management
 - Packet-lossless deep sleep mode for static power management
- PMC wake on: filtered LAN activity, USB connection, GPIO, internal timer, or external interrupt event

2.4.12 PCI Express Interfaces

The P1022 supports three PCI Express interfaces designed to comply with the *PCI Express Base Specification Revision 1.0a*. They are configurable at boot time to act as either root complex or endpoint.

The physical layer of the PCI Express interface operates at a transmission rate of 2.5 Gbaud (data rate of 2.0 Gbps) per lane. The theoretical unidirectional peak bandwidth is 2 Gbps per lane. Receive and transmit ports operate independently, resulting in an aggregate theoretical bandwidth of 4 Gbps per lane.

Other features of the PCI Express interface include:

- Support for one of the following configurations:
 - One $\times 4$ and two $\times 1$
 - One $\times 2$ and two $\times 1$
 - Three $\times 2$
 - Three $\times 1$
- Both 32- and 64-bit addressing and 256-byte maximum payload size
- Full 64-bit decode with 36-bit wide windows
- Inbound INTx transactions
- Message signalled interrupt (MSI) transactions

2.4.13 Serial ATA (SATA) Controllers

The SATA controllers have the following features:

- Support for host SATA I per spec Rev 1.0a
 - OOB
 - Port multipliers
 - ATAPI 6+
 - Spread spectrum clocking on receive
- Support for SATA II extensions
 - Asynchronous notification
 - Hot plug including asynchronous signal recovery
 - Link power management
 - Native command queuing
 - Staggered spin-up and port multiplier support
- Support for SATA I and II data rates (1.5 & 3.0 Gbaud)
- Standard ATA master-only emulation
- Includes ATA shadow registers
- Implements SATA superset registers (SError, SControl, SStatus)
- Interrupt driven
- Power management support
- Error handling and diagnostic features
 - Far end/near end loopback
 - Failed CRC error reporting
 - Increased ALIGN insertion rates
 - Scrambling and CONT override

2.4.14 Programmable Interrupt Controller (PIC)

The P1022 PIC implements the logic and programming structures of the OpenPIC architecture, providing for external interrupts (with fully nested interrupt delivery), message interrupts, internal-logic driven interrupts, and global high-resolution timers. Up to 16 programmable interrupt priority levels are supported. The PIC can be bypassed to allow use of an external interrupt controller.

2.4.15 Enhanced SD Host Controller (eSDHC)

The eSDHC provides an interface between the host system and memory cards such as MultiMediaCard (MMC) and secure digital (SD) card. The eSDHC acts as a bridge, passing host bus transactions to SD/MMC cards by sending commands and performing data accesses to or from the cards.

The eSDHC includes the following features:

- SD bus clock frequency up to 50 MHz
- Supports 1-/4-bit SD modes, 1-/4-/8-bit MMC modes
 - Up to 200 Mbps data transfer for SD/MMC cards, using 4 parallel data lines
- Supports single- and multi-block read and write
- Supports write protection switch for write operations
- Supports synchronous and asynchronous abort
- Supports pause during the data transfer at a block gap
- Supports Auto CMD12 for multi-block transfer
- Host can initiate non-data transfer commands while the data transfer is in progress
- Embodies a fully configurable 128×32 -bit FIFO for read/write data
- Supports internal DMA capabilities

2.4.16 Time Division Multiplexing (TDM) Interface

The TDM interface supports the following features:

- Independent receive and transmit with dedicated data, clock and frame sync line
- Separate or shared RCK and TCK whose source can be either internal or external
- Glueless interface to E1/T1 frames and MVIP, SCAS, and H.110 buses
- Up to 128 time slots, where each slot can be programmed to be active or inactive
- 8- or 16-bit word widths
- The TDM transmitter sync signal (TFS), transmitter clock signal (TCK) and receiver clock signal (RCK) configurable as either input or output
- Frame sync and data signals programmable for sampling either on the rising edge or on the falling edge of the clock
- Frame sync programmable as active low or active high
- MSB or LSB first support

2.4.17 DMA, I²C, DUART, and eLBC

The P1022 provides two integrated four-channel DMA controllers, which can transfer data between any of its I/O or memory ports or between two devices or locations on the same port. The DMA controller can be used as follows:

- To chain (both extended and direct) through local memory-mapped chain descriptors.
- To handle misaligned transfers as well as stride transfers and complex transaction chaining.
- To specify local attributes such as snoop and L2 write stashing.

There are two I²C controllers. These synchronous, multimaster buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. Both the transmitter and receiver support 16-byte FIFOs.

The P1022 enhanced local bus controller (eLBC) port allows connection with a wide variety of external memories, DSPs, and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The user programmable machine (UPM) can be programmed to interface with synchronous devices or custom ASIC interfaces. The NAND Flash control machine (FCM) further extends interface options. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM, UPM, or FCM controller. All may exist in the same system. The local bus controller supports the following features:

- Multiplexed 32-bit address and data bus operating at 66 MHz
- Four chip selects support four external slaves
- Up to eight-beat burst transfers
- 16- and 8-bit port sizes controlled by on-chip memory controller
- Three protocol engines available on a per-chip-select basis
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- FCM supports NAND Flash, GPCM supports NOR Flash

2.4.18 Device Boot Locations

The P1022 may be configured to boot using one of the following interfaces:

- DDR2/DDR3 memory controller
- Any PCI Express interface
- Enhanced local bus interface (using the GPCM or FCM)
- I²C boot sequencer (I²C1 interface)
- SPI flash
- SD/MMC flash

2.4.19 System Performance Monitor

The performance monitor facility supports eight 32-bit counters that can count up to 512 counter-specific events. It supports duration and quantity threshold counting and a burstiness feature that permits counting of burst events with a programmable time between bursts.

3 Development Environment

Development tools, hardware platforms, software building blocks and application-specific software solutions are available from Freescale and the Freescale Alliance Program, including third party protocol and signaling stack suppliers, real-time operating systems support and a variety of applications software support. All of this builds upon the existing industry standard PowerQUICC family support program.

4 Document Revision History

[Table 3](#) provides a revision history for this product brief.

Table 3. Document Revision History

Rev. No.	Date	Substantive Change(s)
0	9/2009	Initial Release

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