FS26

Safety System Basis Chip with Low Power for ASIL D /ASIL B

Rev. 1 — 13 September 2021 Product brief

1 About this document

This Product brief is intended to provide overview/summary information for the purpose of evaluating a product for design suitability. It is intended for quick reference only and should not be relied upon to contain detailed and full information.

Some of the content in this product brief is extracted from the product's full data sheet. In case of any inconsistency or conflict, the full data sheet shall prevail.

For detailed and full information, see the relevant FS26 full data sheet, available via the NXP DocStore at https://www.docstore.nxp.com.

2 General description

The FS26 is a family of automotive Safety SBC devices with multiple power supplies designed to support entry and mid-range safety microcontrollers like S32K3 series while maintaining flexibility to fit other microcontrollers targeting automotive electrification such as power train, chassis, safety, and low-end gateway applications.

This family of devices is comprised of several versions, pin to pin and software compatible, to support a wide range of applications, offering choice in number of output rails, output voltage settings, operating frequency, power up sequencing and integrated system level features to address multiple applications with Automotive Safety Integrity Levels (ASIL) B or D.

FS26 features multiple switch mode regulators as well as LDO voltage regulators to supply the microcontroller, sensors, peripheral ICs and communication interfaces. FS26 offers a high precision voltage reference available to the system as well as reference voltage for two independent voltage tracking regulators, various functionalities for system control and diagnostics such as Analog multiplexer, GPIOS and Selectable wake up events from I/O, Long Duration Timer or SPI communication.

The FS26 is developed in compliance with the ISO 26262 standard and includes enhanced safety features with multiple fail-safe outputs, becoming a full part of a safety-oriented system partitioning, covering both ASIL B and ASIL D safety integrity levels, with latest on-demand latent fault monitoring.

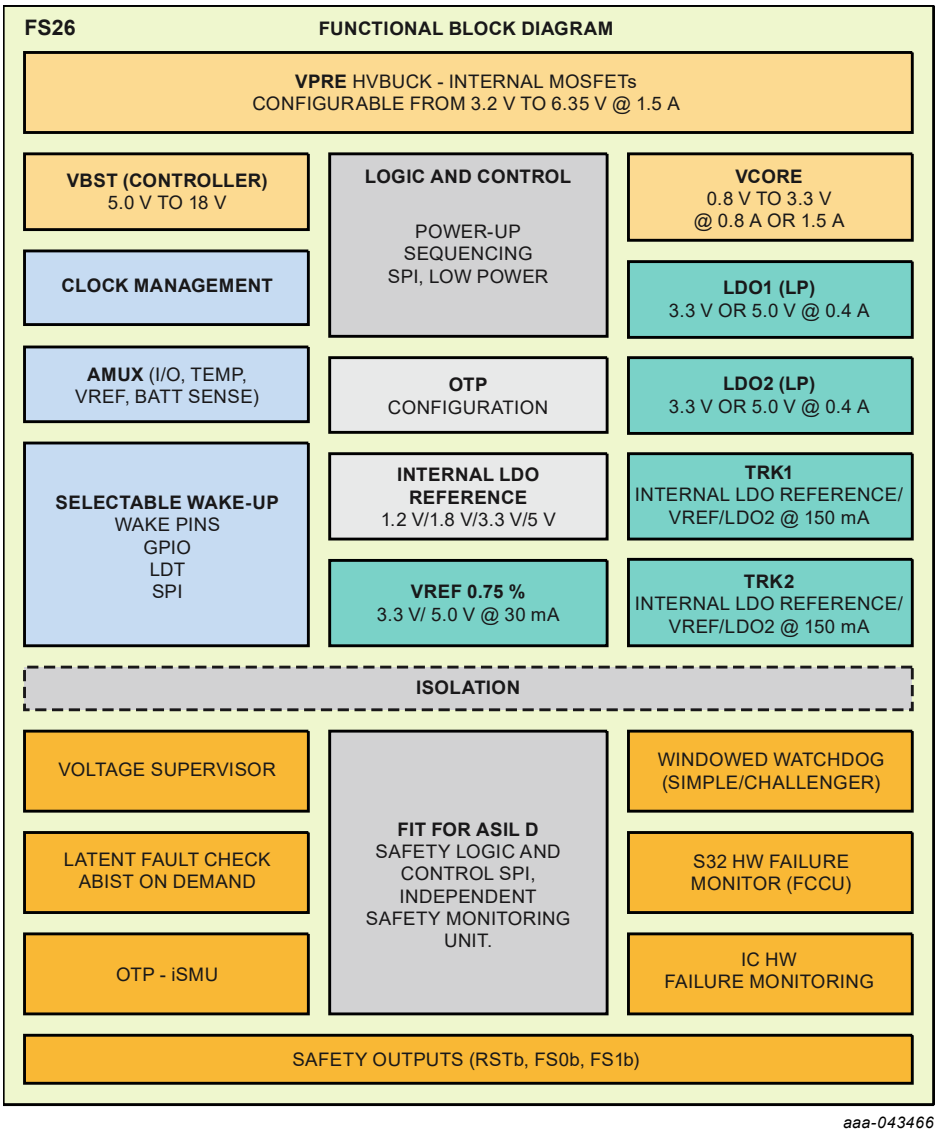


Figure 1. Functional block diagram

3 Features and benefits

Operating range:

- 40 V DC maximum input voltage
- Support operating voltage range down to battery 3.2 V with the BOOST
- Support operating voltage range down to battery 6.0 V without the BOOST
- Low-power OFF mode with 30 µA quiescent current
- Low-power Standby mode with 25 µA quiescent current with VPRE active. LDO1 or LDO2 activation selectable via OTP configuration.

Power supplies:

- VPRE: synchronous buck converter with integrated FETs. Configurable output voltage and switching frequency, output DC current capability up to 1.5 A and PFM mode for Low-power Standby mode operation.

- VCORE: synchronous buck converter with integrated FETs. VCORE is dedicated for microcontroller core supply. Output DC current up to 0.8 A or 1.5 A (depending on part number), output voltage range setting from 0.8 V to 3.3 V.
- VBST: asynchronous boost controller with external low side switch, diode and current sense resistor. VBST is configurable as front-end supply to withstand low voltage cranking profiles or in back-end supply with configurable output voltage and scalable output DC current capability.
- LDO1: LDO regulator for microcontroller I/O support with selectable output voltage between 3.3 V and 5.0 V and up to 400 mA current capability.
- LDO2: LDO regulator for system peripheral support with selectable output voltage between 3.3 V and 5.0 V and up to 400 mA current capability.
- VREF: high precision reference voltage with 0.75 % accuracy for external ADC reference and internal tracking reference.
- TRK1 and TRK2: voltage tracking regulators with selectable output voltage between VREF, LDO2 or Internal LDO reference. Support high-voltage protection for ECU off board operation. Each tracker has a current capability up to 150 mA.

System support:

- Two wake-up inputs with high-voltage support for system robustness
- Two programmable GPIO with wake-up capability or HS/LS driver
- Programmable long duration timer (LDT) for system shutdown and wake-up control
- System voltage monitoring (including battery voltage monitoring) through the Analog Multiplexer
- Selectable wake-up sources from: WAKE/GPIO pins, LDT or SPI activity
- Device control via 32 bits SPI interface with CRC

Compliance:

- EMC optimization techniques on switching regulators including spread spectrum, slew rate control and manual frequency tuning
- EMI robustness supporting various automotive EMI test standards

Functional Safety:

- Scalable portfolio from Automotive Safety Integrity Levels (ASIL) B to D
- Independent monitoring circuitry, dedicated interface for microcontroller monitoring, simple and challenger watchdog function
- Analog Built-In Self-Test (ABIST) and Logical Built-In Self-Test (LBIST) at start-up
- Analog Built-In Self-Test (ABIST) on demand
- Safety outputs with latent fault detection mechanism (RSTB, FS0B, FS1B)

Configuration and enablement:

- LQFP48 pins with exposed pad for optimized thermal management
- Permanent device customization via One-Time-Programming (OTP) fuse memory
- OTP emulation mode for system development and evaluation

4 Applications

- xEV and Powertrain market (Inverter, OBC, DCDC, BMS, BSG)
- Body market (Gateway, Zonal control, Body controller, Smart Junction Box)
- Safety and Chassis (Suspension, Power Steering)

- MCU attach (NXP S32K3 family, Infineon Aurix family (TC2x and TC3x), Renesas RH850 family, Cypress Traveo family)

5 Ordering information

M		FS		26 X Y		A		M		Zzz		AD	
Release type		**Family**		**Product core**		**Release version**		**Temperature**		**Funct. or Param. variant**		**Package**	
M	Production	FS	High-voltage power management	2600-2633	Core	A	initial release	M	−40 °C to 125 °C	Blank	if not required	AD	LQFP48
P	Pre-release					B-Z	as required			AAA-999	unique part identification		
S	Customer special												

PFS 26 X Y AM Z A0

Family segmentation	
2 series	General-purpose
26	Attach to S32K3

X	PMIC solutions
0	Vcore 0.8 A, Vboost, 1 MV Buck, 2 LDOs 1 Tracker
1	Vcore 0.8 A, Vboost, 1 MV Buck, 2 LDOs 2 Trackers
2	Vcore 1.5 A, Vboost, 1 MV Buck, 2 LDOs 1 Tracker
3	Vcore 1.5 A, Vboost, 1 MV Buck, 2 LDOs 2 Trackers

Y	FS1b	LDT	Use case
0	no	no	Base
1	yes	no	FS1b
2	no	yes	LDT
3	yes	yes	FS1b and LDT

Z	ASIL
B	Fit for ASIL B (Simple WD, UV/OV, ABIST, VMON)
D	Fit for ASIL D (Challenger WD, FCCU, ABIST/LBIST, VMON)

Figure 2 shows the part number mapping versus the product features set.

Vcore	0.8A core				1.5A core			
EXT Supply	1 TRK		2 TRK		1 TRK		2 TRK	
ASIL Level	ASIL B	ASIL D	ASIL B	ASIL D	ASIL B	ASIL D	ASIL B	ASIL D
Base	FS2600B	FS2600D	FS2610B	FS2610D	FS2620B	FS2620D	FS2630B	FS2630D
FS1b	FS2601B	FS2601D	FS2611B	FS2611D	FS2621B	FS2621D	FS2631B	FS2631D
LDT	FS2602B	FS2602D	FS2612B	FS2612D	FS2622B	FS2622D	FS2632B	FS2632D
FS1b + LDT	FS2603B	FS2603D	FS2613B	FS2613D	FS2623B	FS2623D	FS2633B	FS2633D

Figure 2. Part number mapping versus features set

Table 1. Device options

Part number	DEV_ID	Tracker 2	Core current capability	Long duration timer	Tracker 2 monitoring	FS1B	ABIST on demand	Watchdog type	Fault recovery	FCCU monitoring	LBIST
FS2600B	0x01	NO	0.8 A	NO	NO	NO	YES	Simple	NO	NO	NO
FS2601B	0x02	NO	0.8 A	NO	NO	YES	YES	Simple	NO	NO	NO

Table 1. Device options...*continued*

Part number	DEV_ID	Tracker 2	Core current capability	Long duration timer	Tracker 2 monitoring	FS1B	ABIST on demand	Watchdog type	Fault recovery	FCCU monitoring	LBIST
FS2602B	0x03	NO	0.8 A	YES	NO	NO	YES	Simple	NO	NO	NO
FS2603B	0x04	NO	0.8 A	YES	NO	YES	YES	Simple	NO	NO	NO
FS2600D	0x05	NO	0.8 A	NO	NO	NO	YES	Challenger	YES	YES	YES
FS2601D	0x06	NO	0.8 A	NO	NO	YES	YES	Challenger	YES	YES	YES
FS2602D	0x07	NO	0.8 A	YES	NO	NO	YES	Challenger	YES	YES	YES
FS2603D	0x08	NO	0.8 A	YES	NO	YES	YES	Challenger	YES	YES	YES
FS2610B	0x09	YES	0.8 A	NO	YES	NO	YES	Simple	NO	NO	NO
FS2611B	0x0A	YES	0.8 A	NO	YES	YES	YES	Simple	NO	NO	NO
FS2612B	0x0B	YES	0.8 A	YES	YES	NO	YES	Simple	NO	NO	NO
FS2613B	0x0C	YES	0.8 A	YES	YES	YES	YES	Simple	NO	NO	NO
FS2610D	0x0D	YES	0.8 A	NO	YES	NO	YES	Challenger	YES	YES	YES
FS2611D	0x0E	YES	0.8 A	NO	YES	YES	YES	Challenger	YES	YES	YES
FS2612D	0x0F	YES	0.8 A	YES	YES	NO	YES	Challenger	YES	YES	YES
FS2613D	0x10	YES	0.8 A	YES	YES	YES	YES	Challenger	YES	YES	YES
FS2620B	0x11	NO	1.5 A	NO	NO	NO	YES	Simple	NO	NO	NO
FS2621B	0x12	NO	1.5 A	NO	NO	YES	YES	Simple	NO	NO	NO
FS2622B	0x13	NO	1.5 A	YES	NO	NO	YES	Simple	NO	NO	NO
FS2623B	0x14	NO	1.5 A	YES	NO	YES	YES	Simple	NO	NO	NO
FS2620D	0x15	NO	1.5 A	NO	NO	NO	YES	Challenger	YES	YES	YES
FS2621D	0x16	NO	1.5 A	NO	NO	YES	YES	Challenger	YES	YES	YES
FS2622D	0x17	NO	1.5 A	YES	NO	NO	YES	Challenger	YES	YES	YES
FS2623D	0x18	NO	1.5 A	YES	NO	YES	YES	Challenger	YES	YES	YES
FS2630B	0x19	YES	1.5 A	NO	YES	NO	YES	Simple	NO	NO	NO
FS2631B	0x1A	YES	1.5 A	NO	YES	YES	YES	Simple	NO	NO	NO
FS2632B	0x1B	YES	1.5 A	YES	YES	NO	YES	Simple	NO	NO	NO
FS2633B	0x1C	YES	1.5 A	YES	YES	YES	YES	Simple	NO	NO	NO
FS2630D	0x1D	YES	1.5 A	NO	YES	NO	YES	Challenger	YES	YES	YES
FS2631D	0x1E	YES	1.5 A	NO	YES	YES	YES	Challenger	YES	YES	YES
FS2632D	0x1F	YES	1.5 A	YES	YES	NO	YES	Challenger	YES	YES	YES
FS2633D	0x20	YES	1.5 A	YES	YES	YES	YES	Challenger	YES	YES	YES

Table 1 provides a list of the different device options available.

Empty OTP samples can be ordered for engineering purpose by part number PFS2630AMDA0AD.

6 Simplified application diagram

The following figure shows the FS26 simplified block diagram for a typical system utilizing the boost controller to support battery cold-crank events.

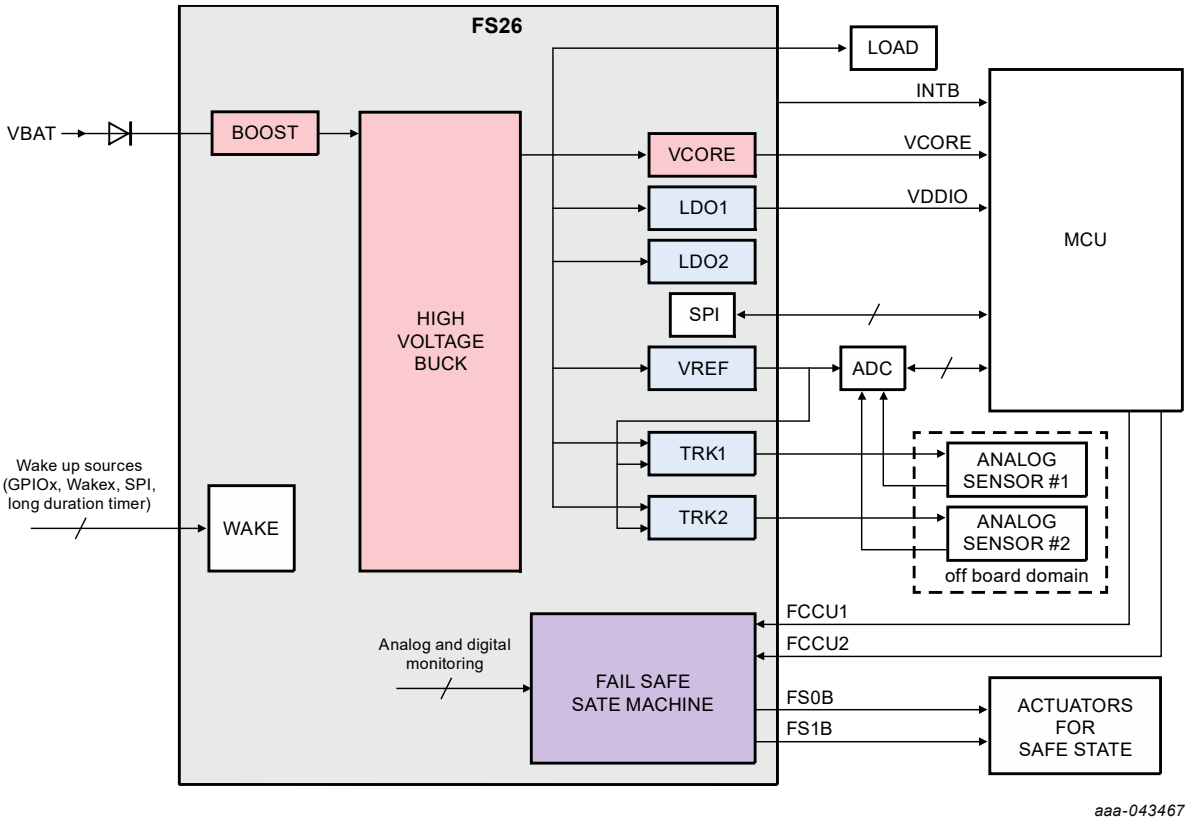


Figure 3. Example of an application diagram (with boost as a front-end regulator)

The following figure shows the FS26 simplified block diagram for a typical system utilizing the boost controller to generate a voltage above the high-voltage buck output voltage.

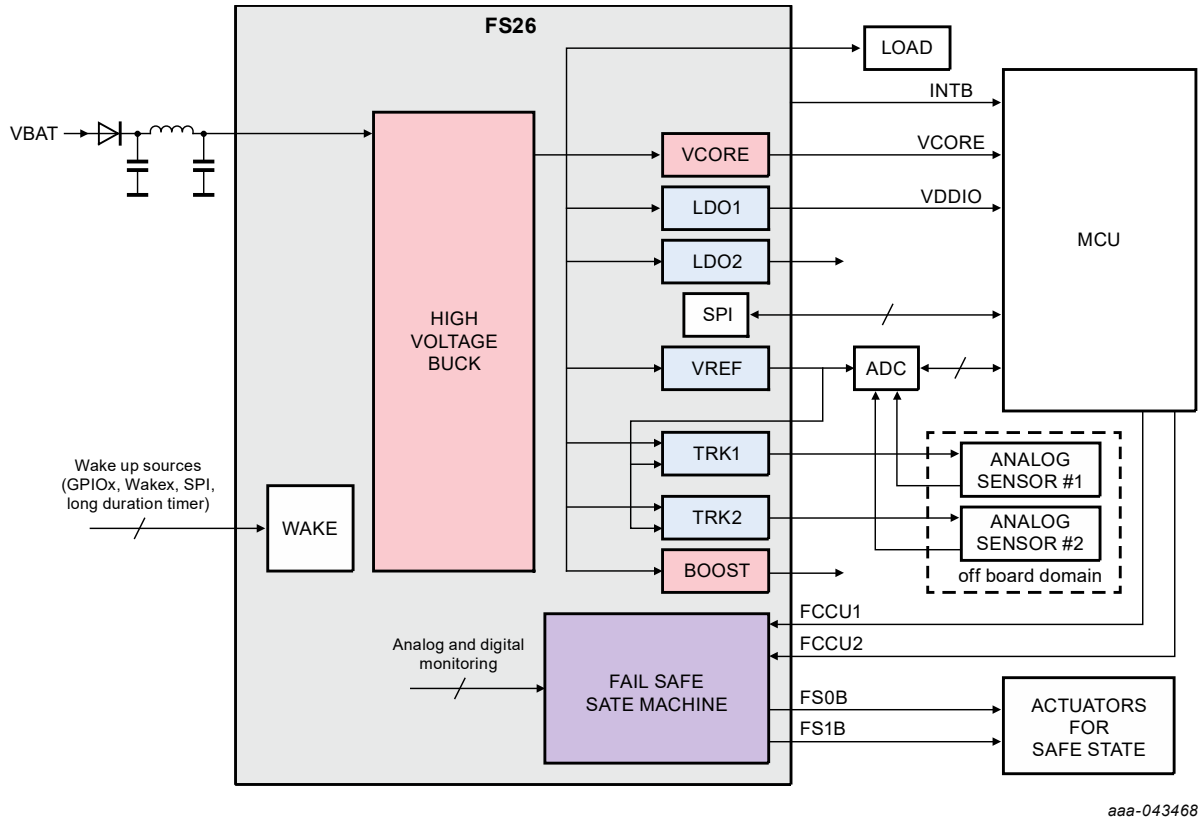


Figure 4. Example of an application diagram (with boost as a back-end regulator)

7 Block diagram

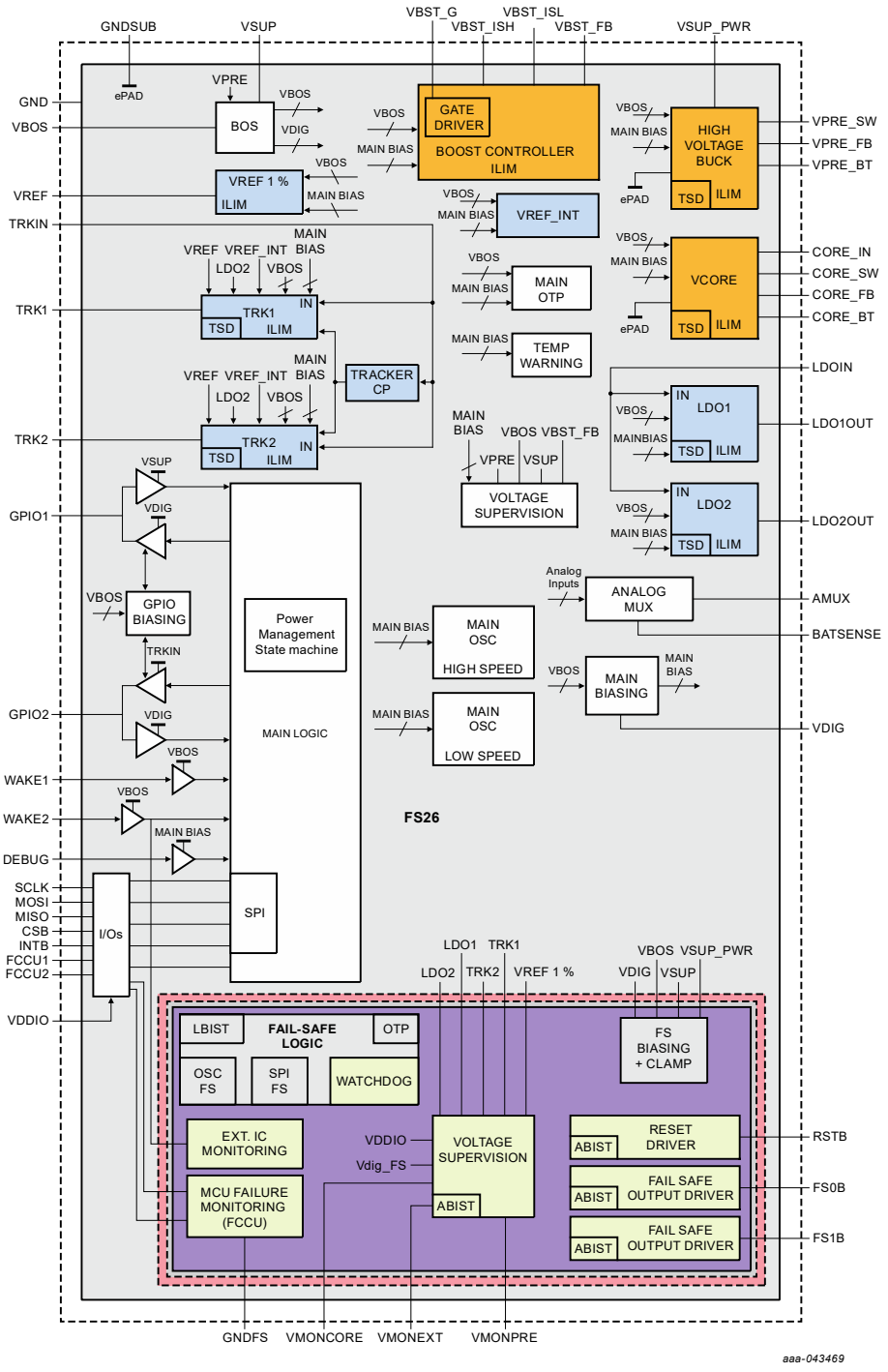


Figure 5. FS26 block diagram

8 Pinning information

8.1 Pinning

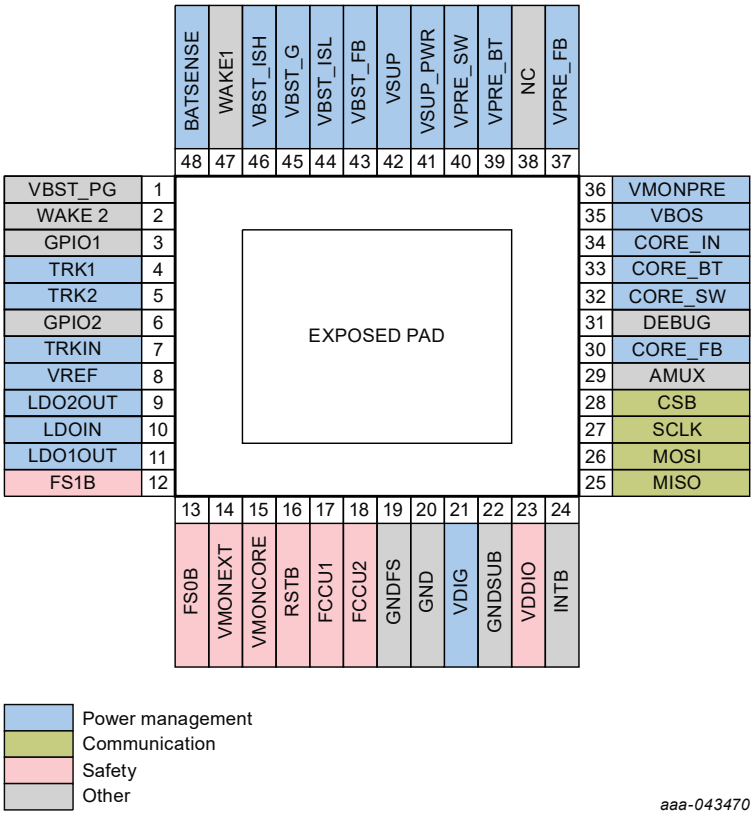


Figure 6. Pin configuration

8.2 Pin description

Table 2. Pin description

Symbol	Pin number	Type	Description
VBST_PG	1	Digital output	Power good signal for boost converter
WAKE2	2	Analog input	WAKE2 input pin or ERROR monitoring Input
GPIO1	3	Analog output / Digital Input	General-purpose I/O 1
TRK1	4	Analog output	TRK1 output
TRK2	5	Analog output	TRK2 output
GPIO2	6	Analog output / Digital Input	General-purpose I/O 2
TRKIN	7	Analog input	Tracker input
VREF	8	Analog output	Voltage reference output
LDO2OUT	9	Analog output	LDO2 output
LDOIN	10	Analog input	LDO input voltage supply
LDO1OUT	11	Analog output	LDO1 output
FS1B	12	Digital output	Safety output #1
FS0B	13	Digital output	Safety output #0

Table 2. Pin description*...continued*

Symbol	Pin number	Type	Description
VMONEXT	14	Analog input	External VMON input
VMONCORE	15	Analog input	VCORE voltage monitoring input
RSTB	16	Digital output	Reset output
FCCU1	17	Digital input	Fault control collection unit 1
FCCU2	18	Digital input	Fault control collection unit 2
GNDFS	19	Ground connection	GND for fail-safe circuitry
GND	20	Ground connection	GND for main circuit
VDIG	21	Analog output	1.6 V digital supply
GNDSUB	22	Ground connection	Substrate ground
VDDIO	23	Analog input	I/O input supply
INTB	24	Digital output	Interrupt output
MISO	25	Digital output	SPI MISO
MOSI	26	Digital input	SPI MOSI
SCLK	27	Digital input	SPI clock input
CSB	28	Digital input	SPI chip select
AMUX	29	Analog output	Analog multiplexer output
CORE_FB	30	Analog input	VCORE feedback node
DEBUG	31	Digital input	DEBUG input pin
CORE_SW	32	Analog output	VCORE switching node
CORE_BT	33	Analog input	VCORE bootstrap supply
CORE_IN	34	Analog input	VCORE input supply
VBOS	35	Analog output	Best of supply decoupling output
VMON_PRE	36	Analog input	VPRE monitoring pin
VPRE_FB	37	Analog input	VPRE Feedback node
NC	38	Not connected pin	Not connected pin
VPRE_BT	39	Analog output	VPRE boot strap capacitor
VPRE_SW	40	Analog output	VPRE switching node
VSUP_PWR	41	Analog input	VPRE converter supply pin
VSUP	42	Analog input	Supply pin for internal biasing
VBST_FB	43	Analog input	VBST feedback node
VBST_ISL	44	Analog input	VBST current sense low
VBST_G	45	Analog output	VBST low-side gate drive
VBST_ISH	46	Analog input	VBST current sense high
WAKE 1	47	Analog input	WAKE1 input pin
BATSENSE	48	Analog input	Battery sense terminal
EP	49	Ground connection	Exposed pad (to be connected to GND)

9 Maximum ratings

Table 3. Maximum ratings

Symbol	Description (Rating)	Min	Max	Unit
Voltage ratings				
VPRE_BT	DC voltage at VPRE_BT pin	−0.3	45.5	V
GPIO1, GPIO2, FS1B, FS0B, VMONEXT, VMONCORE, WAKE2, VPRE_SW, VBST_FB, WAKE1	DC voltage at GPIO1, TRK1, TRK2, GPIO2, FS1B, FS0B, VMONEXT, VMONCORE, WAKE2, VPRE_SW, VBST_FB, WAKE1 and BATSENSE pins	−0.3	40	V
BATSENSE	DC voltage at BATSENSE pin with −10 mA maximum reverse current (recommended 5.1 kΩ serial resistor)	−18	40	V
TRK1, TRK2, VSUP, VSUP_PWR	DC voltage at TRK1, TRK2, VSUP_PWR, VSUP pins	−1.2	40	V
CORE_BT, DEBUG	DC voltage at CORE_BT and DEBUG pins	−0.3	10	V
TRKIN, LDOIN, CORE_IN, VPRE_FB, VMONPRE, CORE_SW	DC voltage at TRKIN, LDOIN, CORE_IN, VPRE_FB, VMONPRE pins	−0.3	7.0	V
VBOS	DC voltage at VBOS pin	−0.3	5.6	V
VREF, LDO2OUT, LDO1OUT, RSTB, FCCU1, FCCU2, VDDIO, INTB, MISO, MOSI, SCLK, CSB, AMUX, CORE_FB, VBST_ISH, VBST_ISL, VBST_G, VBST_PG	DC voltage at VREF, LDO2OUT, LDO1OUT, RSTB, FCCU1, FCCU2, VDDIO, INTB, MISO, MOSI, SCLK, CSB, AMUX, CORE_FB, VBST_ISH, VBST_G and VBST_PG pins	−0.3	5.5	V
VDIG	DC voltage at VDIG pin	−0.3	2.0	V
GNDFS, GND, GNDSUB	DC voltage at GNDFS, GND, GNDSUB pins	−0.3	0.3	V
WAKE1, WAKE2, GPIO1, GPIO2	DC maximum reverse current at WAKE1, WAKE2, GPIO1, GPIO2 pins	−5.0	—	mA

10 Electrostatic discharge

Table 4. Maximum ratings

Symbol	Description (Rating)	Min	Max	Unit
ESD ratings				
Human body model: AEC-Q-100 Rev H				
V_{ESD_HBM}	All pins	−2.0	2.0	kV
Charged Device model: AEC-Q-100 Rev H				
V_{ESD_CDM1}	All pins	−500	500	V
V_{ESD_CDM2}	Corner pins	−750	750	V
Gun Test				
V_{ESD_CDT1}	ESD - GUN discharged contact test 330 Ω/150 pF unpowered according to IEC61000-4-2 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	−8.0	8.0	kV

Table 4. Maximum ratings*...continued*

Symbol	Description (Rating)	Min	Max	Unit
V_{ESD_CDT2}	ESD - GUN discharged contact test 2 kΩ/150 pF unpowered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	−8.0	8.0	kV
V_{ESD_CDT3}	ESD - GUN discharged contact test 2 kΩ/330 pF powered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	−8.0	8.0	kV
V_{ESD_CDT4}	ESD - GUN discharged contact test 330 Ω/150 pF powered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	−8.0	8.0	kV
V_{ESD_CDT5}	Operating ESD- GUN discharged contact test 330 Ω/150 pF powered according to ISO10605.2008 Global pins (GND, BATSENSE, FS0B, FS1B). Criteria: CLASS A	−8.0	8.0	kV

11 Thermal ratings

Table 5. Temperature range

Symbol	Description	Min	Typ	Max	Unit
T_A	Ambient temperature	−40	—	125	°C
T_J	Junction temperature	−40	—	150	°C
T_{STG}	Storage temperature	−55	—	150	°C
T_{WARN}	Temperature warning threshold to set TWARN_S SPI bit	145	155	170	°C

Table 6. Thermal resistance (per JEDEC JESD51-2)

Symbol	Description	Value	Unit
$R_{\theta JA}$	Thermal resistance junction to ambient [1]	25	°C/W
$R_{\theta JCBOTTOM}$	Thermal resistance junction to case bottom [2] [3]	1.7	°C/W
$R_{\theta JCTOP}$	Thermal resistance junction to case top [4]	13.5	°C/W
Y_{JT}	Thermal characterization parameter junction to top [1] [2]	0.8	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[2] Thermal test board meets JEDEC specification for this package (JESD51-7).
[3] Thermal resistance between the die and the printed circuit board. Board temperature is measured on the top surface of the board near the package.
[4] For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

12 Package information

Table 7. Package information

Package	Suffix	Package outline drawing number
7.0 x 7.0, 48-pin LQFP exposed pad, with 0.5 mm pitch, and a 4.5 x 4.5 exposed pad	AE	98ASA00173D

12.1 Package outline

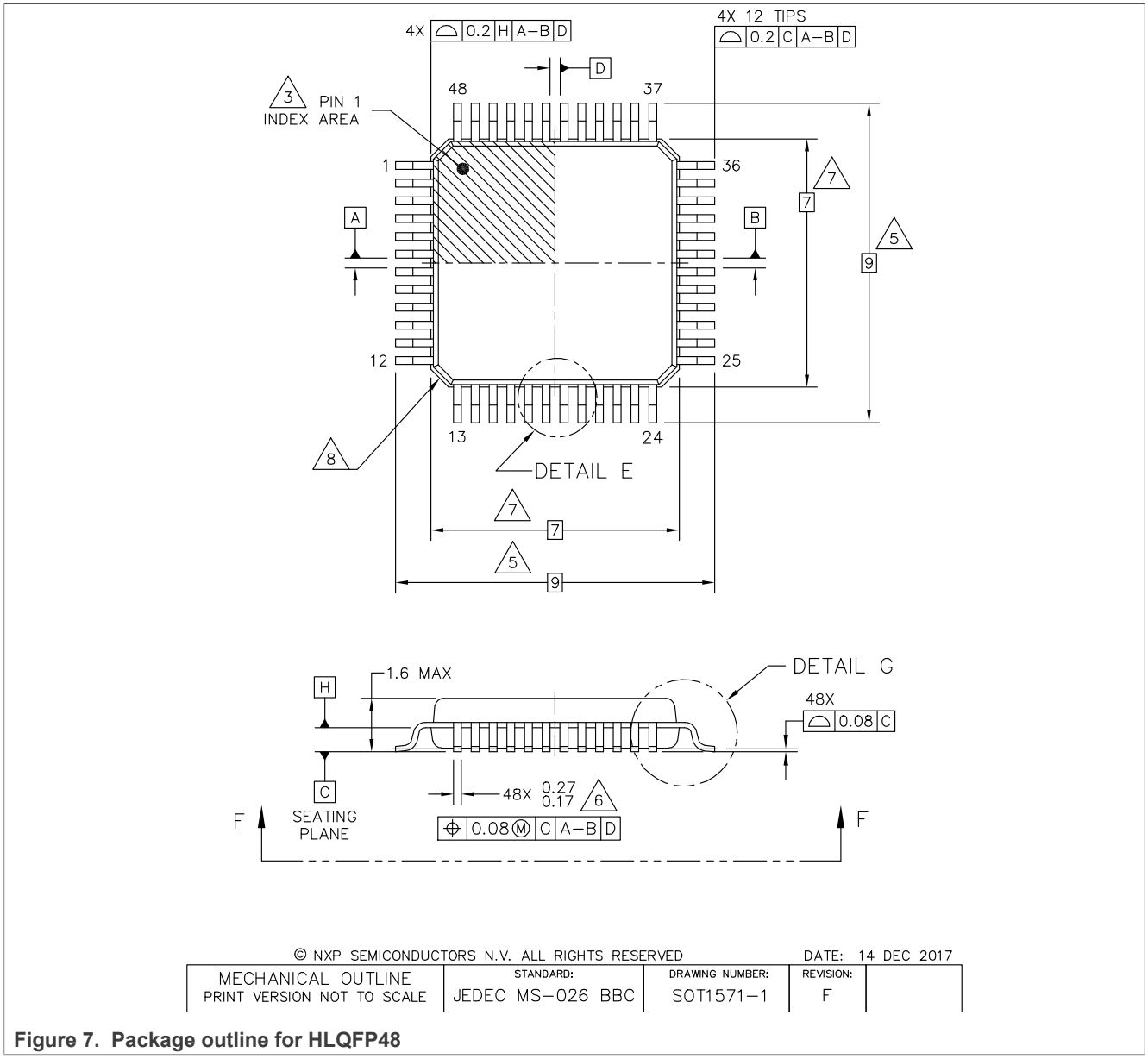
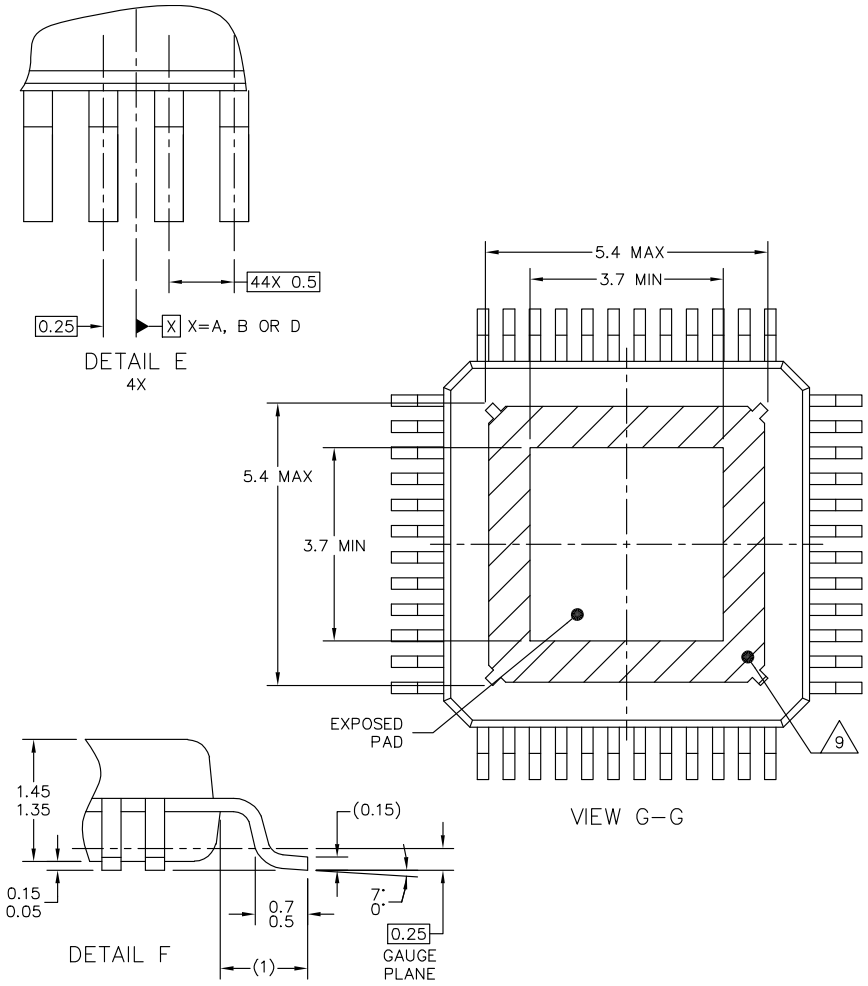


Figure 7. Package outline for HLQFP48



 DATE: 14 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS–026 BBC	DRAWING NUMBER: SOT1571–1	REVISION: F	

Figure 8. Package outline detail for HLQFP48

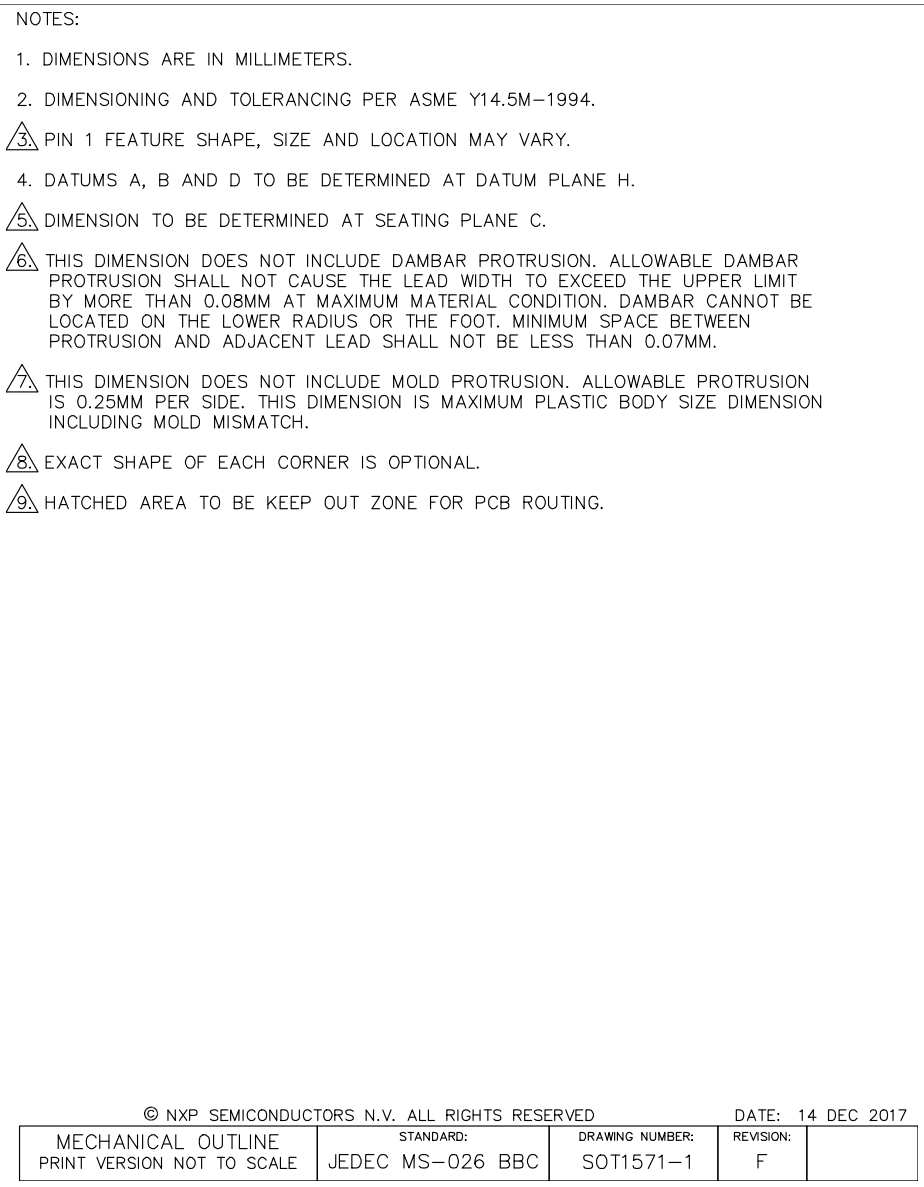


Figure 9. Package outline notes for HLQFP48

13 References

[1] **FS26** — Safety System Basis Chip (SBC) with Low Power Fit for ASIL D
http://www.nxp.com/FS26

[2] **FS26 Dynamic FMEDA** — FMEDA analysis
https://www.docstore.nxp.com

[3] **AN12995** — FS26 product guidelines application note
https://www.docstore.nxp.com

[4] **FS26SMUG** — Safety manual
https://www.docstore.nxp.com

[5] **FS26_SMPS_Calculator.xls** — calculation tool (Excel file)
https://www.docstore.nxp.com

[6] **FS26 SMPS Simplis Model** Simplis model for stability and transient simulations
https://www.docstore.nxp.com

[7] **FS26 Graphical User Interface** — calculate the power dissipation, create an OTP configuration, and interface an EVB KIT with a computer
https://www.docstore.nxp.com

[8] **KITFS26AEEVM** — detailed information on this board, including documentation, downloads, and software and tools
http://www.nxp.com/KITFS26AEEVM

[9] **KITFS26SKTEVM** — detailed information on this board, including documentation, downloads, and software and tools
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