PB_PF5113

Power management integrated circuit (PMIC) for high performance applications

Rev. 1 — 12 January 2023 Product brief

1 Introduction

This product brief provides overview/summary information for evaluating a product for design suitability. It is intended for quick reference only and should not be relied upon to contain detailed and full information.

Some of the content in this product brief is extracted from the full data sheet of the product. The full data sheet prevails in case of any inconsistency or conflict.

2 General description

The PF5113 integrates multiple high-performance buck regulators and LDO regulators. It can operate as a standalone point-of-load regulator integrated circuit (IC), or as a companion chip to a larger power management integrated circuit (PMIC).

Built-in one time programmable (OTP) memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of regulators. Regulator parameters are adjustable through high-speed I^2C after startup, offering flexibility for different system states.

Functional safety features, developed according to ISO 26262 specifications, enable the device to reach safety levels up to ASIL D.

3 Features and benefits

The PF5113 is a PMIC designed to be the primary, core power supply for radar application processors.

- Buck regulators
  - SW1: 0.8 V, 0.825 V, 0.9 V, 1.2 V; 2600 mA; 1.5 % accuracy
  - SW2: 1.3 V, 1.5 V, 1.8 V, 2.3 V, 2.5 V, 3.3 V; 3500 mA; 1.5 % accuracy
  - SW3: 1.1 V, 1.3 V, 1.5 V, 2.5 V, 3.3 V; 2600 mA; 1.5 % accuracy
  - Dynamic voltage scaling
  - Configurable as a dual- and triple-phase regulator
  - Programmable current limit
  - Spread spectrum and manual tuning of switching frequency
- LDO regulator
  - LDO1: 1.8 V, 3.3 V; 200 mA; 1.5 % accuracy
  - LDO2: 1.8 V, 3.3 V; 250 mA; 1.5 % accuracy
- PGOOD output and monitor
- Clock synchronization through configurable input sync pin
- System features
  - Advanced state machine for seamless processor interface
  - High-speed I^2C interface support (up to 3.4 MHz)

- Programmable soft-start sequence and power down sequence
- Programmable regulator configuration

- One time programmable (OTP) memory for device configuration
- Monitoring circuit to fit ASIL D safety level
  - Independent voltage monitoring with programmable fault protection
  - Advance thermal monitoring and protection
  - Watchdog monitoring and programmable internal watchdog counter
  - I^2C cyclic redundancy check (CRC) and write protection mechanism
  - Analog built-in self-test (ABIST)
  - Logic built-in self-test (LBIST)

4 Applications

- Automotive – radar

5 Ordering information

Table 1. Ordering information

Type number [1]	Package		
	Name	Description	Version
PPF5113AMDA0ES[2]	HWQFN28	HWQFN28, plastic thermal enhanced very thin quad flat pack; no leads, wettable flank, 28 terminals, 0.5 mm pitch, 4.5 mm x 4.5 mm x 0.53 mm body	SOT2089-1(SC)
PPF5113AMBA0ES[3]			
PPF5113AMMA0ES[4]			

[1] To order parts in tape and reel, add the R2 suffix to the part number.
[2] Safety grade: ASIL D, non-programmed device, custom OTP is PPF5113AMDxxES. "xx" is unique letter and number by each OTP config.
[3] Safety grade: ASIL B, non-programmed device, custom OTP is PPF5113AMDxxES. "xx" is unique letter and number by each OTP config.
[4] Safety grade: QM, non-programmed device, custom OTP is PPF5113AMDxxES. "xx" is unique letter and number by each OTP config.

6 Block diagram

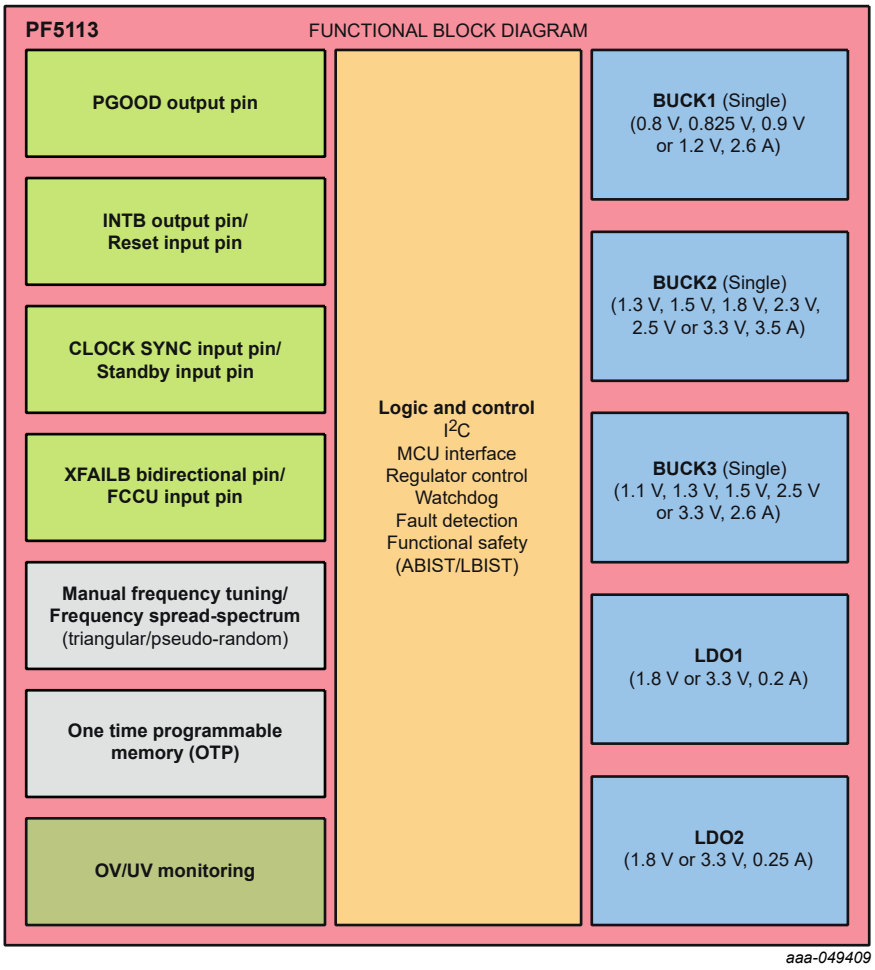

Figure 1. PF5113 block diagram

6.1 Simplified application diagram

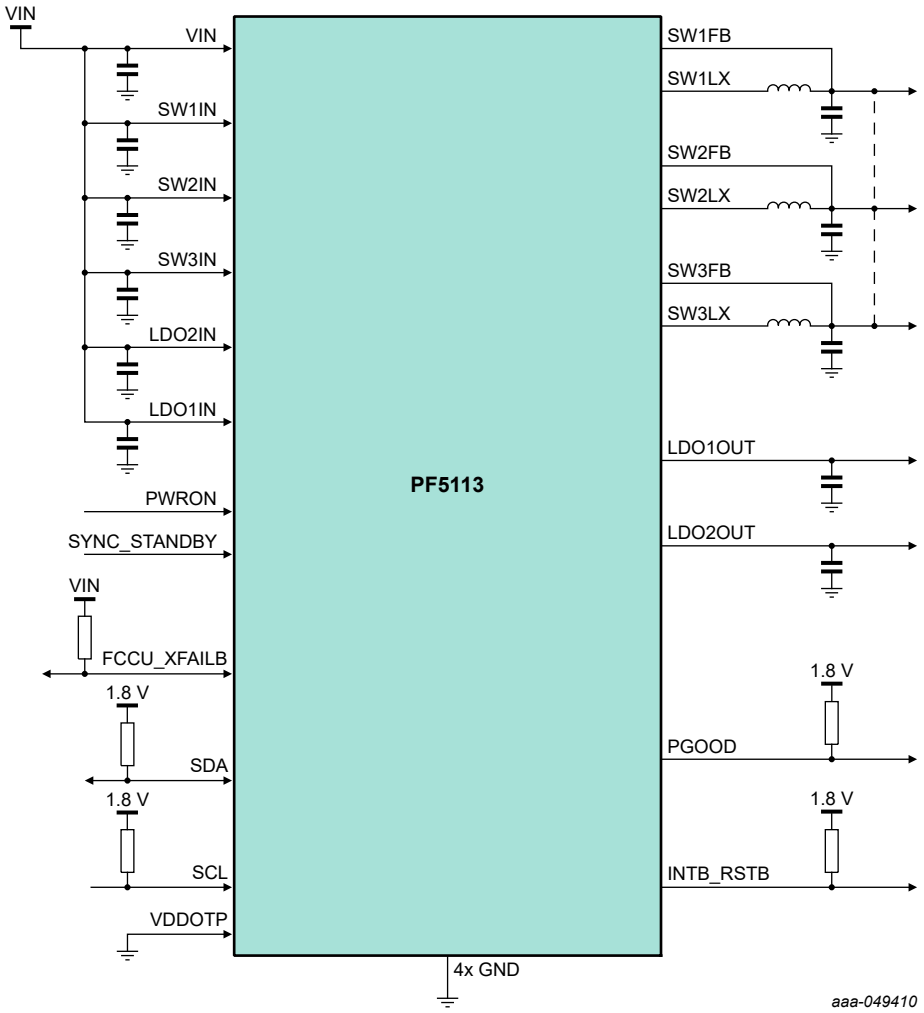

Figure 2. Simplified application diagram

7 Pinning information

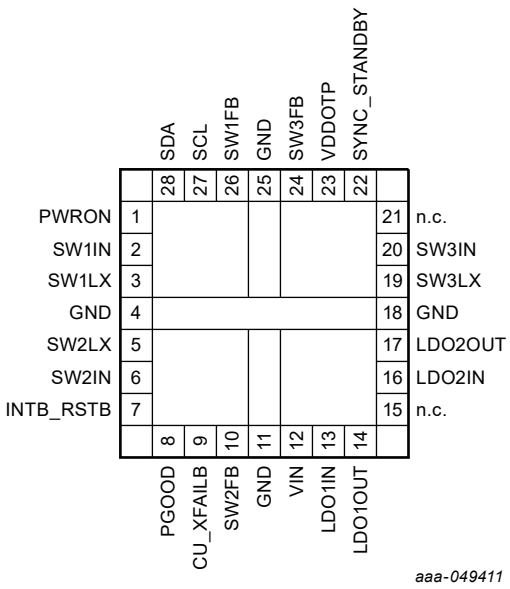

Figure 3. PF5113 pinout (top view)

Table 2. Pinning information

QFN pin number	Pin name	Pin description	Min	Max	Unit
1	PWRON	PWRON input	−0.3	5.5	V
2	SW1IN	SW1 input supply	−0.3	5.5	V
3	SW1LX	SW1 switching node	−0.3	5.5	V
4	PGND	Ground	−0.3	0.3	V
5	SW2LX	SW2 switching node	−0.7	5.5	V
6	SW2IN	SW2 input supply	−0.3	5.5	V
7	INTB_RSTB	Interrupt output/External reset input	−0.3	5.5	V
8	PGOOD	PGOOD output	−0.3	5.5	V
9	FCCU_XFAILB	FCCU input/XFAILB bidirectional signal	−0.3	5.5	V
10	SW2FB	SW2 feedback input	−0.3	5.5	V
11	GND	Ground	−0.3	0.3	V
12	VIN	Input supply	−0.3	5.5	V
13	LDO1IN	LDO1 input	−0.3	5.5	V
14	LDO1OUT	LDO1 output	−0.3	5.5	V
15	NC	No connect	−0.3	0.3	V
16	LDO2IN	LDO2 INPUT	-0.3	5.5	V
17	LDO2OUT	LDO2 output	−0.3	5.5	V
18	GND	Ground	−0.3	0.3	V
19	SW3LX	SW3 switching node	−0.7	5.5	V
20	SW3IN	SW3 input supply	−0.3	5.5	V

Table 2. Pinning information*...continued*

QFN pin number	Pin name	Pin description	Min	Max	Unit
21	NC	No connect	−0.3	0.3	V
22	SYNC_STANDBY	Clock synchronization input/Standby input	−0.3	5.5	V
23	VDDOTP	Debug mode/OTP programming input supply	−0.3	10	V
24	SW3FB	SW3 feedback input	−0.3	5.5	V
25	GND	Ground	−0.3	0.3	V
26	SW1FB	SW1 feedback input	−0.3	5.5	V
27	SCL	I^2C SCL signal	−0.3	5.5	V
28	SDA	I^2C SDA signal	−0.3	5.5	V

8 Package information

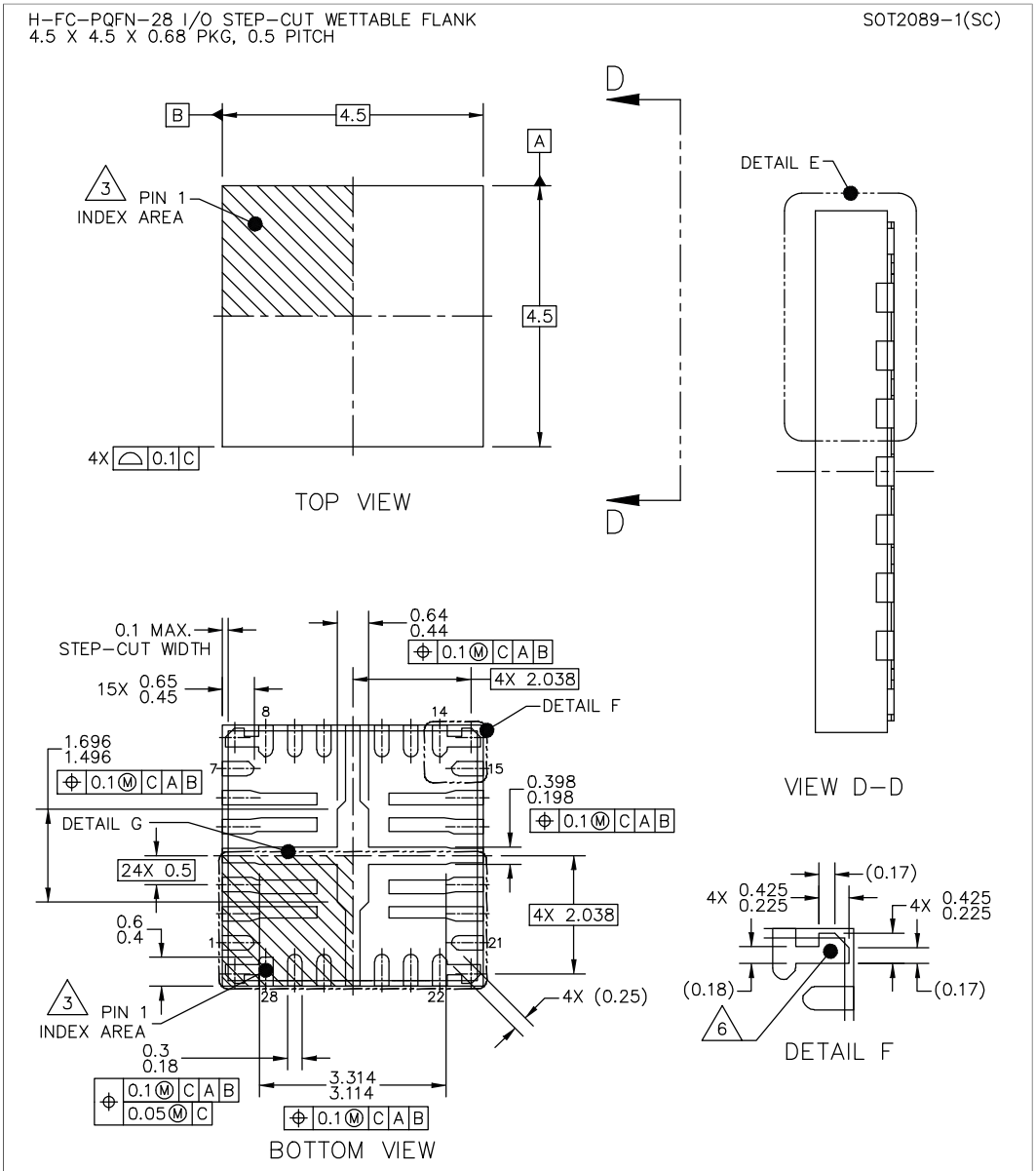

Figure 4. Package outline for PQFN28

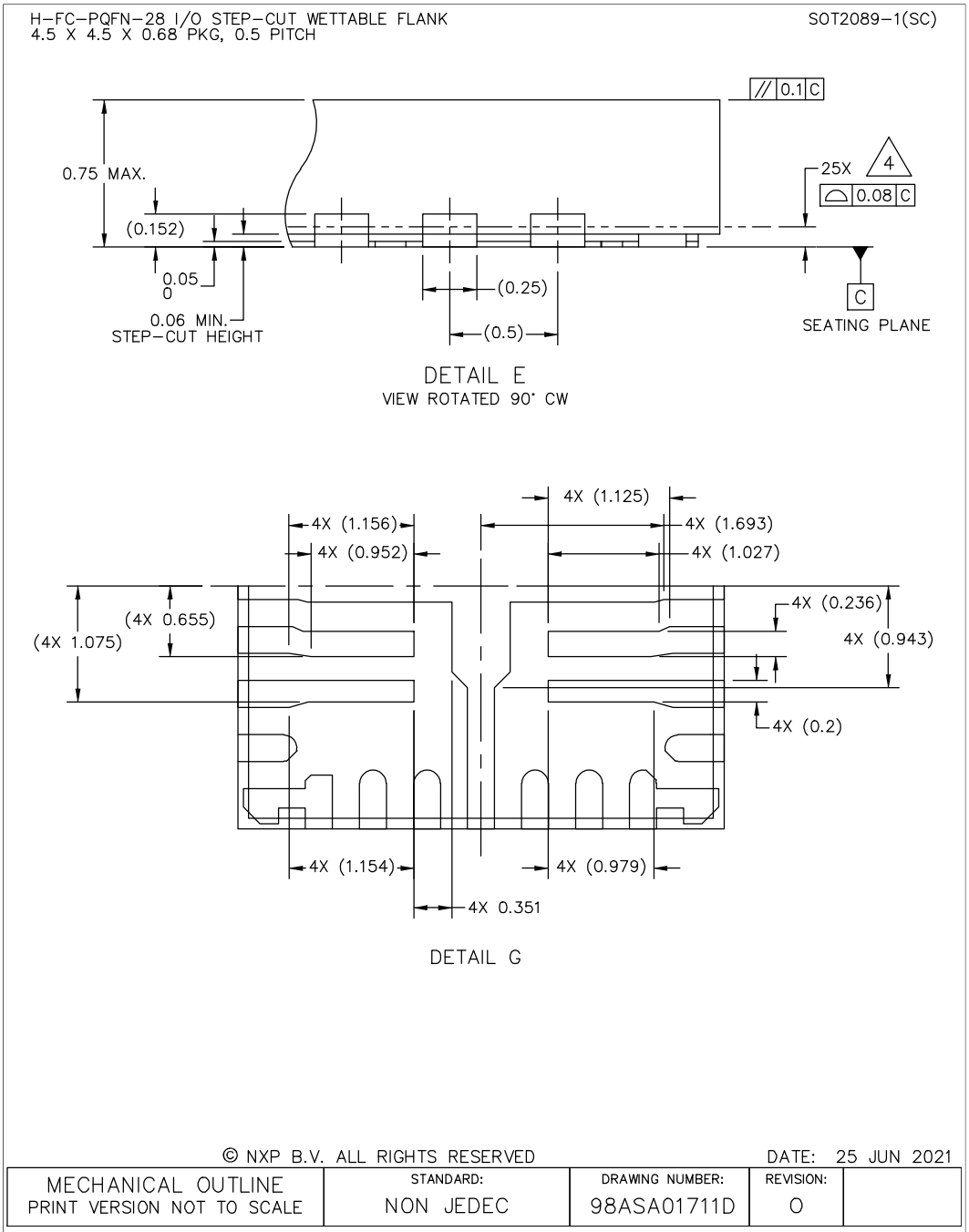

Figure 5. Package outline detail for PQFN28

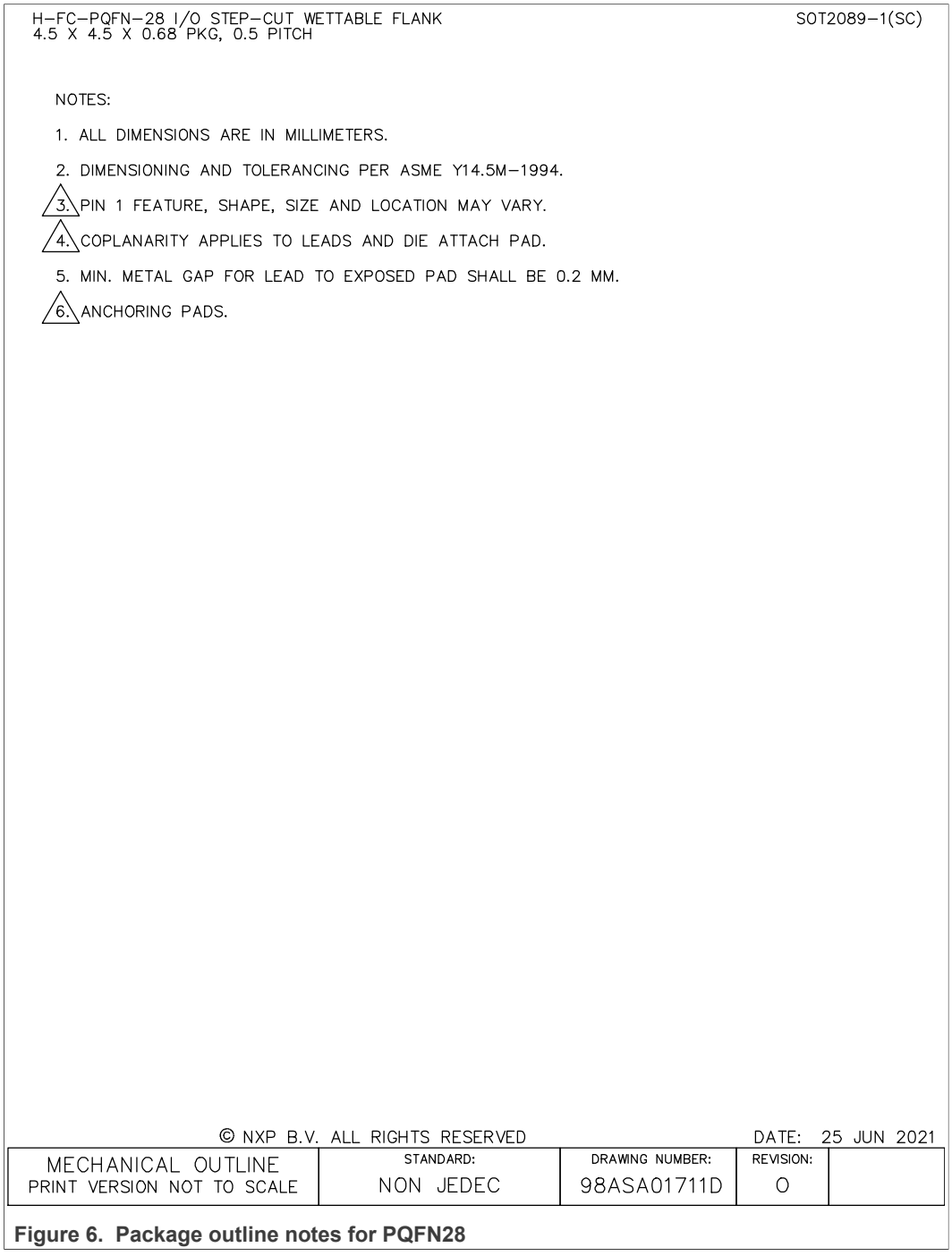

Figure 6. Package outline notes for PQFN28

Revision history

Revision	Date	Description
v.1	20230112	Initial release

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