

OSI Layer 2 and Layer 3 Router

Overview

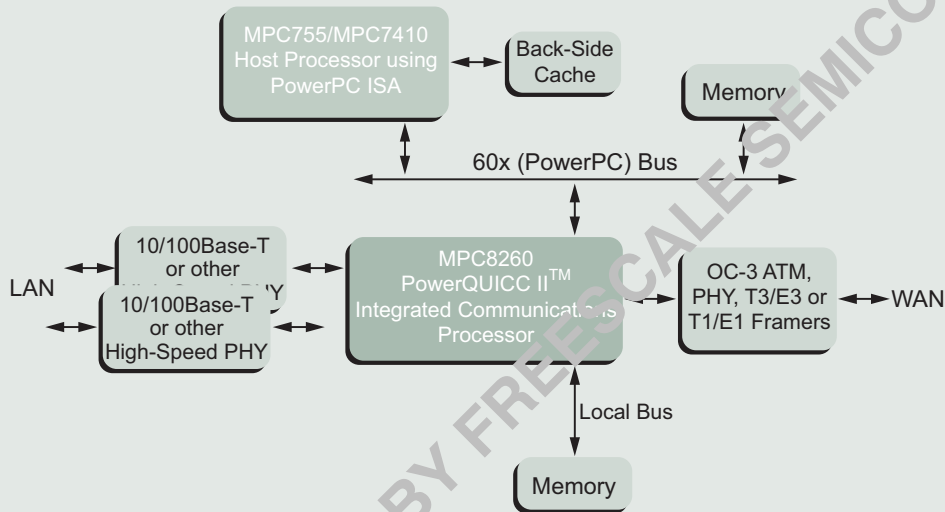
The OSI layer 2 and layer 3 router provides additional intelligence to networks by implementing the data link and network layers of the OSI model. The data link layer describes the logical organization of data bits transmitted on a particular medium; for example, this layer defines the framing,

addressing, and cyclic redundancy checks of Ethernet packets. The network layer describes how a series of exchanges over various data links delivers data between any two nodes in a network and defines the addressing and routing structure of the Internet.

Key Benefits

- > Implements the data link and network layers of the OSI model to provide additional intelligence to networks
- > Enables cost-efficient solutions through support for Freescale Semiconductor's Smart Alliance Program
- > Enables accelerated time-to-market for router equipment suppliers

OSI LAYER 2 AND LAYER 3 BLOCK DIAGRAM



Freescale Ordering Information

Part Number	Product Highlights	Additional Information
MPC8266 MPC8265 MPC8264 MPC8260 MPC8255	<ul style="list-style-type: none"> > System core microprocessor supporting frequencies of 133 to 300 MHz > System integration unit (SIU) > High performance communications processor module (CPM) with operating frequency of 133, 166, or 200 MHz > Two bus architectures: one 64-bit 60x bus and one 32-bit PCI or local bus > Two UTOPIA level-2 master/slave ports with multi-PHY support > Three MII interfaces > Eight TDM interfaces (T1/E1); two TDM ports can be seamlessly integrated to T3/E3 > 1.8 V or 2.0 V internal and 3.3 V I/O > 300 MHz power consumption: 2.5 W > 480 TBGA package (37.5 mm x 37.5 mm) 	www.freescale.com/smartnetworks
MPC862 MPC860 MPC857T MPC855T MPC850	<ul style="list-style-type: none"> > Embedded MPC8xx core > Instruction and data MMUs > Up to 32-bit data bus (dynamic bus sizing for 8,16, and 32 bits) > 32 address lines > Complete static design (040 MHz operation) > Memory controller (eight banks) > General purpose timers > System integration unit (SIU) > Interrupts > Communications processor module (CPM) > On-chip 16x16 multiply accumulate controller (MAC) > Four baud-rate generators > Four serial communication controllers (SCC) > Two serial management channels (SMC) > One serial peripheral interface (SPI) > One I²C (inter-integrated circuit) port > Time-slot assigner > Parallel interface port > PCMCIA interface > Low power support > Debug interface > 3.3 V operation with 5V TTL compatibility 	
MPC74xx family	<ul style="list-style-type: none"> > Host microprocessor family > High performance, low power 32-bit implementation of the PowerPC RISC > Architecture with a full 32-bit implementation of Freescale Semiconductor's AltiVec technology > Reach speeds up to 1 GHz with a core voltage of 1.6 V that includes 256 KB of on-chip L2 cache with support of up to 2MB of backside L3 > Benefit from Freescale Semiconductor's HiPerMOS silicon-on-insulator process technology that enables the processor to deliver increased performance and lower power over bulk CMOS technology 	
MPC75x family	<ul style="list-style-type: none"> > Superscalar design > Capable of issuing three instructions per clock cycle into six independent execution units: two integer units, a load/store unit, a floating-point unit (MPC750/740), a double-precision floating-point unit (MPC755 and MPC745), a system register unit, and a branch processing unit 	

Design Challenges

The performance of upper-layer router equipment is defined by serial data transfer rates. Obtaining faster serial data transfer rates while achieving the processing power required for layers 2 and 3 data manipulation and routing normally requires a series of hardware designs and limited reuse of software (protocol and services) across the various interfaces.

Freescale Semiconductor Solution

Freescale Semiconductor's PowerQUICC™ family of integrated communications processors are coupled with host processors using PowerPC™

ISA to meet the dual challenges of connecting to a high-speed serial interface and handling layer 2 and layer 3 data manipulation.

The MPC755 or MPC7410 host processor achieves the data manipulation rate required for the OSI standard with a powerful RISC architecture designed to execute several instructions per clock cycle. It interfaces seamlessly with the MPC8260 PowerQUICC II that operates in slave mode and transfers the serial data to memory.

The host processor's RISC microprocessor, associated with single-cycle access dual-port static RAM, is dedicated to service the on-chip serial communications ports and use direct memory access (DMA) to transfer serial data to external memory.

In addition, the established code base and broad third-party support from Freescale Semiconductor's Smart Network Alliance Program members further enable cost-efficient solutions and accelerated time-to-market for router equipment suppliers.

Development Tools *Note*

Tool Type	Product Name	Vendor	Description
Software	CWEPPC	Metrowerks	CodeWarrior Development Studio for PowerPC ISA
Software	CWLINPPC	Metrowerks	CodeWarrior Development Studio, Linux Application Edition for PowerPC
Development Kit	MPC8260ADSKIT	Freescale Semiconductor	MPC8260 Application Development System Kit
Hardware	MPC8260ADS-L2C	Freescale Semiconductor	MPC8260 Application Development System (with L2 cache) (DISCONTINUED)
Hardware	MPC8260ADS-PQ2	Freescale Semiconductor	MPC8260 Application Development System
Development Kit	MPC8266ADS-KIT	Freescale Semiconductor	MPC8266 Application Development System Kit
Hardware	MPC8266ADS-PCI	Freescale Semiconductor	MPC8266 Application Development System (for PCI Host Mode)
Hardware	MPC8266ADS-PCIAI	Freescale Semiconductor	MPC8266 Application Development System (Add-In Card)
Hardware	MPC8XXFADSMB	Freescale Semiconductor	MPC8xx Family Application Development System Motherboard
Hardware	PPCEVAL-SP3-7400	Freescale Semiconductor	Altimus X3 MPC7400 PMC Module for the Sandpoint X3 Motherboard
Hardware	PPCEVAL-SP3-750	Freescale Semiconductor	Altimus X3 MPC750 PMC Module for the Sandpoint X3 Motherboard (discontinued)
Hardware	SANDPOINTX3	Freescale Semiconductor	Sandpoint X3 Evaluation System - Motherboard
Software	DINK32	Freescale Semiconductor	ROM-Based Debug Monitor, R13.0

Note: For detailed information, go to www.freescale.com and click on Tools. Search for tools by product or technology, family or function, and product number.

Notes

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