MPC823e Pocket Guide

A Quick Reference to the
MPC823e Reference Manual

This pocket guide contains the memory map, list of registers, instructions, and signals for the MPC823e microprocessor. The page numbers listed in each table are referencing the *MPC823e Reference Manual.* For more information on the MPC823e, visit our website at www.mot.orola.com.

Design Guidelines
Revision 1.3

When integrating the MPC8xx family of microprocessors into an application, the following items can help guide you through the process. These guidelines originated from common problems that were found while debugging and operating actual MPC8xx implementations.

- **Find the Mask Number and Version of Your Chip**
  Each chip has different sets of numbers etched onto it and one of these sets is the mask and revision number for that particular chip. The mask number and the revision number are combined into one. For example, 0F98S. 0 is the revision number and F98S is the mask number. You need this information in order to find the errata for that version of the chip. Obtaining the appropriate errata will help you design your product more efficiently. Once you know your mask and revision numbers, go to our website for your particular MPC8xx chip errata. If you do not have web access, contact your local Motorola sales office. In addition, the feature differences between early revs of the MPC823e are significant. This is another reason to find the mask number and version of your chip.

System Considerations

- **Always Provide a Development Interface Port on Your Design**
  The MPC823e Family Application Development System (MPC823eFADS) has a 10-pin header that you can use to connect to your target board. With this header installed, you can perform initial testing and follow-up debugging. By connecting a FADS board to your PC, you can use our PC hosted debugger (MPC8bug) to manipulate registers on your target board, just as you would directly on the FADS board. However, you must remove the MPC823e device from its socket on the FADS board. To minimize noise and maintain system integrity, use the shortest 10-wire cable between the FADS board and your target board. Other third-party tools use this 10-pin header for their debugger capability as well.

  The DSDI and DSCK pins of the 10-pin header are configured during reset to select certain modes of the development port system interface. If you want to pull these pins low, then you should use 1Kohm pull-downs so that low logic levels are recognized on all versions of the MPC823e.

  The MPC823eFADS boards can be an invaluable tool for developing software or you can simply use the accompanying schematics as a template. Our web site contains the documentation and schematics for the MPC823eFADS boards, which can be ordered from your local Motorola sales office.

- **$\overline{\text{IRQ0}}$ is Really $\overline{\text{NMI}}$**
  It is mentioned in the manual that $\overline{\text{IRQ0}}$ causes a non-maskable interrupt, i.e., reset. Do not connect anything to this pin that you do not want causing a system reset. Memory upgrades for FADS/Compatible Systems. Any 16MB, 32-bit 72-pin 60ns EDO DRAM SIMM should work with our ADS or FADS systems. We recommend ordering from Southland Micro Systems. The part number for 16MB SIMMs is SGE 4X32T6E. Note that 5V DRAMs are needed since the FADS boards are designed for it. If you choose 3.3V DRAM, solder a zero-ohm resistor or a short on R83.

Memory Considerations

See **Section 15 Memory Controller** of the *MPC823e Reference Manual* for additional information.

- **Increase Your Chip-Select Drive Capability**
  You can get more drive capability on the CS2 and CS3 signals by having each of them output on two pins. CS2 can be driven on the normal CS2 pin and GPL_A2 and CS3 can be driven on the normal CS3 pin and GPL_A3. The CSx pins can also be used as RAS lines where drive capability is critical in gaining the last nanosecond from the memory system. Program the SIUMCR register (located in **Section 12 System Interface Unit** of the *MPC823e Reference Manual*) to implement this double drive function.

- **Do Not Rely Solely on the R/W Pin**
  The timing of the R/W pin may not be the best choice for the memory type you have chosen. Remember that the R/W timing is fixed and the WEx signals are usually a better choice. If the timing of the WEx signals is not suitable, you can use the more flexible user-programmable machine of the memory controller to get precise timing on these signals.

Clocking Considerations

Using the following suggestions can improve the stability of your clock and minimize skew. See **Section 5 Clocks and Power Control** of the *MPC823e Reference Manual* for more detailed information.

- **Choose Oscillators Instead of Crystals**
  If you can afford the power dissipation and higher cost of using an oscillator instead of a crystal for the clock input source, choose an oscillator. Often, crystal circuits must be tweaked after the die goes through a geometry shrink. If you need to use both an oscillator and a crystal on the same design and if the crystal is the main source for the system clock, you should gate off the external clock. You can use oscillators and crystals simultaneously on the MPC823e. However, you should not use the crystal on the EXTAL and XTAL pins and, to prevent excessive jitter, you should leave the oscillator free running into the EXTCLK pin. If you are not using a crystal, then ground the EXTAL pin. If the crystal is only used for the real-time clock and the main clock source is from the oscillator, then gating is not required.

- **Place the Crystal Within 0.5 Inches of the MPC823e**
  The crystal and the XFC capacitor must be as close to the chip as possible.

- **Do Not Use an RC Filter on the VDDSYN Pin**
  You should use an LC filter instead.

Electrical Considerations

- **Determine the Proper Value for your External Filter Capacitor (XFC)**
  The following table illustrates how to compute the minimum, maximum, and recommended values of the XFC capacitor, as a function of the MF field in the PLPRCR register. Please consult **Section 5 Clocks and Power Control** of the *MPC823e Reference Manual* for more information.

MF RANGE	RECOMMENDED CAPACITANCE	MINIMUM CAPACITANCE	MAXIMUM CAPACITANCE	UNIT
MF <= 4	680 * (MF+1) - 120	580 * (MF+1) - 100	780 * (MF+1) - 140	pF
MF > 4	1100 * (MF+1)	830 * (MF+1)	1470 * (MF+1)	pF

- **Remember Not All MPC823 Pins Are 5 Volt Friendly**
  Although the MPC823 and MPC823e supports 5V inputs, EXTAL, XTAL, and EXTCLK are not 5V friendly inputs. Inputs on those signals are limited to VCC + 0.3V. The only pins on the MPC823e that are 5V friendly are the PCMCIA and parallel port pins.

- **Do Not Use a 2.2 Voltage Source for Frequencies Greater Than 25MHz**
  If 2.2 is the voltage source for the VDDL pins, then the maximum frequency of the device is 25MHz. Otherwise, the VDDL power plane should be connected to a 3.3V source.

- **Use Multiple Power and Ground Planes**
  You should use at least one ground plane, one 3.3V VCC plane, and one 5V VCC plane (if 5V parts exist in the system). This ensures easy routing to and from the MPC823e.

- **Decouple the Analog Power Plane**
  The VDDSYN pin is routed to a via that punches down to a mini plane (a peninsula on a signal layer), which is decoupled from VSSSYN with 10µF and 0.1µF parallel caps and also attaches to the 3.3V plane through a 8.2mH inductor. The 3.3V and 5V planes have a keep-out region in the PLL power plane area. You should separate the PLL VSSSYN from global ground by splitting the plane with a connection point as close to the power supply as possible. On other layers, signals are kept out of this area. You should also place the PLL loop filter and decoupling caps close to the MPC823e.

- **Improve DRAM Signal Integrity**
  If you are using DRAM SIMMs in your design, use series dampening resistors on all memory control lines to improve signal integrity.

- **Use Pull-Ups and Pull-Downs**
  We suggest following pins must be pulled-up/pulled-down with an appropriate value to ensure higher frequency operation:

PIN	Resistor Value
- $\overline{BR}$	4.7K
- $\overline{BB}$	2K
- $\overline{BI}$	4.7K
- $\overline{TA}$	2K
- $\overline{TEA}$	2K
- $\overline{DSCK}$	1K Pull-down

- **Do Not Leave Unused Input Pins Floating**
  Floating input and tri-state input pins may cause excessive current draw in low-power modes. The address and data bus signals are OK because the MPC823e can pull them down internalls with the FIOPD bit in the PLPRCR. All other unused input pins and tri-state input pins need to pulled high, ie TSIZx, R_W, DPx, IRQ0-7. Also, coming out of reset the $\overline{GPL\_A4}$/UPWAITA/$\overline{AS}$ and GPL_B4/UPWAITB are inputs and, if unused, need to be set as outputs or pulled high.

- **Floating Pins can Cause Over 100µA of Current Each.**
  Due to varying voltage levels on floating inputs, not every device will indicate a higher than expected current consumption, so it is important that you ensure that your design is properly terminated. You may want to test a large sample (>30) for verification of your low-power configuration and design.

- **When You Are Not Using the Port Pins, Configure Them as Outputs**
  The parallel port pins do not have internal pull-ups or pull-downs. Therefore, unused parallel I/O pins should be configured as outputs after reset and left unconnected.
- **Avoid Contentions on Lines**
  Do not set a pin high while it is being externally driven low.
- **TMS and TDI**
  TMS and TDI need to be either disconnected or pulled high. They have weak internal pull-ups.
- **Consider MODCKx Pin Configuration**
  You can configure the MODCKx pins to become outputs after reset by driving them with three-state buffers enabled by HRESET, but not PORESET since it has a slow rising edge.
- **Connect $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$**
  Connect $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$ through a diode, pointing towards PORESET~.
- **Driving $\overline{\text{SRESET}}$**
  The MPC823e can drive the soft reset pin ($\overline{\text{SRESET}}$) as an output. It is driven by the MPC823e any time that $\overline{\text{PORESET}}$ or $\overline{\text{HRESET}}$ is asserted, and also if a RESET command is delivered to the debug port.
- **Properly Configure CPM General-Purpose IO (GPIO) Pins**
  When CPM inputs are externally driven by a device that enters its own low-power mode with tri-stated pins, change the GPIO pin to outputs, and set the value so that it will not cause a problem.
  - Signal the external device to shutdown.
  - Change the GPIO direction to output.
  - Enter a low power mode.
  - On wakeup from low power mode, change GPIO direction
  - Wakeup external device
- **Decide Whether Or Not You Need PCMCIA Buffers**
  Although there are buffers in PCMCIA design examples these buffers on the address or data bus are only required if the address or data bus is heavily loaded, if you are designing a 2-slot PCMCIA system, or if the board needs to be protected by a PCMCIA card hot plug-in. Keep in mind that the MPC823e supports one PCMCIA slot.
- **Optimize Memory-to-Memory IDMA Transfers**
  If you need to use the IDMA in memory-to-memory mode, you must assert the DREQx pin. You can either ground the pin or use a parallel I/O pin to selectively enable the DREQx function. Using the parallel I/O pin is recommended, which saves the RISC microcontroller overhead since it has to poll the IDMA buffer descriptors to see if the valid (V) bit has been set.

Reset Considerations

- **Actively Drive the Data Bus During Reset Configuration**
  Driving the data bus with an active device instead of pull-ups during reset configuration ensures that the appropriate value is written into the configuration register. If you do or do not use pull-ups on the data bus and default hard reset configuration word is acceptable, tie the $\overline{\text{RSTCONF}}$ pin high. If you want to change the hard reset configuration word to something other than the default, drive the appropriate data bus lines low with an active device and connect the

RSTCONF pin to ground. If the default hard reset configuration word is not acceptable and power consumption is a concern, drive the appropriate data lines high with an active device and connect the RSTCONF pin to ground. If power consumption is not a concern, you can use pull-ups on the appropriate data lines for your hard reset configuration word. See **Section 4 Reset** of the *MPC823e Reference Manual* for additional information.

Software Considerations

- **Remember PowerPC Byte Lane Architecture**
  If you are using an 8-bit wide memory/EPROM, attach the device to byte lane zero (D0-D7). In PowerPC architecture, D0-D7 is the highest order byte lane on the data bus and D0 is the highest order pin of that byte lane. D0-D7 corresponds to write enable 0 (WE0) and Byte Select A or B 0 (BS_x0). D0-D7 is associated with WE0 and BS_x0. D15-D8 is associated with WE1 and BS_x1, D23-D16 is associated with WE2 and BS_x2, and D31-D24 is associated with WE3 and BS_x3. The most significant bit is D0 and the least significant bit is D31.

- **Remember the PowerPC Addressing Convention**
  On the MPC823e, the highest order address pin is A6. For all MPC8xx microprocessors, the lowest order address pin is A31.

- **Using MMUlite with a Display**
  With a few simple additions, MMU lite can almost remove the need for using dynamic translations. More than one MPC823e TLB can point to the same physical memory, so long as their virtual memory addresses are different. For example, we could setup TLB 1 to make all of DRAM with the caches on and set to copyback. TLB 2 can be set with caches on and writethrough, and TLB 3 with cache inhibit. Each one will need its own virtual address, but they can all point to the same physical DRAM. Normal variables can be accesses through TLB1, the display through TLB2, and CPM buffers through TLB3. Remember the CPM always deals with real addresses.

- **Don't Cache Internal Memory Space**
  Internal Memory Space, configured in the Hard Reset Configuration Word, must not be in a data-cached region. If it is, erratic operation may occur. See **Section 4 Reset** in the *MPC823e Reference Manual*.

- **When Using 2 MB FLASH and Larger, Set ~IIP=1**
  Setting the ~IIP=1 in the Hard Reset Configuration Word will cause the Initial PowerPC Interrupt Table base address to be 0x0. This will ensure that the Interrupt Table, at boot time, will always be in the same location in the FLASH, namely the beginning, regardless of the size of the FLASH. See **Section 4 Reset** in the *MPC823e Reference Manual*.

- **External Interrupt Setup and Access**
  For external interrupt pins, if a request signal is a pulse, the interrupt request pin should be configured to "edge detect mode". See the subsection on Interrupt Configuration in **Section 12 System Interface Unit** of the *MPC823e Reference Manual*. This ensures that the interrupt will be recognized even if interrupts are temporarily blocked or disabled by the software. The interrupt service routine (ISR) should clear the edge status flag after the ISR is entered and prior to setting the EE bin in the MSR (Machine Status Register). If the ISR waits until after the EE bit is set, a second interrupt may be taken. If a request signal is a "standard handshake", the assertion is asynchronous, but the negation occurs upon request from the ISR. This ensures that the interrupt is taken and the source of the interrupt is known. The timing with respect to the EE bit is the same.

To avoid spurious interrupts, interrupt masks should not be set while interrupts might be sent to the core. Likewise, no interrupts should be disabled while the interrupt might be pending at the core. That way, when the core responds to the interrupt request, the request will still be pending and the core can determine the source of the interrupt. To accomplish all of the above, the EE bit should be disabled when masks are set or when interrupt enables are cleared.

- **Writing to the ICTRL Register**
  If you use the mtspr instruction to set the Ignore First Match (IFM) bit of the ICTRL register at the same time you set an instruction breakpoint on this instruction, the chip will behave unpredictably. The workaround is to disable instruction breakpoints when setting the IFM bit.

- **Overlapping Parameter RAM Tables for Ethernet and SPI (MPC823 Only)**
  The address range in Parameter RAM (PRAM) for Ethernet is (DPRAM_Base + 0x1d00 ... 0x1da3). The address range in Parameter RAM for SPI is (DPRAM_Base + 0x1d80 ... 0x1daf). If you require concurrent operation of SPI and Ethernet then download the Microcode Patch which relocates the SPI PRAM.

- **Don't Let Internal Memory Space and the PowerPC Interrupt Table Overlap**
  Make sure the ISB (Initial Internal Space Base) and the PowerPC Interrupt Table base location do not overlap each other. The IIP (Initial Interrupt Prefix) bit in the Hard Reset Configuration Word determines the initial PowerPC Interrupt Table base address, after reset. The Interrupt Table includes the Reset Vector (offset 0x100), where execution begins after reset. The ISB field in the Hard Reset Configuration Word determines the base address of the Internal Memory Space. If there is an overlap, the PowerPC core may fetch instructions from Internal Memory space, leading to erratic operation. See **Section 4 Reset** in the *MPC823e Reference Manual*.

Ethernet Considerations

- **The MC68160 Is Not Recommended for New Designs**
  The Motorola MC68160 Enhanced Ethernet Transceiver, which is featured in the MPC823FADS, is no longer recommended for new designs. Level One and AMD are alternative sources of ethernet transceivers for use with the MPC823e.

LCD Considerations

- **Choose an LCD Panel that Works with a 4-Clock Cycle HSYNC Pulse**
  The MPC823e LCD controller is specifically designed to operate with panels that take an HSYNC pulse of 4 clock cycles in length. See the **Section 18 LCD Controller** in the *MPC823e Reference Manual*.

- **Caching the LCD/Video Frame Buffer**
  If you are manipulate bit fields on the LCD frame buffer for graphic drawings, it's recommended you mark the frame buffer as cacheable write-through. This will help cut down the bandwidth consumption due to read accesses and yet still keep the picture coherence with what in the cache. Otherwise, you should mark the frame buffer as cache-inhibited. An easy way to setup the caches with the LCD controller is covered under *Using MMUlite with a Display.*

- **Differences Between the MPC823e and MPC821 LCD Controllers**
  The MPC823e uses 4 bits to encode each of Red, Green, and Blue (RGB) for TFT displays only in the LCD Color RAM words. The MPC821 uses 3 bits to encode each color. This is the only difference.

- **Understand the Factors that Limit the Maximum Display Resolution**

1) **HPC**—Horizontal Pixel Count (this is a field in the LCHCR), which is related to the number of pixels per line on the panel, by Table 18-2 in the *MPC823e Reference Manual*. The maximum value for HPC is 2047.

2) **VPC**—Vertical Pixel Count (this is a field in the LCVCR), which is related to the number of lines on the panel by Table 18-3 in the *MPC823e Reference Manual*. The maximum value for VPC is 1023.

3) **BNUM**—Memory Bursts per Frame (this is a field in the LCCR). The maximum value for BNUM is 32767.

From the maximum value allowed by BNUM, we can compute maximum values for H (number of lines), and W (number of pixels per line), assuming BPIX = 8.

BNUM = W * H * BPIX / 128 = 32767

H * W = 524272 but, W = 4/3 * H assuming a standard 4/3 aspect ratio (e.g., 640x480, 1024x768, etc...)

4/3 * H * H = 524272

H = 627 (approx.)

W = 836 (approx.)

So, 800x600 is the maximum standard resolution at 8 bits per pixel.

4) **Bus Bandwidth—**We recommend not exceeding 45% bus utilization for the LCD panel.

Assuming a design using SDRAM with a timing of 4-1-1-2 (8 clocks per burst), running at 50 MHz system frequency, and again assuming 8 bits per pixel.

LCD Panel bandwidth = 45% * 50 MHz / 8 clocks per burst * 16 bytes per burst = 45 MB/s

Assume a frame rate of 100 frames/s

Number of bytes per frame = 45 MB/s / 100 frames/s = 450,000

Number of pixels per frame = 450,000 again, assuming 8 bits per pixel

H * W = 450000 again, assuming a standard 4/3 aspect ratio, as in the above example,

4/3 * H * H = 450000

W = 580 (approx.)

H = 774 (approx.)

However, by running slightly above the recommended bus utilization (at 48%), you could again select a resolution of 800x600.

Memory Map

ADDRESS	REGISTER	SIZE	PAGE #
SYSTEM INTERFACE UNIT			
000	SIUMCR—SIU Module Configuration Register	32	Section 12-30
004	SYPCR—System Protection Control Register	32	Section 12-35
008 to 00D	RES—Reserved	—	—
00E	SWSR—Software Service Register	16	Section 12-27
010	SIPEND—SIU Interrupt Pending Register	32	Section 12-7
014	SIMASK—SIU Interrupt Mask Register	32	Section 12-8
018	SIEL—SIU Interrupt Edge/ Level Register	32	Section 12-9
01C	SIVEC—SIU Interrupt Vector Register	32	Section 12-10
020	TESR—Transfer Error Status Register	32	Section 12-36
024 to 02F	RES—Reserved	—	—
030	SDCR—SDMA Configuration Register	32	16-86
034 to 07F	RES—Reserved	—	—
PCMCIA			
080	PBR0—PCMCIA Interface Base Register 0	32	Section 17-16
084	POR0—PCMCIA Interface Option Register 0	32	Section 17-17

ADDRESS	REGISTER	SIZE	PAGE #
088	PBR1—PCMCIA Interface Base Register 1	32	Section 17-16
08C	POR1—PCMCIA Interface Option Register 1	32	Section 17-17
090	PBR2—PCMCIA Interface Base Register 2	32	Section 17-16
094	POR2—PCMCIA Interface Option Register 2	32	Section 17-17
098	PBR3—PCMCIA Interface Base Register 3	32	Section 17-16
09C	POR3—PCMCIA Interface Option Register 3	32	Section 17-17
0A0	PBR4—PCMCIA Interface Base Register 4	32	Section 17-16
0A4	POR4—PCMCIA Interface Option Register 4	32	Section 17-17
0A8	PBR5—PCMCIA Interface Base Register 5	32	Section 17-16
0AC	POR5—PCMCIA Interface Option Register 5	32	Section 17-17
0B0	PBR6—PCMCIA Interface Base Register 6	32	Section 17-16
0B4	POR6—PCMCIA Interface Option Register 6	32	Section 17-17
0B8	PBR7—PCMCIA Interface Base Register 7	32	Section 17-16
0BC	POR7—PCMCIA Interface Option Register 7	32	Section 17-17
0C0 to 0E3	RES—Reserved	—	—
0E4	PGCRB—PCMCIA Interface General Control Register B	32	Section 17-15

ADDRESS	REGISTER	SIZE	PAGE #
0E8	PSCR—PCMCIA Interface Status Change Register	32	Section 17-11
0EC to 0EF	RES—Reserved	—	—
0F0	PIPR—PCMCIA Interface Input Pins Register	32	Section 17-9
0F4 to 0F7	RES—Reserved	—	—
0F8	PER—PCMCIA Interface Enable Register	32	Section 17-13
0FC to 0FF	RES—Reserved	—	—
MEMORY CONTROLLER			
100	BR0—Base Register Bank 0	32	Section 15-9
104	OR0—Option Register Bank 0	32	Section 15-11
108	BR1—Base Register Bank 1	32	Section 15-9
10c	OR1—Option Register Bank 1	32	Section 15-11
110	BR2—Base Register Bank 2	32	Section 15-9
114	OR2—Option Register Bank 2	32	Section 15-11
118	BR3—Base Register Bank 3	32	Section 15-9
11C	OR3—Option Register Bank 3	32	Section 15-11
120	BR4—Base Register Bank 4	32	Section 15-9
124	OR4—Option Register Bank 4	32	Section 15-11

ADDRESS	REGISTER	SIZE	PAGE #
128	BR5—Base Register Bank 5	32	Section 15-9
12C	OR5—Option Register Bank 5	32	Section 15-11
130	BR6—Base Register Bank 6	32	Section 15-9
134	OR6—Option Register Bank 6	32	Section 15-11
138	BR7—Base Register Bank 7	32	Section 15-9
13C	OR7—Option Register Bank 7	32	Section 15-11
140 to 163	RES—Reserved	—	—
164	MAR—Memory Address Register	32	Section 15-26
168	MCR—Memory Command Register	32	Section 15-17
16C to 16F	RES—Reserved	—	—
170	MAMR—Machine A Mode Register	32	Section 15-19
174	MBMR—Machine B Mode Register	32	Section 15-22
178	MSTAT—Memory Status Register	16	Section 15-15
17A	MPTPR—Memory Periodic Timer Prescaler	16	Section 15-27
17C	MDR—Memory Data Register	32	Section 15-26
180 to 1FF	RES—Reserved	—	—

ADDRESS	REGISTER	SIZE	PAGE #
SYSTEM INTEGRATION TIMERS			
200	TBSCR—Timebase Status and Control Register	16	Section 12-16
204	TBREFU—Timebase Reference Register Upper	32	Section 12-15
208	TBREFL—Timebase Reference Register Lower	32	Section 12-15
20C to 21F	RES—Reserved	—	—
220	RTCSC—Real-Time Clock Status and Control Register	16	Section 12-18
224	RTC—Real-Time Clock Register	32	Section 12-19
228	RTSEC—Real-Time Clock Alarm Seconds Register	32	Section 12-20
22C	RTCAL—Real-Time Clock Alarm Register	32	Section 12-21
230 to 23F	RES—Reserved	—	—
240	PISCR—Periodic Interrupt Status and Control Register	16	Section 12-23
244	PITC—Periodic Interrupt Timer Count Register	32	Section 12-24
248	PITR—Periodic Interrupt Timer Register	32	Section 12-25
24C to 27F	RES—Reserved	—	—
CLOCKS AND RESET			
280	SCCR—System Clock and Reset Control Register	32	Section 5-3
284	PLPRCR—PLL, Low-Power and Reset Control Register	32	Section 5-7

ADDRESS	REGISTER	SIZE	PAGE #
288	RSR—Reset Status Register	32	Section 4-5
28C to 2FF	RES—Reserved	—	—
SYSTEM INTEGRATION TIMERS KEYS			
300	TBSCRK—Timebase Status and Control Register Key	32	Section 5-27
304	TBREFFUK—Timebase Reference Register Upper Key	32	Section 5-27
308	TBREFFLK—Timebase Reference Register Lower Key	32	Section 5-27
30C	TBK—Timebase and Decrementer Register Key	32	Section 5-27
310 to 31F	RES—Reserved	—	—
320	RTCSCK—Real-Time Clock Status and Control Register Key	32	Section 5-27
324	RTCK—Real-Time Clock Register Key	32	Section 5-27
328	RTSECK—Real-Time Alarm Seconds Key	32	Section 5-27
32C	RTCALK—Real-Time Alarm Register Key	32	Section 5-27
330 to 33F	RES—Reserved	—	—
340	PISCRK—Periodic Interrupt Status and Control Register Key	32	Section 5-27
344	PITCK—Periodic Interrupt Count Register Key	32	Section 5-27
348 to 37F	RES—Reserved	—	—

ADDRESS	REGISTER	SIZE	PAGE #
CLOCKS AND RESET KEYS			
380	SCCRK—System Clock Control Key	32	Section 5-27
384	PLPRCRK—PLL, Low Power and Reset Control Register Key	32	Section 5-27
388	RSRK—Reset Status Register Key	32	Section 5-27
38C to 7FF	RES—Reserved	—	—
VIDEO CONTROLLER			
800	VCCR—Video Controller Configuration Register	16	Section 19-5
802 to 803	RES—Reserved	16	—
804	VSR—Video Status Register	8	Section 19-7
805	RES—Reserved	8	—
806	VCMR—Video Controller Command Register	8	Section 19-8
807	RES—Reserved	8	—
808	VBCB—Video Background Color Buffer Register	32	Section 19-9
80C to 80F	RES—Reserved	16	—
810	VFCR0—Video Frame Configuration Register (Set 0)	32	Section 19-10
814	VFAA0—Video Frame Buffer A Start Address Register (Set 0)	32	Section 19-11
818	VFBA0—Video Frame Buffer B Start Address Register (Set 0)	32	Section 19-12

ADDRESS	REGISTER	SIZE	PAGE #
81C	VFCR1—Video Frame Configuration Register (Set 1)	32	Section 19-13
820	VFAA1—Video Frame Buffer A Start Address Register (Set 1)	32	Section 19-14
824	VFBA1—Video Frame Buffer B Start Address Register (Set 1)	32	Section 19-15
828 to 83F	RES—Reserved	—	—
LCD CONTROLLER			
840	LCCR—LCD Panel Configuration Register	32	Section 18-21
844	LCHCR—LCD Horizontal Control Register	32	Section 18-23
848	LCVCR—LCD Vertical Configuration Register	32	Section 18-25
84C to 84F	RES—Reserved	—	—
850	LCFAA—LCD Frame Buffer A Start Address	32	Section 18-27
854	LCFBA—LCD Frame Buffer B Start Address	32	Section 18-28
858	LCSR—LCD Status Register	8	Section 18-29
859 to 85F	RES—Reserved	—	—
I^2C CONTROLLER			
860	I2MOD—I^2C Mode Register	8	16-473
864	I2ADD—I^2C Address Register	8	16-478

ADDRESS	REGISTER	SIZE	PAGE #
868	I2BRG—I^2C Baud Rate Generator Register	8	16-479
86C	I2COM—I^2C Command Register	8	16-479
870	I2CER—I^2C Event Register	8	16-480
874	I2CMR—I^2C Mask Register	8	16-481
875 to 8FF	RES—Reserved	—	—
DMA CONTROLLER			
900 to 903	RES—Reserved	—	—
904	SDAR—SDMA Address Register	32	16-90
908	SDSR—SDMA Status Register (DSP Interrupts)	8	16-88
909 to 90B	RES—Reserved	—	—
90C	SDMR—SDMA Mask Register (DSP Interrupts)	8	16-34, 16-89
90D to 90F	RES—Reserved	—	—
910	IDSR1—IDMA1 Status Register	8	16-95
911 to 913	RES—Reserved	—	—
914	IDMR1—IDMA1 Mask Register	8	16-96
915 to 917	RES—Reserved	—	—
918	IDSR2—IDMA2 Status Register	8	16-95
919 to 91B	RES—Reserved	—	—

ADDRESS	REGISTER	SIZE	PAGE #
91C	IDMR2—IDMA2 Mask Register	8	16-96
91D to 92F	RES—Reserved	—	—
COMMUNICATIONS PROCESSOR MODULE INTERRUPT CONTROLLER			
930	CIVR—CPM Interrupt Vector Register	16	16-516
932 to 93F	RES—Reserved	—	—
940	CICR—CPM Interrupt Configuration Register	32	16-511
944	CIPR—CPM Interrupt Pending Register	32	16-513
948	CIMR—CPM Interrupt Mask Register	32	16-514
94C	CISR—CPM Interrupt In-Service Register	32	16-515
PARALLEL PORTS			
950	PADIR—Port A Data Direction Register	16	16-486
952	PAPAR—Port A Pin Assignment Register	16	16-486
954	PAODR—Port A Open-Drain Register	16	16-485
956	PADAT—Port A Data Register	16	16-485
958 to 95F	RES—Reserved	—	—
960	PCDIR—Port C Data Direction Register	16	16-497
962	PCPAR—Port C Pin Assignment Register	16	16-498
964	PCSO—Port C Special Options Register	16	16-498

ADDRESS	REGISTER	SIZE	PAGE #
966	PCDAT—Port C Data Register	16	16-497
968	PCINT—Port C Interrupt Control Register	16	16-500
96A to 96F	RES—Reserved	—	—
970	PDDIR—Port D Data Direction Register	16	16-502
972	PDPAR—Port D Pin Assignment Register	16	16-503
974	RES—Reserved	—	—
976	PDDAT—Port D Data Register	16	16-502
978 to 97F	RES—Reserved	—	—
CPM TIMERS			
980	TGCR—Timer Global Configuration Register	16	16-78
982 to 98F	RES—Reserved	—	—
990	TMR1—Timer1 Mode Register	16	16-79
992	TMR2—Timer2 Mode Register	16	16-79
994	TRR1—Timer1 Reference Register	16	16-80
996	TRR2—Timer2 Reference Register	16	16-80
998	TCR1—Timer1 Capture Register	16	16-81
99A	TCR2—Timer2 Capture Register	16	16-81
99C	TCN1—Timer1 Counter Register	16	16-81

ADDRESS	REGISTER	SIZE	PAGE #
99E	TCN2—Timer2 Counter Register	16	16-81
9A0	TMR3—Timer3 Mode Register	16	16-79
9A2	TMR4—Timer4 Mode Register	16	16-79
9A4	TRR3—Timer3 Reference Register	16	16-80
9A6	TRR4—Timer4 Reference Register	16	16-80
9A8	TCR3—Timer3 Capture Register	16	16-81
9AA	TCR4—Timer4 Capture Register	16	16-81
9AC	TCN3—Timer3 Counter Register	16	16-81
9AE	TCN4—Timer4 Counter Register	16	16-81
9B0	TER1—Timer1 Event Register	16	16-82
9B2	TER2—Timer2 Event Register	16	16-82
9B4	TER3—Timer3 Event Register	16	16-82
9B6	TER4—Timer4 Event Register	16	16-82
9B8 to 9BF	RES—Reserved	—	—

ADDRESS	REGISTER	SIZE	PAGE #
COMMUNICATION PROCESSOR MODULE			
9C0	CPCR—Communication Processor Module Command Register	16	Section 16-9
9C2 to 9C3	RES—Reserved	16	—
9C4 to 9C7	RCCR/RMDS—RISC Controller Configuration Register and RISC Microcode Development Support Control Register	32	Section 16-7
9C8 to 9CB	RES—Reserved	32	—
9CC	RCTR1—RISC Controller Trap Register 1	16	—
9CE	RCTR2—RISC Controller Trap Register 2	16	—
9D0	RCTR3—RISC Controller Trap Register 3	16	—
9D2	RCTR4—RISC Controller Trap Register 4	16	—
9D4 to 9D5	RES—Reserved	—	—
9D6	RTER—RISC Timer Event Register	16	Section 16-23
9D8 to 9D9	RES—Reserved	—	—
9DA to 9DB	RTMR—RISC Timer Mask Register	16	Section 16-23
9DC to 9EF	RES—Reserved	—	—

ADDRESS	REGISTER	SIZE	PAGE #
BAUD RATE GENERATORS			
9F0	BRGC1—BRG1 Configuration Register	32	16-161
9F4	BRGC2—BRG2 Configuration Register	32	16-161
9F8	BRGC3—BRG3 Configuration Register	32	16-161
9FC	BRGC4—BRG4 Configuration Register	32	16-161
UNIVERSAL SERIAL BUS			
a00	USMOD—USB Mode Register	8	16-369
a01	USADR—USB Slave Address Register	8	16-375
a02	USCOM—USB Command Register	8	16-376
A03	RES—Reserved	8	—
a04	USEP0—USB Endooint Configuration 0 Register	16	16-377
a06	USEP1—USB Endooint Configuration 1 Register	16	16-377
a08	USEP2—USB Endooint Configuration 2 Register	16	16-377
a0A	USEP3—USB Endooint Configuration 3 Register	16	16-377
A0C to A0F	RES—Reserved	—	—
a10	USBER—USB Event Register	16	16-380
A12	RES—Reserved	16	—
a14	USBMR—USB Mask Register	16	16-381

ADDRESS	REGISTER	SIZE	PAGE #
A16	RES—Reserved	8	—
a17	USBS—USB Status Register	8	16-381
A18 to A1F	RES—Reserved	—	—
SERIAL COMMUNICATION CONTROLLER 2			
a20	GSMR_L—SCC2 General Mode Low Register	32	16-168
a24	GSMR_H—SCC2 General Mode High Register	32	16-168
a28	PSMR—SCC2 Protocol-Specific Mode Register	16	16-178 16-220 (UART) 16-245 (HDLC) 16-283 (AHDLC) 16-313 (Trans)
A2A to A2B	RES—Reserved	16	—
a2c	TODR—SCC2 Transmit-on-Demand Register	16	16-179
a2e	DSR—SCC2 Data Synchronization Register	16	16-179
a30	SCCE—SCC2 Event Register	16	16-189 16-230 (UART) 16-253 (HDLC) 16-288 (AHDLC) 16-318 (Trans)
A32	RES—Reserved	16	—
a34	SCCM—SCC2 Mask Register	16	16-189 16-232 (UART) 16-256 (HDLC) 16-320 (Trans)
A36	RES—Reserved	8	—

ADDRESS	REGISTER	SIZE	PAGE #
a37	SCCS—SCC2 Status Register	8	16-189 16-233 (UART) 16-257 (HDLC) 16-320 (Trans)
a38	IRMODE—SCC2 Infra-Red Mode Register	16	16-298
A3A	IRSIP—SCC2 Infra-Red Serial Interaction Pulse Control Register	16	16-300
A3C to A3F	RES—Reserved	—	—
SERIAL COMMUNICATION CONTROLLER 3			
A40	GSMR_L— SCC3 General Mode Low Register	32	16-168
A44	GSMR_H — SCC3 General Mode High Register	32	16-168
A48	PSMR—SCC3 Protocol-Specific Mode Register	16	16-178 16-220 (UART) 16-245 (HDLC) 16-283 (AHDLC) 16-313 (Trans)
A4A-A4B	Reserved	16	—
A4C	TODR—SCC3 Transmit-on-Demand Register	16	16-179
A4E	DSR—SCC3 Data Synchronization Register	16	16-179
A50	SCCE—SCC3 Event Register	16	16-189 16-230 (UART) 16-253 (HDLC) 16-288 (AHDLC) 16-318 (Trans)
A52-A53	Reserved	16	—

ADDRESS	REGISTER	SIZE	PAGE #
A54	SCCM—SCC3 Mask Register	16	16-189 16-232 (UART) 16-256 (HDLC) 16-320 (Trans)
A56	Reserved	8	—
A57	SCCS—SCC3 Status Register	8	16-189 16-233 (UART) 16-257 (HDLC) 16-320 (Trans)
A58-A81	Reserved	—	—
SERIAL MANAGEMENT CONTROLLER 1			
A82	SMCMR—SMC Mode Register	16	16-389 16-403 (UART) 16-421 (Trans) 16-436 (GCI)
A84	RES—Reserved	16	—
A86	SMCE—SMC Event Register	8	16-410 (UART) 16-427 (Trans) 16-437 (GCI)
A87 to A89	RES—Reserved	—	—
A8A	SMCM—SMC Mask Register	8	16-412 (UART 16-428 (Trans) 16-438 (GCI)
A8B to A91	RES—Reserved	—	—
SERIAL MANAGEMENT CONTROLLER 2			
A92	SMCMR—SMC Mode Register	16	16-389 16-403 (UART) 16-421 (Trans) 16-436 (GCI)
A94	RES—Reserved	16	—
A96	SMCE—SMC Event Register	8	16-410 (UART) 16-427 (Trans) 16-437 (GCI)
A97 to A99	RES—Reserved	—	—

ADDRESS	REGISTER	SIZE	PAGE #
A9A	SMCM—SMC Mask Register	8	16-412 (UART 16-428 (Trans) 16-438 (GCI)
A9B to A9F	RES—Reserved	—	—
SERIAL PERIPHERAL INTERFACE			
AA0	SPMODE—SPI Mode Register	16	16-448
AA2	RES—Reserved	16	—
AA6	SPIE—SPI Event Register	8	16-457
AA7 to AA9	RES—Reserved	—	—
AAA	SPIM—SPI Mask Register	8	16-458
AAB	RES—Reserved	16	—
AAD	SPCOM—SPI Command Register	8	16-456
AAE to AB7	RES—Reserved	—	—
PORT B			
AB8	PBDIR—Port B Data Direction Register	32	16-492
ABC	PBPAR—Port B Pin Assignment Register	32	16-493
AC0	PBODR—Port B Open-Drain Register	32	16-490
AC4	PBDAT—Port B Data Register	32	16-491
SERIAL INTERFACE			
AE0	SIMODE—Serial Interface Mode Register	32	16-130
AE4	SIGMR—Serial Interface Global Mode Register	8	16-129

ADDRESS	REGISTER	SIZE	PAGE #
AE5	RES—Reserved	8	—
AE6	SISTR—Serial Interface Status Register	8	16-141
AE7	SICMR—Serial Interface Command Register	8	16-140
AE8 to AEB	RES—Reserved	—	—
AEC	SICR—Serial Interface Clock Route Register	32	16-137
AF0	SIRP—Serial Interface RAM Pointer Register	32	16-142
AF4 to AFF	RES—Reserved	—	—
SPECIALIZED RAM			
B00 to BFF	VCRAM—Video Controller RAM Array	256 bytes	Section 19-16
C00 to DFF	SIRAM—Serial Interface RAM	512 bytes	16-123
E00 to FFF	LCOLR—LCD Color RAM	512 bytes	Section 18-30
1000 to 1FFF	RES—Reserved	—	—

POWERPC INSTRUCTIONS

INSTRUCTION	PAGE #		INSTRUCTION	PAGE #
A				
add	B-7		addc	B-8
adde	B-9		addi	B-10
addic	B-11		addic.	B-12
addis	B-13		addme	B-14
addze	B-15		and	B-16
andc	B-17		andi.	B-18
andis.	B-19			
B				
b	B-20		bc	B-21
bcctr	B-23		bclr	B-25
C				
cmp	B-27		cmpi	B-28
cmpl	B-29		cmpli	B-30
cntlzw	B-31		crand	B-32
crandc	B-33		creqv	B-34
crnand	B-35		crnor	B-36
cror	B-37		crorc	B-38
crxor	B-39			
D				
dcbf	B-40		dcbi	B-42
dcbst	B-44		dcbt	B-45
dcbtst	B-46		dcbz	B-47
divw	B-49		divwu	B-51
E				
eciwx	B-53		ecowx	B-55
eieio	B-57		eqv	B-59
extest	21-19		extsb	B-60
extsh	B-61			
I				
icbi	B-62		isync	B-64
L				
lbz	B-65		lbzu	B-66

EXTERNAL SIGNALS

SIGNAL	PIN NUMBER
A[6:31]	See following table for pin breakout.
TSIZ0 REG	F15
TSIZ1	E15
RD/WR	C13
BURST	B10
BDIP GPL_B5	A13
TS	D10
TA	A12
TEA	C11
BI	B12
RSV IRQ2	D9
IRQ4 KR RETRY SPKROUT	B7
D[0:31]	See following table for pin breakout.
DP0 IRQ3	C3
DP1 IRQ4	D4
DP2 IRQ5	D3
DP3 IRQ6	C2
BR	B11
BG	C10
BB	A11
IRQ6 FRZ	A10
IRQ0	N1
IRQ1	N2
IRQ7	N3
CS[0:5]	See following table for pin breakout.

SIGNAL	PIN NUMBER
$\overline{\text{CS6}}$ $\overline{\text{CE1\_B}}$	C14
$\overline{\text{CS7}}$ $\overline{\text{CE2\_B}}$	B15
$\overline{\text{WE0}}$ $\overline{\text{BS\_AB0}}$ $\overline{\text{IORD}}$	D16
$\overline{\text{WE1}}$ $\overline{\text{BS\_AB1}}$ $\overline{\text{IOWR}}$	E16
$\overline{\text{WE2}}$ $\overline{\text{BS\_AB2}}$ $\overline{\text{PCOE}}$	D15
$\overline{\text{WE3}}$ $\overline{\text{BS\_AB3}}$ $\overline{\text{PCWE}}$	F13
$\overline{\text{GPL\_A0}}$ $\overline{\text{GPL\_B0}}$	E13
$\overline{\text{GPL\_A1}}$ $\overline{\text{GPL\_B1}}$ $\overline{\text{OE}}$	C16
$\overline{\text{GPL\_A2}}$ $\overline{\text{GPL\_B2}}$ $\overline{\text{CS2}}$	C15
$\overline{\text{GPL\_A3}}$ $\overline{\text{GPL\_B3}}$ $\overline{\text{CS3}}$	D14
$\overline{\text{GPL\_A4}}$ UPWAITA $\overline{\text{AS}}$	D11
$\overline{\text{GPL\_B4}}$ UPWAITB	B13
$\overline{\text{GPL\_A5}}$	C12
$\overline{\text{PORESET}}$	B3
$\overline{\text{RSTCONF}}$	C5
$\overline{\text{HRESET}}$	B5
$\overline{\text{SRESET}}$	B4
XTAL	A4
EXTAL	A5
XFC	B2
CLKOUT	D1
EXTCLK	A6

SIGNAL	PIN NUMBER
TEXP	D5
WAIT_B	C4
ALE_B DSCK AT1	B8
IP_B0 IWP0 VFLS0	A8
IP_B1 IWP1 VFLS1	C8
IP_B2 IOIS16_B AT2	D7
IP_B3 IWP2 VF2	A9
IP_B4 LWP0 VF0	B9
IP_B5 LWP1 VF1	C9
IP_B6 DSDI AT0	C7
IP_B7 PTR AT3	D8
MODCK1 OP2 STS	D6
MODCK2 OP3 DSDO	B6
PA[15] USBRXD	P16
PA[14] USBOE	R15
PA[13] RXD2	R14
PA[12] TXD2	R13

SIGNAL	PIN NUMBER
PA[9] L1TXDA SMRXD2	N10
PA[8] L1RXDA SMTXD2	T9
PA[7] CLK1 TIN1 L1RCLKA BRGO1	T8
PA[6] CLK2 $\overline{\text{TOUT1}}$ TIN3 L1RCLKB	P8
PA[5] CLK3 TIN2 L1TCLKA BRGO2	T6
PA[4] CLK4 $\overline{\text{TOUT2}}$ TIN4 L1TCLKB	R6
$\overline{\text{PB[31]}}$ $\overline{\text{SPISEL}}$ LCD_A	N14
PB[30] SPICLK TXD3	P15
PB[29] SPIMOSI RXD3	P14
PB[28] SPIMISO BRGO3	T15
PB[27] I2CSDA BRGO1	T14
PB[26] I2CSCL BRGO2	P12
PB[25] SMTXD1 TXD3	N11

SIGNAL	PIN NUMBER
PB[24] SMRXD1 RXD3 L1RXDB	T11
PB[23] $\overline{\text{SMSYN1}}$ $\overline{\text{CTS3}}$ $\overline{\text{SDACK1}}$ L1TSYNCB	T10
PB[22] $\overline{\text{SMSYN2}}$ $\overline{\text{SDACK2}}$ L1RSYNCB	R9
PB[19] L1ST1 LCD_B	R7
PB[18] $\overline{\text{RTS2}}$ L1ST2	P7
PB[17] L1ST3 LCD_C	N7
PB[16] L1RQA L1ST4	R5
PC[15] $\overline{\text{DREQ1}}$ L1ST5 L1TXDB	R16
PC[14] $\overline{\text{DREQ2}}$ $\overline{\text{RTS2}}$ L1ST6	T16
PC[13] L1ST7 RTS3	P13
PC[12] L1RQA L1ST8	T13
PC[11] USBRXP	R10
PC[10] TGATE1 USBRXN	P9
PC[9] $\overline{\text{CTS2}}$	R8

SIGNAL	PIN NUMBER
PC[8] $\overline{\text{CD2}}$ $\overline{\text{TGATE1}}$	N8
PC[7] USBTXP	T5
PC[6] USBTXN	N6
PC[5] L1TSYNCA $\overline{\text{SDACK1}}$ $\overline{\text{CTS3}}$	P6
PC[4] L1RSYNCA $\overline{\text{CD3}}$	T4
PD[15] LD8 VD7	R4
PD[14] LD7 VD6	T3
PD[13] LD6 VD5	P5
PD[12] LD5 VD4	R3
PD[11] LD4 VD3	N5
PD[10] LD3 VD2	T2
PD[9] LD2 VD1	P4
PD[8] LD1 VD0	T1
PD[7] LD0 FIELD	R2
PD[6] LCD_AC LOE BLANK	R1

SIGNAL	PIN NUMBER
PD[5] FRAME VSYNC	P2
PD[4] LOAD HSYNC	P3
PD[3] SHIFT/CLK CLK	N4
Power Supply	See following table for pin breakout.
TCK DSCK	T12
TMS	R12
TDI DSDI	R11
TDO DSDO	N12

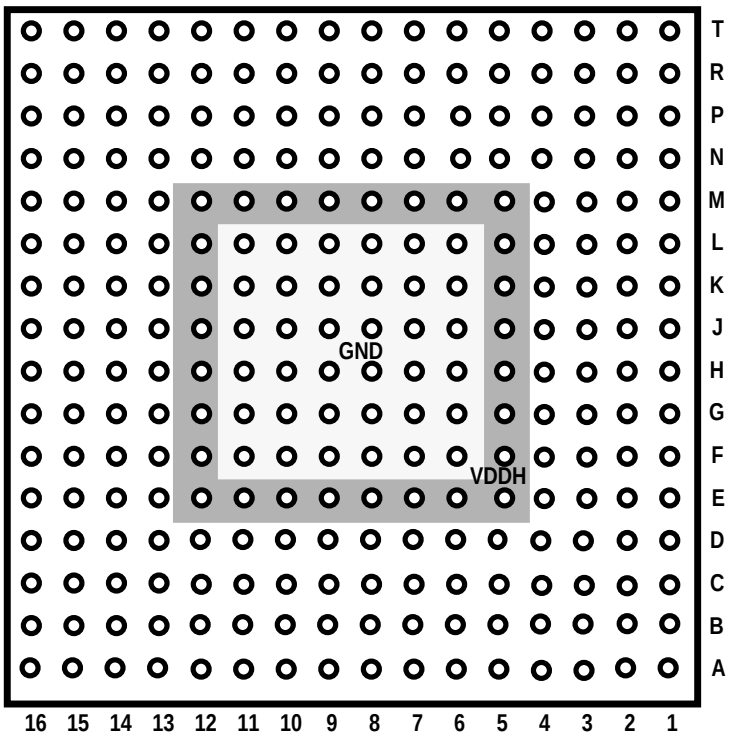
	SIGNAL	PIN #
ADDRESS BUS PINS	A6	M13
	A7	N15
	A8	N16
	A9	M15
	A10	L13
	A11	M16
	A12	M14
	A13	L14
	A14	L15
	A15	L16
	A16	K14
	A17	K13
	A18	G13
	A19	K15
	A20	J15
	A21	J14
	A22	G14
	A23	H15
	A24	H13
	A25	H14
	A26	F14
	A27	K16
	A28	G16
	A29	H16
	A30	G15

	SIGNAL	PIN #
	A31	F16
DATA BUS PINS	D0	M1
	D1	L1
	D2	J2
	D3	J1
	D4	L2
	D5	H1
	D6	F1
	D7	E1
	D8	M2
	D9	K2
	D10	K3
	D11	K1
	D12	M4
	D13	M3
	D14	J3
	D15	J4
	D16	H2
	D17	K4
	D18	H3
	D19	G2
	D20	G3
	D21	F2
	D22	H4
	D23	L4

	SIGNAL	PIN #
	D24	F3
	D25	G4
	D26	E4
	D27	L3
	D28	F4
	D29	E2
	D30	D2
	D31	E3
CHIP SELECT PINS	$\overline{CS0}$	D12
	$\overline{CS1}$	A14
	$\overline{CS2}$	B14
	$\overline{CS3}$	A15
	$\overline{CS4}$	B16
	$\overline{CS5}$	D13
	$\overline{CS6}$	C14
	$\overline{CS7}$	B15
POWER SUPPLY PINS	VDDH	E5–12, F5, F12, G5, G12, H5, H12, J5, J12, K5, K12, L5, L12, M5–M12
	VDDL	A7, G1, J16, T7
	VDDSYN	B1
	KAPWR	A3

	SIGNAL	PIN #
	VSSSYN	A1
	VSSSYN1	A2
	GND	F6–F11, G6–G11, H6–H11, J6–J11, K6–K11, L6–L11
NO CONNECT PINS	N/C	A16, C1, C6, E14, J13, N9, N13, P1, P10

MPC823e Pinout (Top View)



RISC MICROCONTROLLER COMMANDS

The following commands are explained in more detail on page 16-12 of the *MPC823e Reference Manual*.

- ARM IDMA
- CLOSE RX BD
- ENTER HUNT MODE
- GCI ABORT REQUEST
- GCI TIMEOUT
- GRACEFUL STOP TRANSMIT
- INIT DSP
- INIT IDMA
- INIT RX PARAMETERS
- INIT RX AND TX PARAMS
- INIT TX PARAMETERS
- RESTART TRANSMIT
- SET GROUP ADDRESS
- SET TIMER
- START DSP
- STOP IDMA
- STOP TRANSMIT
- USB

MPC8bug COMMANDS

The following commands are explained in more detail in the *MPC8bug User's Manual*, which can be downloaded from the Motorola website.

- A
- ARG
- BR
- BRD
- CAL
- DEF
- EX
- GO
- HELP
- HIS
- LOAD
- LOADF
- LOG
- MBC
- MBF
- MBM
- MBS
- MD
- MM
- NOA
- NOBR
- PAGE
- QUIT
- RD
- RDS
- RESET
- RM
- RMS
- SDEF
- STDIN
- STDOUT
- STDERR
- SYM
- T
- TC
- UPM
- VE