

Freescale Semiconductor, Inc.

ALTIVECPEMAD/D (Motorola Order Number) 3/1999 REV. 0



Errata AltiVec™ Technology Programming Environments Manual Errata

This errata describes corrections to the *AltiVec Technology Programming Environments Manual* (order #: ALTIVECPEM/D, rev. 0) referred to as the PEM. For convenience, the section number and page number are provided.

This document contains information on a new product under development by Motorola. Motorola reserves the right to change or discontinue this product without notice. © Motorola, Inc., 1999. All rights reserved.





Freescale Semiconductor, Inc.

2.1.2. Page 2-4Replace Figure 2-4, "Saving/Restoring the AltiVec Context Register (VRSAVE)" with the following:0123456789101112131415FieldVR0VR3 <th colspan="2" th="" vr3<=""><th>Section</th><th>on #/F</th><th>Page #</th><th>¥</th><th colspan="12">Changes</th></th>	<th>Section</th> <th>on #/F</th> <th>Page #</th> <th>¥</th> <th colspan="12">Changes</th>		Section	on #/F	Page #	¥	Changes											
(VRSAVE)'' with the following: $(VRSAVE)'' with the following:$	2.1.2, Page 2-4 Replace Figure 2-4, "Saving/Restoring the AltiVec Context Reg										gister							
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 Field VR0 VR1 VR2 VR3 VR4 VR5 VR6 VR7 VR8 VR10 VR11 VR12 VR13 VR14 VR15 Reset 0000_0000_0000_0000_0000 0000_0000_0000 VR10 VR11 VR12 VR13 VR14 VR15 Field VR16 VR17 VR18 VR19 VR20 VR21 VR22 VR23 VR26 VR26 VR29 VR30 VR31 Field VR16 VR17 VR18 VR19 VR20 VR21 VR22 VR26 VR26 VR29 VR30 VR31 VR30 VR30 VR31 VR30 VR31 VR30 VR31 VR30 VR31 VR30 VR30 VR30 VR30 VR31 VR30 VR30 VR30 VR31 VR30 VR30 VR30 VR31 </td <td colspan="12">(VRSAVE)" with the following:</td>	(VRSAVE)" with the following:																	
Field VR0 VR1 VR2 VR3 VR4 VR5 VR6 VR7 VR8 VR9 VR10 VR11 VR13 VR14 VR15 Reset 0000_0000_0000_0000_0000 RW using mfspr or mfspr instructions Image: transmitted inst		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Reset 0000_0000_0000_0000_0000 RW RW using mfspr or mfspr instructions 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 Reset 0000_0000_0000_0000_0000 VR20	Field	VR0	VR1	VR2	VR3	VR4	VR5	VR6	VR7	VR8	VR9	VR10	VR11	VR12	VR13	VR14	VR15	
RW using mfspr or mfspr instructions 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 Reset 0000_0000_0000_0000 RE RW RW using mfspr or mfspr instructions SPR256 2.2, Page 2-9 Figure 2-10—The vector registers are 128 bits wide not 64 bits wide as shown. 4.2.2.4, Page 4-20 Change Table 4-9 as follows: • • • • • • • • • • • • • • • • • • • •	Reset		0000_0000_0000															
16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 Field VR16 VR16 VR16 VR19 VR19 VR20 VR21 VR22 VR23 VR26 VR26 VR26 VR26 VR28 VR29 VR30 VR31 Reset 0000_0000_0000_0000 RW SPR26 2.2, Page 2-9 Figure 2-10 — The vector registers are 128 bits wide not 64 bits wide as shown. 42.2.2.4, Page 4-20 Change Table 4-9 as follows: • the memonic for Vector Round to Floating-Point Integer Nearest should be vrfin not fvrfin. • the mnemonic for Vector Round to Floating-Point Integer toward Zero should be vrfin, not fvrfin. • the mnemonic for Vector Round to Floating-Point Integer toward Minus Infinity should be vrfin, not fvrfin. • the mnemonic for Vector Round to Floating-Point Integer toward Minus Infinity should be vrfin, not fvrfin. • Change the mfvscr encoding as shown below (note: bit 31 is not 0): 0 5 6 10 11 15	R/W	R/W using mfspr or mtspr instructions																
Field VR16 VR17 VR18 VR19 VR20 VR21 VR22 VR22 VR26 VR27 VR28 VR29 VR30 VR31Reset0000_0000_0000_0000RWSPR2562.2, Page 2-9Figure 2-10—The vector registers are 128 bits wide not 64 bits wide as shown.4.2.2.4, Page 4-20Change Table 4-9 as follows:• the mnemonic for Vector Round to Floating-Point Integer Nearest should be vrfin not fvrfin.• the mnemonic for Vector Round to Floating-Point Integer toward Zero should be vrfiz, not fvrfiz.• the mnemonic for Vector Round to Floating-Point Integer toward Zero should be vrfiz, not fvrfiz.• the mnemonic for Vector Round to Floating-Point Integer toward Positive Infinity should be vrfip, not fvrfip.• the mnemonic for Vector Round to Floating-Point Integer toward Minus Infinity should be vrfim, not fvrfin.• Change the mfvscr encoding as shown below (note: bit 31 is not 0):04vD00000000000000000000000000000000000		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
Reset 0000_0000_0000 RW using mfspr or mtspr instructions SPR SPR256 2.2, Page 2-9 Figure 2-10—The vector registers are 128 bits wide not 64 bits wide as shown. 4.2.2.4, Page 4-20 Change Table 4-9 as follows: • the mnemonic for Vector Round to Floating-Point Integer Nearest should be vrfin not fvrfin. • the mnemonic for Vector Round to Floating-Point Integer toward Zero should be vrfin, not fvrfiz. • the mnemonic for Vector Round to Floating-Point Integer toward Zero should be vrfin, not fvrfip. • the mnemonic for Vector Round to Floating-Point Integer toward Positive Infinity should be vrfin, not fvrfip. • the mnemonic for Vector Round to Floating-Point Integer toward Positive Infinity should be vrfim, not fvrfin. 6.2, Page 6-24 Change the mfvscr encoding as shown below (note: bit 31 is not 0): 0 5 0 5 0 5 0 5 0 10 0 5 0 10 0 5 0 <td c<="" td=""><td>Field</td><td>VR16</td><td>VR17</td><td>VR18</td><td>VR19</td><td>VR20</td><td>VR21</td><td>VR22</td><td>VR23</td><td>VR24</td><td>VR25</td><td>VR26</td><td>VR27</td><td>VR28</td><td>VR29</td><td>VR30</td><td>VR31</td></td>	<td>Field</td> <td>VR16</td> <td>VR17</td> <td>VR18</td> <td>VR19</td> <td>VR20</td> <td>VR21</td> <td>VR22</td> <td>VR23</td> <td>VR24</td> <td>VR25</td> <td>VR26</td> <td>VR27</td> <td>VR28</td> <td>VR29</td> <td>VR30</td> <td>VR31</td>	Field	VR16	VR17	VR18	VR19	VR20	VR21	VR22	VR23	VR24	VR25	VR26	VR27	VR28	VR29	VR30	VR31
RW RW using mfspr or mtspr instructions SPR SPR256 2.2, Page 2-9 Figure 2-10—The vector registers are 128 bits wide not 64 bits wide as shown. 4.2.2.4, Page 4-20 Change Table 4-9 as follows: • the mnemonic for Vector Round to Floating-Point Integer Nearest should be vrfin not fvrfin. • the mnemonic for Vector Round to Floating-Point Integer toward Zero should be vrfiz, not fvrfiz. • the mnemonic for Vector Round to Floating-Point Integer toward Positive Infinity should be vrfip, not fvrfip. • the mnemonic for Vector Round to Floating-Point Integer toward Positive Infinity should be vrfim, not fvrfin. 6.2, Page 6-24 Change the mfvscr encoding as shown below (note: bit 31 is not 0): 0 5 6 10 11 15 16 20 21 31 6.2, Page 6-25 Change the mfvscr encoding as shown below (note: bit 31 is not 0): 0 5 6 10 11 15 1604 0 31 6.1, Page A-2 Change the mfvscr encoding as shown below (note: bit 31 is not 0): 11 15 1604 0 1604 0 5 6 10 11 15 1604 11 31 A.1, Page A-2 Change the mfvscr encodin	Reset	t0000_0000_0000																
SPR SPR256 2.2, Page 2-9 Figure 2-10—The vector registers are 128 bits wide not 64 bits wide as shown. 4.2.2.4, Page 4-20 Change Table 4-9 as follows: the mnemonic for Vector Round to Floating-Point Integer Nearest should be vrfin not fvrfin. the mnemonic for Vector Round to Floating-Point Integer toward Zero should be vrfiz,not fvrfiz. the mnemonic for Vector Round to Floating-Point Integer toward Positive Infinity should be vrfip, not fvrfip. the mnemonic for Vector Round to Floating-Point Integer toward Minus Infinity should be vrfip, not fvrfin. 6.2, Page 6-24 Change the mfvscr encoding as shown below (note: bit 31 is not 0): 0 5 6 10 11 15 16 20 21 31 6.2, Page 6-25 Change the mfvscr encoding as shown below (note: bit 31 is not 0): 0 5 6 10 11 15 16 20 21 31 A.1, Page A-2 Change the mfvscr encoding as shown below (note: bit 31 is not 0): mfvser 04 00000 00000 00000 1540 	R/W	V R/W using mfspr or mtspr instructions																
2.2, Page 2-9Figure 2-10—The vector registers are 128 bits wide not 64 bits wide as shown.4.2.2.4, Page 4-20Change Table 4-9 as follows: • the mnemonic for Vector Round to Floating-Point Integer Nearest should be vrfin not fvrfin. • the mnemonic for Vector Round to Floating-Point Integer toward Zero should be vrfiz , not fvrfiz. • the mnemonic for Vector Round to Floating-Point Integer toward Positive Infinity should be vrfip , not fvrfip. • the mnemonic for Vector Round to Floating-Point Integer toward Minus Infinity should be vrfim , not fvrfim.6.2, Page 6-24Change the mfvscr encoding as shown below (note: bit 31 is not 0): 0 5 6 0 00000 1540 0 5 6 10 11 15 20 21 31 6.2 , Page 6-25Change the mtvscr encoding as shown below (note: bit 31 is not 0): 0 5 6 10 11 15 20 21 31 $A.1$, Page A-2Change the mtvscr encoding as shown below (note: bit 31 is not 0): mtvscr 04 vD 00000 00000 1540	SPR	SPR SPR256																
as shown. 4.2.2.4, Page 4-20 Change Table 4-9 as follows: • the mnemonic for Vector Round to Floating-Point Integer Nearest should be vrfin not fvrfin. • the mnemonic for Vector Round to Floating-Point Integer toward Zero should be vrfiz , not fvrfiz. • the mnemonic for Vector Round to Floating-Point Integer toward Positive Infinity should be vrfip , not fvrfip. • the mnemonic for Vector Round to Floating-Point Integer toward Positive Infinity should be vrfim , not fvrfin. 6.2, Page 6-24 Change the mfvscr encoding as shown below (note: bit 31 is not 0):	2.2, Page 2-9 Figure 2-10—The vector registers are 128 bits wide not 64 bits wide												wide					
4.2.2.4, Page 4-20Change Table 4-9 as follows:• the mnemonic for Vector Round to Floating-Point Integer Nearest should be vrfin not fvrfin.• the mnemonic for Vector Round to Floating-Point Integer toward Zero should be vrfiz, not fvrfiz.• the mnemonic for Vector Round to Floating-Point Integer toward Positive Infinity should be vrfip, not fvrfip.• the mnemonic for Vector Round to Floating-Point Integer toward Minus Infinity should be vrfim, not fvrfin.6.2, Page 6-24• Change the mfvscr encoding as shown below (note: bit 31 is not 0):• 0• 0• 0• 0• 0• 0• 0• 10• 11• 15• 16• 10• 11• 15• 16• 10• 11• 15• 16• 10• 11• 15• 16• 10• 11• 15• 16• 10• 11• 15• 16• 10• 11• 15• 10• 11• 15• 16• 10• 11• 15• 16• 10• 11• 15• 16• 10• 11• 15• 16• 10• 11• 15• 16• 17• 18• 19• 19• 19• 10• 10• 11 </td <td colspan="12">as shown.</td>	as shown.																	
 the mnemonic for Vector Round to Floating-Point Integer Nearest should be vrfin not fvrfin. the mnemonic for Vector Round to Floating-Point Integer toward Zero should be vrfiz, not fvrfiz. the mnemonic for Vector Round to Floating-Point Integer toward Positive Infinity should be vrfip, not fvrfip. the mnemonic for Vector Round to Floating-Point Integer toward Minus Infinity should be vrfim, not fvrfim. 6.2, Page 6-24 Change the mfvscr encoding as shown below (note: bit 31 is not 0): 0 5 6 10 11 15 16 20 21 31 6.2, Page 6-25 Change the mtvscr encoding as shown below (note: bit 31 is not 0): 0 5 6 10 11 15 16 20 21 31 6.2, Page A-25 Change the mfvscr encoding as shown below (note: bit 31 is not 0): 0 5 6 10 11 15 16 20 21 31 A.1, Page A-2 Change the mfvscr encoding as shown below (note: bit 31 is not 0): 0	4.2.2.4, Page 4-20 Change Table 4-9 as follows:																	
 should be vrfin not fvrfin. the mnemonic for Vector Round to Floating-Point Integer toward Zero should be vrfiz, not fvrfiz. the mnemonic for Vector Round to Floating-Point Integer toward Positive Infinity should be vrfip, not fvrfip. the mnemonic for Vector Round to Floating-Point Integer toward Minus Infinity should be vrfim, not fvrfim. 6.2, Page 6-24 Change the mfvscr encoding as shown below (note: bit 31 is not 0): 0 5 6 10 11 15 16 20 21 31 6.2, Page 6-25 Change the mtvscr encoding as shown below (note: bit 31 is not 0): 0 0 5 6 10 11 15 16 20 21 31 A.1, Page A-2 Change the mfvscr encoding as shown below (note: bit 31 is not 0): mfvser 04 vD 00000 00000 1540 	• the mnemonic for Vector Round to Floating-Point Integer Nearest																	
 the mnemonic for Vector Round to Floating-Point Integer toward Zero should be vrfiz, not fvrfiz. the mnemonic for Vector Round to Floating-Point Integer toward Positive Infinity should be vrfip, not fvrfip. the mnemonic for Vector Round to Floating-Point Integer toward Minus Infinity should be vrfim, not fvrfim. 6.2, Page 6-24 Change the mfvscr encoding as shown below (note: bit 31 is not 0): 0 5 6 10 11 15 16 20 21 31 6.2, Page 6-25 Change the mtvscr encoding as shown below (note: bit 31 is not 0): 0 5 6 10 11 15 16 20 21 31 A.1, Page A-2 Change the mfvscr encoding as shown below (note: bit 31 is not 0): mfvscr 0 0<!--</td--><td></td><td></td><td></td><td></td><td>sho</td><td>ould t</td><td>be vrf</td><td>in no</td><td>t fvrfi</td><td>n.</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td>					sho	ould t	be vrf	in no	t fvrfi	n.								
Zero should be Vrnz, not IVrnz.• the mnemonic for Vector Round to Floating-Point Integer toward Positive Infinity should be vrfip, not fvrfip.• the mnemonic for Vector Round to Floating-Point Integer toward Minus Infinity should be vrfim, not fvrfim.6.2, Page 6-24Change the mfvscr encoding as shown below (note: bit 31 is not 0): 0					• the	mne	moni	c for	Vecto	r Rou	ind to	Floa	ting-l	Point	Integ	er tov	vard	
 the minemonic for vector Round to Floating-Point Integer toward Positive Infinity should be vrfip, not fvrfip. the mnemonic for Vector Round to Floating-Point Integer toward Minus Infinity should be vrfim, not fvrfim. 6.2, Page 6-24 Change the mfvscr encoding as shown below (note: bit 31 is not 0): 0 5 10 11 15 16 20 21 31 6.2, Page 6-25 Change the mtvscr encoding as shown below (note: bit 31 is not 0): 0 5 6 10 11 15 16 20 21 31 6.2, Page 6-25 Change the mtvscr encoding as shown below (note: bit 31 is not 0): 0 5 10 11 15 16 20 21 31 A.1, Page A-2 Change the mfvscr encoding as shown below (note: bit 31 is not 0): mfvscr 04 00000 00000 00000 1540 						ro sho	ould t	e vri	iz,noi	IVrП п D av	Z.	Elec	tin ~ 1	Daint	Inter		huan	
• the mnemonic for Vector Round to Floating-Point Integer toward Minus Infinity should be vrfim, not fvrfim. 6.2, Page 6-24 Change the mfvscr encoding as shown below (note: bit 31 is not 0): 0					• the Pos	sitive	Infin	ity sh	ould	be vr	fip , n	of fvr	fip.	POIIIt	meg		varu	
Minus Infinity should be vrfim, not fvrfim.6.2, Page 6-24Change the mfvscr encoding as shown below (note: bit 31 is not 0): 0 5 6 10 11 15 16 0 <					• the	mne	moni	c for `	Vecto	r Rot	ind to	Floa	ting-l	Point	Integ	er tov	vard	
6.2, Page 6-24 Change the mfvscr encoding as shown below (note: bit 31 is not 0): 0 vD $0 0 0 0 0$ $0 0 0 0 0$ 1540 0 5 6 10 11 15 20 21 31 6.2 , Page 6-25 Change the mtvscr encoding as shown below (note: bit 31 is not 0): 0		Minus Infinity should be vrfim , not fvrfim.																
04 vD $0\ 0\ 0\ 0\ 0$ $0\ 0\ 0\ 0\ 0$ 1540 0 $5\ 6$ $10\ 11$ $15\ 16$ $20\ 21$ 31 6.2 , Page $6-25$ Change the mtvscr encoding as shown below (note: bit 31 is not 0): 04 $0\ 0\ 0\ 0$ $0\ 0\ 0\ 0$ vB 1604 0 $5\ 6$ $10\ 11$ $15\ 16$ $20\ 21$ 31 0.4 $0\ 0\ 0\ 0$ $0\ 0\ 0\ 0$ vB 1604 0 $5\ 6$ $10\ 11$ $15\ 16$ $20\ 21$ 31 A.1, Page A-2 Change the mfvscr encoding as shown below (note: bit 31 is not 0): $mfvscr$ 04 vD $0\ 0\ 0\ 0$ $0\ 0\ 0\ 0$ 1540	6.2, Page 6-24 Change the mfvscr encoding as shown below (note: bit 31 is not 0):																	
0 5 6 10 11 15 16 20 21 31 6.2, Page 6-25 Change the mtvscr encoding as shown below (note: bit 31 is not 0): 0 0 0 0 0 0 10 11 15 16 20 21 31 A.1, Page A-2 Change the mfvscr encoding as shown below (note: bit 31 is not 0): mfvscr 04 vD 00000 00000 1540		04	04		vD		0	00000		00000			1540					
6.2, Page 6-25Change the mtvscr encoding as shown below (note: bit 31 is not 0): 0 0 0 0 0 0 0 0 0 0 0 0 0 5 6 10 11 15 1604 31 0 5 6 10 11 15 1602 31 A.1, Page A-2Change the mfvscr encoding as shown below (note: bit 31 is not 0): mfvscr 04 vD 00000 00000 1540	0		5 6 10 11 15 16 20 21 31															
04 0 0 0 0 0 0 0 0 0 0 vB 1604 0 5 6 10 11 15 16 20 21 31 A.1, Page A-2 Change the mfvscr encoding as shown below (note: bit 31 is not 0): mfvscr 04 vD 00000 00000 1540	6.2, Page 6-25 Change the mtvscr encoding as shown below (note: bit 31 is not 0):																	
0 5 6 10 11 15 16 20 21 31 A.1, Page A-2 Change the mfvscr encoding as shown below (note: bit 31 is not 0): mfvscr 04 vD 00000 00000 1540		04			00000		00000			V		3		1604				
A.1, Page A-2Change the mfvscr encoding as shown below (note: bit 31 is not 0): mfvscr 04 vD 00000000001540	0		5	6		10	11		15 16	6	2	0 21					31	
mfvscr 04 vD 0 0 0 0 0 0 0 0 0 0 1540	A.1, I	Page	4-2		Chang	ge the	e mfv	scr ei	ncodi	ng as	show	n bel	ow (1	note:	bit 31	is no	ot 0):	
	mf	vscr		04		v	D	0	0000		000	0 0			1540			

2

AltiVec[™] Technology Programming Environments Manual Errata

MOTOROLA



Freescale Semiconductor, Inc.

Section #/	Page #			Chang							
A.1, Page	A-2	Change the mtvscr encoding as shown below (note: bit 31 is not 0 and v D should be v B):									
mtvscr	04		00000	00000		v В	1604				
A.2, Page A-9 Change the mfvscr encoding as shown below (note: bit 31 is not 0):											
mfvscr	1 fvscr 000100		vD	00000		00000	110 0000 0100				
A.2, Page	A-9	Change the mtvscr encoding as shown below (note: bit 31 is not 0):									
mtvscr	000100	00000		00000		v В	110 0100 0100				
A.3, Page A-14 Change the mfvscr encoding as shown below (note: bit 31 is not 0):											
mfvscr	04	vD		00000		00000	1540				
A.3, Page A-14 Change the mtvscr encoding as shown below (note: bit 31 is not 0):											
mtvscr	04	00000		00000		vВ	1604				

MOTOROLA

AltiVec[™] Technology Programming Environments Manual Errata



Semiconductor, Inc. eescale

Mfax and AltiVec are trademarks of Motorola, Inc.

The PowerPC name, the PowerPC logotype are trademarks of International Business Machines Corporation used by Motorola under license from International Business Machines Corporation.

Information in this document is provided solely to enable system and software implementers to use PowerPC microprocessors. There are no express or implied copyright licenses granted hereunder to design or fabricate PowerPC integrated circuits or integrated circuits based on the information in this document.

document. Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application or sustain life, or for any other septerts. Motorola does not corvey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out d, directly or indirectly regarding the design or manufacture of the part. Motorola and (\hat{W}) are regulstread trademarke of Motorola. In Motorola host for any dation for the registread trademarke of Motorola host host and (\hat{W}) are regulstread trademarke of Motorola host for any such unintendee of Motorola host host and (\hat{W}) are regulstread trademarke of Motorola host for any such unintendee of Motorola host host and \hat{W} and registread trademarke of Motorola host host and \hat{W} and the registread trademarke of Motorola host host and \hat{W} and \hat{W} and \hat{W} and \hat{W} and thost and \hat{W} and the registread trademarke of M

Motorola and (A) are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Motorola Literature Distribution Centers:

USA/EUROPE: Motorola Literature Distribution; P.O. Box 5405; Denver, Colorado 80217; Tel.: 1-800-441-2447 or 1-303-675-2140; World Wide Web Address: http://ldc.nmd.com/ JAPAN: Nippon Motorola Ltd SPD, Strategic Planning Office 4-32-1, Nishi-Gotanda Shinagawa-ku, Tokyo 141, Japan Tel.: 81-3-5487-8488

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd Silicon Harbour Centre 2, Dai King Street Tai Po Industrial Estate Tai Po, New Territories, Hong Kong

Mfax™: RMFAX0@email.sps.mot.com; TOUCHTONE 1-602-244-6609; US & Canada ONLY (800) 774-1848; World Wide Web Address: http://sps.motorola.com/mfax INTERNET: http://motorola.com/sps

Technical Information: Motorola Inc. SPS Customer Support Center 1-800-521-6274; electronic mail address; crc@wmkmail.sps.mot.com. Document Comments: FAX (512) 895-2638, Attn: RISC Applications Engineering. World Wide Web Addresses: http://www.motorola.com/PowerPC/ http://www.motorola.com/netcomm/

MOTOROLA

ALTIVECPEMAD/D