USB 3D Mouse Interface Reference Design

Designer Reference Manual

M68HC08 Microcontrollers

DRM012/D
Rev. 0.0, 3/2003

MOTOROLA.COM/SEMICONDUCTORS

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USB 3D Mouse Interface Reference Design

Designer Reference Manual — Rev 0

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Section 1. USB 3D Mouse Interface

1.1 Introduction

This document describes a reference design of a Universal Serial Bus 3D Mouse Interface for Microsoft Windows by using the MC68HC08JB1.

For detailed specification on the MC68HC08JB1 device, please refer to the data sheet; Motorola order number: MC68HC08JB1/D.

1.2 Overview

The Motorola MC68HC08JB1 (hereafter referred as JB1) is a member of the HC08 Family of microcontrollers (MCUs). The features of the JB1 include a Universal Serial Bus (USB), which makes this MCU suited for personal computer Human Interface Devices (HID), such as mice. A USB 3D Mouse is demonstrated using the JB1. The main features of the mouse include:

- Fully USB Specification 1.1 compliant
- Windows 98, ME and 2000 compatible
- 3D wheel support

1.3 MC68HC08JB1 Features

The JB1 is targeted for USB and PS/2 interface mouse applications with minimum external components needed. Features to note are:

- USB D+ and D− pins shared with PS/2 data and clock pins
- Eight Keyboard interrupt pins for button press and release detection
- 50mA direct drive pins for the infrared X, Y and Z LEDs
1.4 Hardware Descriptions

**Figure 1-1** shows the block diagram. The solution includes:

- JB1, the USB microcontroller
- Three LEDs for the X, Y and Z directions
- Three corresponding sensors for the X, Y and Z directions
- Three buttons located at the left, under the wheel and at the right

1.5 Firmware Descriptions

The firmware consists of three main parts:

- Main Routine
- USB Handler Routine
- USB Interrupt Routine
Figure 1-2. Firmware Routines.
USB INITIALIZATION

DEVICE CONFIGURED?

NO

YES

MOVEMENT?

NO

YES

CALCULATE MOVEMENT DISPLACEMENT AND DIRECTION TO REPORT

BUTTON STATUS CHANGED?

NO

YES

CONVERT BUTTON CHANGES TO REPORT

NEW ENDPOINT 1 REPORT?

YES

NO

EP1 TX BUFFER EMPTY?

YES

NO

TX EP1 IN REPORT

USB IDLES FOR 6 ms?

NO

YES

SUSPEND DEVICE

DEVICE IS IN SUSPEND

FORCE RESUME

MOVEMENT?

NO

YES

BUS IDLE FOR 5MS?

NO

YES

INTERRUPT?

BUS IDLE FOR 5MS?

YES

NO

MOVEMENT?

FORCE RESUME

Figure 1-3. Main Routine
1.5.1 USB Main Routine

Figure 1-3 shows the flow of the main routine. It detects if there is any movement in the X, Y and Z directions. If there is any movement, it calculates the displacements and directions of the movements, converts them into report format and stores the data in the report buffer. It then checks if there is any button status changes from pressed to released or from released to being pressed. The information is converted into report format and stored in the report buffer. If the USB Endpoint 1 transmit buffer is not full, it copies data from the report buffer to the Endpoint 1 transmit buffer and waits for the host to send an IN token to read the data.

If the USB bus idles for more than 6ms, the routine puts the JB1 into STOP. While JB1 is in STOP, any button press or external IRQ interrupt can wake up the JB1. External RC in the IRQ pin periodically wakes up JB1 to detect if any movement happens as shown in Figure 1-4. If any button press or movement is detected, JB1 sends a resume signal to the host for remote wakeup. If a resume signal from host is detected, JB1 will be woken up and it will not send any resume signal to the host.

![Figure 1-4. RC Timer in Suspend Mode](image)

1.5.2 USB Interrupt Routine

Figure 1-5 shows the flow of the USB interrupt routine. The USB engine automatically responds to a valid USB token with either ACK, NAK or
STALL depending on the registers setting, and ignores it if it is invalid. The firmware has to set the registers for the USB engine to give correct response to the token in different stages. The USB interrupt will be executed whenever there is an EOP, resume signal from host, valid data received or data transmitted. The USB interrupt routine also makes preparation for the next USB transaction and handles any valid command or data received.

Figure 1-7 to Figure 1-8 show the routines for handling the Control Transfers. Control transfers have two or three transaction stages: Setup, Data (optional) and Status as shown below:

• Control Write: SETUP, OUT, OUT... IN
• Control Read: SETUP, IN, IN, IN... OUT
• No Data Control: SETUP, IN

The firmware first distinguishes the kinds of control transfers and does the corresponding preparation for the next stage.
Figure 1-5. USB Interrupt Routine
**Figure 1-6. Setup Routine**

1. Uninstall EP 0 IN & OUT
2. Copy 8 byte setup data to RAM buffer
3. Clear EP0 RX flag
4. Set NAK to IN EP0

- **Standard Device Request?**
  - Yes: Handle Standard Device Request
  - No: Return Stall

- **HID Class Request?**
  - Yes: Handle HID Class Request
  - No: Return Stall

**OUT Endpoint 0 Handler**

- **Status Stage?**
  - Yes: Set NAK to EP0 IN
  - No: Return Stall

- **Valid Data?**
  - Yes: Copy data to buffer
  - No: Return Stall

1. Copy data to buffer
2. Process OUT data

**Figure 1-7. OUT Endpoint 0 Handler**
1.5.3 USB Mouse Report

The mouse implements an HID mouse in interface 0 (endpoint 1) with an extended report to boot protocols. This implementation enables the mouse to work in BIOS setup and in DOS mode. The first 3 bytes of the input reports are identical to the standard mouse boot protocol report (see Table 1-1) as documented in the Device Class Definition for Human Interface Device (HID) version 1.1. This implementation adds one more byte for Z movement to form 4-byte input reports.

Table 1-1. Interface 0 Input Report

<table>
<thead>
<tr>
<th>Byte</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>00</td>
<td>00</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Middle Button</td>
<td>Right Button</td>
<td>Left Button</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X Movement</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Y Movement</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Z Movement</td>
</tr>
</tbody>
</table>
1.6 Firmware Files

Firmware is compiled under CASM08Z.EXE version 3.16 from P&E Microcomputer Systems, Inc.

Table 1-2 summarizes the functions of each firmware file:

<table>
<thead>
<tr>
<th>Files</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>JB8-MSE3.ASM</td>
<td>Define constants and variables</td>
</tr>
<tr>
<td></td>
<td>Movement detection</td>
</tr>
<tr>
<td></td>
<td>Buttons Status detection</td>
</tr>
<tr>
<td></td>
<td>USB Data handling</td>
</tr>
<tr>
<td>8-HIDPRO.ASM</td>
<td>USB handler</td>
</tr>
<tr>
<td>8USB-ISR.ASM</td>
<td>USB interrupt</td>
</tr>
<tr>
<td>MARCO.ASM</td>
<td>USB interrupt</td>
</tr>
<tr>
<td></td>
<td>USB control transfer handler</td>
</tr>
<tr>
<td>USB-MSE3.H</td>
<td>Device, configure, interface, HID, endpoint, string and report descriptors</td>
</tr>
<tr>
<td>JB8-EQS.H</td>
<td>JB8 registers and memory definitions</td>
</tr>
</tbody>
</table>

1.7 Test Description

- The solution was tested under different Windows operating systems on several brands of PCs.
- USBCheck version 3.2 and HIDView version 3.6.
- Compatibility tests under Windows 98SE.
- Compatibility tests under AMD 750, Intel 810 chip set Desktops, and IBM Thinkpad 570, 600E.

1.8 Customization

1.8.1 Hardware

- Adjust the values of the serial resistors of the infrared LEDs according to the LED characteristics.
1.8.2 Firmware

- Change USB interrupt and handler routines to meet the new USB testing requirements in Command Verifier.
- Change vendor ID, product ID and product revision number in the device descriptor table in "USE-MSE3.H"
- Change vendor name and product name in the string descriptor table in "USB-MSE3.H"
- Change the report descriptor in "USB-MSE3.h" if necessary.

1.9 Extra Features

1.10 Further Information

1.10.1 Related Documents

MC68HC908JB1 Technical Data

Universal Serial Bus Specification, version 1.1

Device Class Definition for Human Interface Device (HID), version 1.1

USB HID Usage Tables, version 1.1
Section 2. Glossary

A — See “accumulator (A).”

accumulator (A) — An 8-bit general-purpose register in the CPU08. The CPU08 uses the accumulator to hold operands and results of arithmetic and logic operations.

acquisition mode — A mode of PLL operation during startup before the PLL locks on a frequency. Also see “tracking mode.”

address bus — The set of wires that the CPU or DMA uses to read and write memory locations.

addressing mode — The way that the CPU determines the operand address for an instruction. The M68HC08 CPU has 16 addressing modes.

ALU — See “arithmetic logic unit (ALU).”

arithmetic logic unit (ALU) — The portion of the CPU that contains the logic circuitry to perform arithmetic, logic, and manipulation operations on operands.

asynchronous — Refers to logic circuits and operations that are not synchronized by a common reference signal.

baud rate — The total number of bits transmitted per unit of time.

BCD — See “binary-coded decimal (BCD).”

binary — Relating to the base 2 number system.

binary number system — The base 2 number system, having two digits, 0 and 1. Binary arithmetic is convenient in digital circuit design because digital circuits have two permissible voltage levels, low and high. The binary digits 0 and 1 can be interpreted to correspond to the two digital voltage levels.

binary-coded decimal (BCD) — A notation that uses 4-bit binary numbers to represent the 10 decimal digits and that retains the same positional structure of a decimal number. For example, 234 (decimal) = 0010 0011 0100 (BCD)

bit — A binary digit. A bit has a value of either logic 0 or logic 1.

branch instruction — An instruction that causes the CPU to continue processing at a memory location other than the next sequential address.

break module — A module in the M68HC08 Family. The break module allows software to halt program execution at a programmable point in order to enter a background routine.

breakpoint — A number written into the break address registers of the break module. When a number appears on the internal address bus that is the same as the number in the break address registers, the CPU executes the software interrupt instruction (SWI).
break interrupt — A software interrupt caused by the appearance on the internal address bus of the same value that is written in the break address registers.

bus — A set of wires that transfers logic signals.

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bus clock — The bus clock is derived from the CGMOUT output from the CGM. The bus clock frequency, \( f_{op} \), is equal to the frequency of the oscillator output, CGMXCLK, divided by four.

byte — A set of eight bits.

C — The carry/borrow bit in the condition code register. The CPU08 sets the carry/borrow bit when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some logical operations and data manipulation instructions also clear or set the carry/borrow bit (as in bit test and branch instructions and shifts and rotates).

CCR — See “condition code register.”

central processor unit (CPU) — The primary functioning unit of any computer system. The CPU controls the execution of instructions.

CGM — See “clock generator module (CGM).”

clear — To change a bit from logic 1 to logic 0; the opposite of set.

clock — A square wave signal used to synchronize events in a computer.

clock generator module (CGM) — A module in the M68HC08 Family. The CGM generates a base clock signal from which the system clocks are derived. The CGM may include a crystal oscillator circuit and or phase-locked loop (PLL) circuit.

comparator — A device that compares the magnitude of two inputs. A digital comparator defines the equality or relative differences between two binary numbers.

counter clock — The input clock to the TIM counter. This clock is the output of the TIM prescaler.

cpu — See “central processor unit (CPU).”

CPU08 — The central processor unit of the M68HC08 Family.

CPU clock — The CPU clock is derived from the CGMOUT output from the CGM. The CPU clock frequency is equal to the frequency of the oscillator output, CGMXCLK, divided by four.
CPU cycles — A CPU cycle is one period of the internal bus clock, normally derived by dividing a crystal oscillator source by two or more so the high and low times will be equal. The length of time required to execute an instruction is measured in CPU clock cycles.

CPU registers — Memory locations that are wired directly into the CPU logic instead of being part of the addressable memory map. The CPU always has direct access to the information in these registers. The CPU registers in an M68HC08 are:

- A (8-bit accumulator)
- H:X (16-bit index register)
- SP (16-bit stack pointer)
- PC (16-bit program counter)
- CCR (condition code register containing the V, H, I, N, Z, and C bits)

CSIC — customer-specified integrated circuit

cycle time — The period of the operating frequency: \( t_{\text{CYC}} = 1/f_{\text{OP}} \).

decimal number system — Base 10 numbering system that uses the digits zero through nine.

direct memory access module (DMA) — A M68HC08 Family module that can perform data transfers between any two CPU-addressable locations without CPU intervention. For transmitting or receiving blocks of data to or from peripherals, DMA transfers are faster and more code-efficient than CPU interrupts.

DMA — See “direct memory access module (DMA).”

DMA service request — A signal from a peripheral to the DMA module that enables the DMA module to transfer data.

duty cycle — A ratio of the amount of time the signal is on versus the time it is off. Duty cycle is usually represented by a percentage.

EEPROM — Electrically erasable, programmable, read-only memory. A nonvolatile type of memory that can be electrically reprogrammed.

EPROM — Erasable, programmable, read-only memory. A nonvolatile type of memory that can be erased by exposure to an ultraviolet light source and then reprogrammed.

exception — An event such as an interrupt or a reset that stops the sequential execution of the instructions in the main program.

external interrupt module (IRQ) — A module in the M68HC08 Family with both dedicated external interrupt pins and port pins that can be enabled as interrupt pins.

fetch — To copy data from a memory location into the accumulator.

firmware — Instructions and data programmed into nonvolatile memory.

free-running counter — A device that counts from zero to a predetermined number, then rolls over to zero and begins counting again.

full-duplex transmission — Communication on a channel in which data can be sent and received simultaneously.
Glossary

H — The upper byte of the 16-bit index register (H:X) in the CPU08.

H — The half-carry bit in the condition code register of the CPU08. This bit indicates a carry from the low-order four bits of the accumulator value to the high-order four bits. The half-carry bit is required for binary-coded decimal arithmetic operations. The decimal adjust accumulator (DAA) instruction uses the state of the H and C bits to determine the appropriate correction factor.

hexadecimal — Base 16 numbering system that uses the digits 0 through 9 and the letters A through F.

high byte — The most significant eight bits of a word.

illegal address — An address not within the memory map.

illegal opcode — A nonexistent opcode.

I — The interrupt mask bit in the condition code register of the CPU08. When I is set, all interrupts are disabled.

index register (H:X) — A 16-bit register in the CPU08. The upper byte of H:X is called H. The lower byte is called X. In the indexed addressing modes, the CPU uses the contents of H:X to determine the effective address of the operand. H:X can also serve as a temporary data storage location.

input/output (I/O) — Input/output interfaces between a computer system and the external world. A CPU reads an input to sense the level of an external signal and writes to an output to change the level on an external signal.

instructions — Operations that a CPU can perform. Instructions are expressed by programmers as assembly language mnemonics. A CPU interprets an opcode and its associated operand(s) and instruction.

interrupt — A temporary break in the sequential execution of a program to respond to signals from peripheral devices by executing a subroutine.

interrupt request — A signal from a peripheral to the CPU intended to cause the CPU to execute a subroutine.

I/O — See “input/output (I/O).”

IRQ — See “external interrupt module (IRQ).”

jitter — Short-term signal instability.

latch — A circuit that retains the voltage level (logic 1 or logic 0) written to it for as long as power is applied to the circuit.

latency — The time lag between instruction completion and data movement.

least significant bit (LSB) — The rightmost digit of a binary number.

logic 1 — A voltage level approximately equal to the input power voltage (V_{DD}).

logic 0 — A voltage level approximately equal to the ground voltage (V_{SS}).

low byte — The least significant eight bits of a word.

low voltage inhibit module (LVI) — A module that monitors power supply voltage.

LVI — See “low voltage inhibit module (LVI).”
M68HC08 — A Motorola family of 8-bit MCUs.

mark/space — The logic 1/logic 0 convention used in formatting data in serial communication.

mask — 1. A logic circuit that forces a bit or group of bits to a desired state. 2. A photomask used in integrated circuit fabrication to transfer an image onto silicon.

mask option — A optional microcontroller feature that the customer chooses to enable or disable.

mask option register (MOR) — An EPROM location containing bits that enable or disable certain MCU features.

MCU — Microcontroller unit. See “microcontroller.”

memory location — Each M68HC08 memory location holds one byte of data and has a unique address. To store information in a memory location, the CPU places the address of the location on the address bus, the data information on the data bus, and asserts the write signal. To read information from a memory location, the CPU places the address of the location on the address bus and asserts the read signal. In response to the read signal, the selected memory location places its data onto the data bus.

memory map — A pictorial representation of all memory locations in a computer system.

microcontroller — Microcontroller unit (MCU). A complete computer system, including a CPU, memory, a clock oscillator, and input/output (I/O) on a single integrated circuit.

modulo counter — A counter that can be programmed to count to any number from zero to its maximum possible modulus.

monitor ROM — A section of ROM that can execute commands from a host computer for testing purposes.

MOR — See “mask option register (MOR).”

most significant bit (MSB) — The leftmost digit of a binary number.

multiplexer — A device that can select one of a number of inputs and pass the logic level of that input on to the output.

N — The negative bit in the condition code register of the CPU08. The CPU sets the negative bit when an arithmetic operation, logical operation, or data manipulation produces a negative result.

nibble — A set of four bits (half of a byte).

object code — The output from an assembler or compiler that is itself executable machine code, or is suitable for processing to produce executable machine code.

opcode — A binary code that instructs the CPU to perform an operation.

open-drain — An output that has no pullup transistor. An external pullup device can be connected to the power supply to provide the logic 1 output voltage.

operand — Data on which an operation is performed. Usually a statement consists of an operator and an operand. For example, the operator may be an add instruction, and the operand may be the quantity to be added.

oscillator — A circuit that produces a constant frequency square wave that is used by the computer as a timing and sequencing reference.
Glossary

OTPROM — One-time programmable read-only memory. A nonvolatile type of memory that cannot be reprogrammed.

overflow — A quantity that is too large to be contained in one byte or one word.

page zero — The first 256 bytes of memory (addresses $0000–$00FF).

parity — An error-checking scheme that counts the number of logic 1s in each byte transmitted. In a system that uses odd parity, every byte is expected to have an odd number of logic 1s. In an even parity system, every byte should have an even number of logic 1s. In the transmitter, a parity generator appends an extra bit to each byte to make the number of logic 1s odd for odd parity or even for even parity. A parity checker in the receiver counts the number of logic 1s in each byte. The parity checker generates an error signal if it finds a byte with an incorrect number of logic 1s.

PC — See “program counter (PC).”

peripheral — A circuit not under direct CPU control.

phase-locked loop (PLL) — A oscillator circuit in which the frequency of the oscillator is synchronized to a reference signal.

PLL — See “phase-locked loop (PLL).”

pointer — Pointer register. An index register is sometimes called a pointer register because its contents are used in the calculation of the address of an operand, and therefore points to the operand.

polarity — The two opposite logic levels, logic 1 and logic 0, which correspond to two different voltage levels, $V_{DD}$ and $V_{SS}$.

polling — Periodically reading a status bit to monitor the condition of a peripheral device.

port — A set of wires for communicating with off-chip devices.

prescaler — A circuit that generates an output signal related to the input signal by a fractional scale factor such as 1/2, 1/8, 1/10 etc.

program — A set of computer instructions that cause a computer to perform a desired operation or operations.

program counter (PC) — A 16-bit register in the CPU08. The PC register holds the address of the next instruction or operand that the CPU will use.

pull — An instruction that copies into the accumulator the contents of a stack RAM location. The stack RAM address is in the stack pointer.

pullup — A transistor in the output of a logic gate that connects the output to the logic 1 voltage of the power supply.

pulse-width — The amount of time a signal is on as opposed to being in its off state.

pulse-width modulation (PWM) — Controlled variation (modulation) of the pulse width of a signal with a constant frequency.

push — An instruction that copies the contents of the accumulator to the stack RAM. The stack RAM address is in the stack pointer.

PWM period — The time required for one complete cycle of a PWM waveform.
RAM — Random access memory. All RAM locations can be read or written by the CPU. The contents of a RAM memory location remain valid until the CPU writes a different value or until power is turned off.

RC circuit — A circuit consisting of capacitors and resistors having a defined time constant.

read — To copy the contents of a memory location to the accumulator.

register — A circuit that stores a group of bits.

reserved memory location — A memory location that is used only in special factory test modes. Writing to a reserved location has no effect. Reading a reserved location returns an unpredictable value.

reset — To force a device to a known condition.

ROM — Read-only memory. A type of memory that can be read but cannot be changed (written). The contents of ROM must be specified before manufacturing the MCU.

SCI — See “serial communication interface module (SCI).”

serial — Pertaining to sequential transmission over a single line.

serial communications interface module (SCI) — A module in the M68HC08 Family that supports asynchronous communication.

serial peripheral interface module (SPI) — A module in the M68HC08 Family that supports synchronous communication.

set — To change a bit from logic 0 to logic 1; opposite of clear.

shift register — A chain of circuits that can retain the logic levels (logic 1 or logic 0) written to them and that can shift the logic levels to the right or left through adjacent circuits in the chain.

signed — A binary number notation that accommodates both positive and negative numbers. The most significant bit is used to indicate whether the number is positive or negative, normally logic 0 for positive and logic 1 for negative. The other seven bits indicate the magnitude of the number.

software — Instructions and data that control the operation of a microcontroller.

software interrupt (SWI) — An instruction that causes an interrupt and its associated vector fetch.

SPI — See “serial peripheral interface module (SPI).”

stack — A portion of RAM reserved for storage of CPU register contents and subroutine return addresses.

stack pointer (SP) — A 16-bit register in the CPU08 containing the address of the next available storage location on the stack.

start bit — A bit that signals the beginning of an asynchronous serial transmission.

status bit — A register bit that indicates the condition of a device.

stop bit — A bit that signals the end of an asynchronous serial transmission.
subroutine — A sequence of instructions to be used more than once in the course of a program. The last instruction in a subroutine is a return from subroutine (RTS) instruction. At each place in the main program where the subroutine instructions are needed, a jump or branch to subroutine (JSR or BSR) instruction is used to call the subroutine. The CPU leaves the flow of the main program to execute the instructions in the subroutine. When the RTS instruction is executed, the CPU returns to the main program where it left off.

synchronous — Refers to logic circuits and operations that are synchronized by a common reference signal.

TIM — See “timer interface module (TIM).”

timer interface module (TIM) — A module used to relate events in a system to a point in time.

timer — A module used to relate events in a system to a point in time.

toggle — To change the state of an output from a logic 0 to a logic 1 or from a logic 1 to a logic 0.

tracking mode — Mode of low-jitter PLL operation during which the PLL is locked on a frequency. Also see “acquisition mode.”

two’s complement — A means of performing binary subtraction using addition techniques. The most significant bit of a two’s complement number indicates the sign of the number (1 indicates negative). The two’s complement negative of a number is obtained by inverting each bit in the number and then adding 1 to the result.

unbuffered — Utilizes only one register for data; new data overwrites current data.

unimplemented memory location — A memory location that is not used. Writing to an unimplemented location has no effect. Reading an unimplemented location returns an unpredictable value. Executing an opcode at an unimplemented location causes an illegal address reset.

V — The overflow bit in the condition code register of the CPU08. The CPU08 sets the V bit when a two’s complement overflow occurs. The signed branch instructions BGT, BGE, BLE, and BLT use the overflow bit.

variable — A value that changes during the course of program execution.

VCO — See “voltage-controlled oscillator.”

vector — A memory location that contains the address of the beginning of a subroutine written to service an interrupt or reset.

voltage-controlled oscillator (VCO) — A circuit that produces an oscillating output signal of a frequency that is controlled by a dc voltage applied to a control input.

waveform — A graphical representation in which the amplitude of a wave is plotted against time.

wired-OR — Connection of circuit outputs so that if any output is high, the connection point is high.

word — A set of two bytes (16 bits).

write — The transfer of a byte of data from the CPU to a memory location.

X — The lower byte of the index register (H:X) in the CPU08.

Z — The zero bit in the condition code register of the CPU08. The CPU08 sets the zero bit when an arithmetic operation, logical operation, or data manipulation produces a result of $00.
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