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a

User Manual Errata

MC68307 Integrated Multiple Bus Processor

Date: Tues, 25th July 1995.

p3-14: Section 3.1.7., 8051-Bus Operation. The 8051-compatible read and write cycles should be as follows:

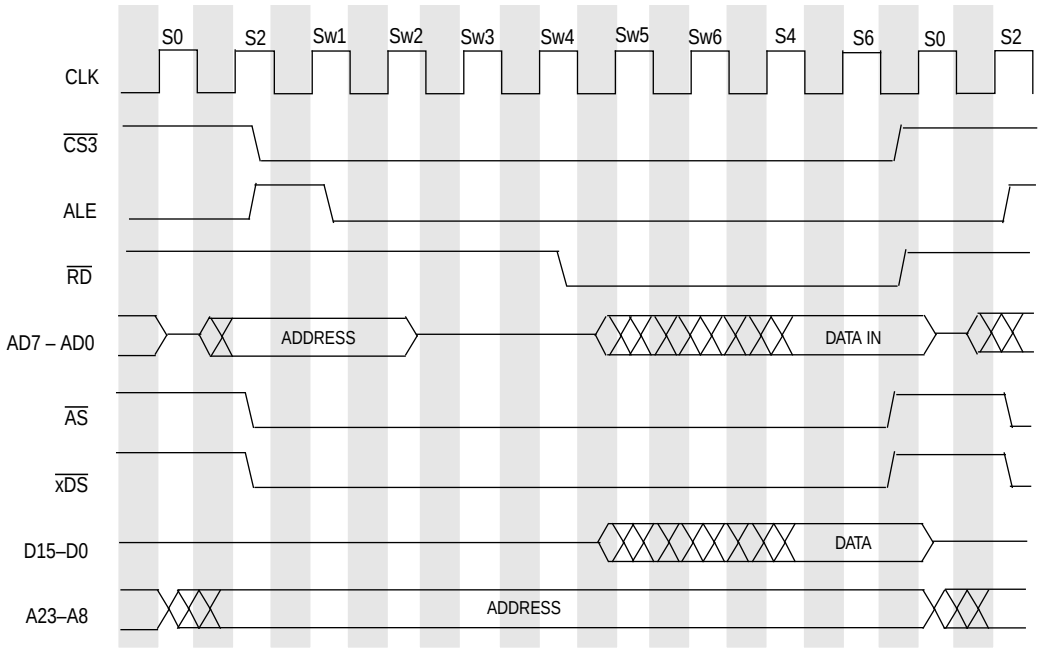


Figure 3-12. 8051-Compatible Read Cycle Signals

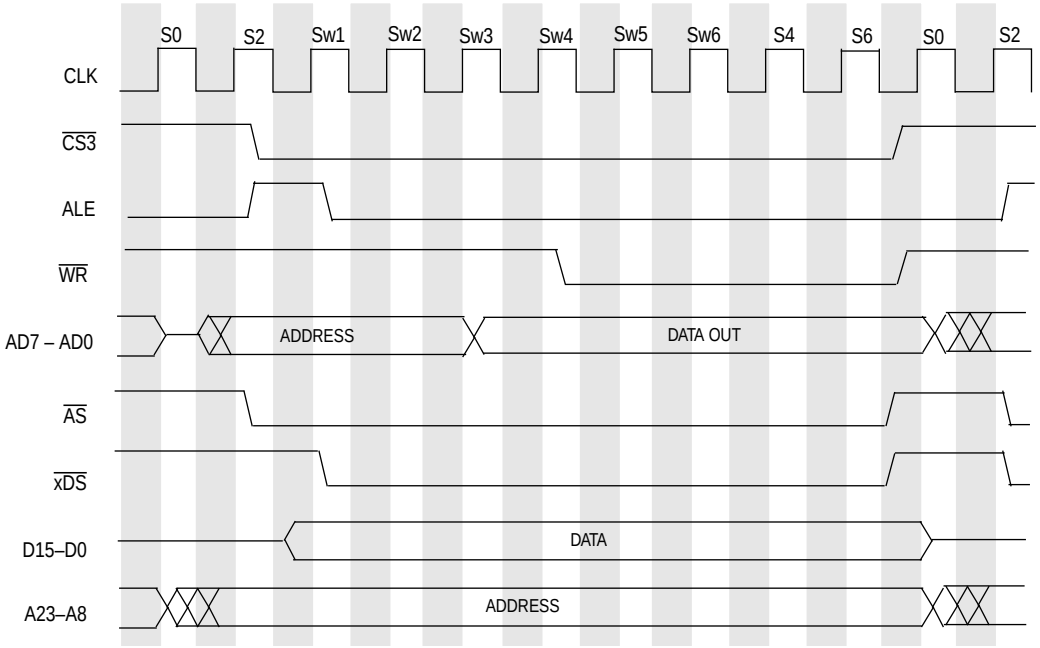


Figure 3-13. 8051-Compatible Write Cycle Signals

p5-40: Section 5.2.4.2. The Peripheral Interrupt Control Register (PICR) does not specify the peripheral interrupt pending bits.

PICR MBASE+$024

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_T1	T1IPL(2–0)			PI_T2	T2IPL(2–0)			PI_UA	UAIPL(2–0)			PI_MB	MBIPL(2–0)		
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Read/Write Supervisor or User

Interrupt Priority Level Timer 1, Timer 2, UART, MBUS, T1IPL2–0, T2IPL2–0, MBIPL2–0, UAIPL2–0

These bits allow the user to specify the IPL for the corresponding on-chip peripheral module interrupt input line (Timer 1, Timer 2, UART and M-bus respectively). When an interrupt occurs, the interrupt controller logic asserts the correct priority code on the EC000 interrupt level inputs, and responds to the subsequent acknowledge cycle by coordinating the return of the appropriate vector, as programmed into the programmable interrupt vector register or UART interrupt vector register.

000 = The corresponding interrupt source is inhibited and cannot generate interrupts.
001-111 = The corresponding interrupt source is enabled, and can generate an interrupt to the EC000 core processor with the indicated priority level.

Pending Interrupt – PI_T1, PI_T2, PI_UA, PI_MB

These read-only bits (Bits 15, 11, 7, 3) indicate when the peripherals have an interrupt pending. Writes to these bits are ignored.

Read Only Value
0 = No Interrupt pending.
1 = Interrupt is Pending.

p6-7: Section 6.3.2.2., Watchdog Counter Register (WCR). The WCR has a reset value of 0.

p9-2: Section 9.1, Overview. The boundary scan register has 116 bits.

p9-2: Section 9.1, Figure 9-1. The Test Access Port Block Diagram should show the TCK pin with an internal pullup resistor, and not an internal pulldown resistor.

p9-2: Section 9.1, Overview. The TCK pin has an internal pullup resistor not a pulldown.

TCK— test clock input to synchronize the test logic (with pullup).

p9-4: Section 9.3, Table 9-1. The Boundary Scan Control bit numbers are wrong. Use the corrected table and paragraphs overleaf:

"The MC68307 IEEE 1149.1 implementation has a 116-bit boundary scan register. This register contains bits for all device signal and clock pins and associated control signals. The XTAL, EXTAL and $\overline{\text{RSTIN}}$ pins are associated with analog signals and are not included in the boundary scan register.

All MC68307 bidirectional pins, except the open-drain I/O pins ($\overline{\text{HALT}}$, $\overline{\text{DTACK}}$, $\overline{\text{RESET}}$, SCL and SDA), have a register bit for the output path and another for the input path. In addition, SCL and SDA have a third bit which controls these pins. All open drain I/O pins have a single register bit for pin data and no associated control bit. To ensure proper operation, the open-drain pins require external pullups. Thirty-two control bits in the boundary scan register define the output enable signal (1=output) for associated groups of bidirectional and three-state pins. The control bits and their bit positions are listed in Table 9-1.

Table 3-1. Boundary Scan Control Bits

Name	Bit Number	Name	Bit Number	Name	Bit Number	Name	Bit Number
bus.ctl	3	pa3.ctl	56	pb11.ctl	72	pb3.ctl	88
rw.ctl	10	pa2.ctl	58	pb10.ctl	74	pb2.ctl	90
adb.ctl	21	pa1.ctl	60	pb9.ctl	76	pb1.pu	92
ab.ctl	45	pa0.ctl	62	pb8.ctl	78	pb1.ctl	93
pa7.ctl	48	pb15.ctl	64	pb7.ctl	80	pb0.pu	95
pa6.ctl	50	pb14.ctl	66	pb6.ctl	82	pb0.ctl	96
pa5.ctl	52	pb13.ctl	68	pb5.ctl	84	dhi.ctl	98
pa4.ctl	54	pb12.ctl	70	pb4.ctl	86	dlo.ctl	107

Boundary scan bit definitions are shown in Table 9-2. The first column in Table 9-2 defines the bit's ordinal position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 0; the last bit to be shifted out is bit 115."

p9-5: Section 9.3, Table 9-2. The Boundary Scan Bit Definitions is incorrect. The corrected table follows:

Table 10-2. Boundary Scan Bit Definitions

Bit Num	Cell Type	Signal	Control
0	O.Cell	ALE	—
1	O.Cell	$\overline{RD}$	—
2	O.Cell	$\overline{WR}$	—
3	En.Cell	bus.ctl	—
4	IO.Cell	$\overline{AS}$	bus.ctl
5	IO.Cell	$\overline{UDS}$	bus.ctl
6	IO.Cell	$\overline{LDS}$	bus.ctl
7	IO.Cell	$\overline{RW}$	rw.ctl
8	O.Cell	$\overline{DTACK}$	—
9	I.Cell	$\overline{DTACK}$	—
10	En.Cell	rw.ctl	—
11	O.Cell	$\overline{HALT}$	—
12	I.Cell	$\overline{HALT}$	—
13	O.Cell	$\overline{RESET}$	—
14	I.Cell	$\overline{RESET}$	—
15	O.Cell	$\overline{CS0}$	—
16	O.Cell	$\overline{CS1}$	—
17	O.Cell	$\overline{CS2}$	—
18	O.Cell	$\overline{CS3}$	—
19	O.Cell	CLKOUT	—
20	I.Cell	BUSW	—
21	En.Cell	adb.ctl	—
22	IO.Cell	AD0	adb.ctl
23	IO.Cell	AD1	adb.ctl
24	IO.Cell	AD2	adb.ctl
25	IO.Cell	AD3	adb.ctl
26	IO.Cell	AD4	adb.ctl
27	IO.Cell	AD5	adb.ctl
28	IO.Cell	AD6	adb.ctl
29	IO.Cell	AD7	adb.ctl
30	IO.Cell	A8	ab.ctl
31	IO.Cell	A9	ab.ctl
32	IO.Cell	A10	ab.ctl
33	IO.Cell	A11	ab.ctl
34	IO.Cell	A12	ab.ctl
35	IO.Cell	A13	ab.ctl
36	IO.Cell	A14	ab.ctl
37	IO.Cell	A15	ab.ctl
38	IO.Cell	A16	ab.ctl
39	IO.Cell	A17	ab.ctl
40	IO.Cell	A18	ab.ctl
41	IO.Cell	A19	ab.ctl
42	IO.Cell	A20	ab.ctl
43	IO.Cell	A21	ab.ctl
44	IO.Cell	A22	ab.ctl
45	En.Cell	ab.ctl	—
46	IO.Cell	A23	ab.ctl
47	I.Cell	$\overline{IRQ7}$	—
48	En.Cell	pa7.ctl	—
49	IO.Cell	$\overline{BGACK}$	pa7.ctl
50	En.Cell	pa6.ctl	—
51	IO.Cell	$\overline{BG}$	pa6.ctl
52	En.Cell	pa5.ctl	—
53	IO.Cell	$\overline{BR}$	pa5.ctl
54	En.Cell	pa4.ctl	—
55	IO.Cell	TOUT2	pa4.ctl
56	En.Cell	pa3.ctl	—
57	IO.Cell	TOUT1	pa3.ctl
58	En.Cell	pa2.ctl	—
59	IO.Cell	$\overline{CS2D}$	pa2.ctl
60	En.Cell	pa1.ctl	—
61	IO.Cell	$\overline{CS2C}$	pa1.ctl
62	En.Cell	pa0.ctl	—
63	IO.Cell	$\overline{CS2B}$	pa0.ctl
64	En.Cell	pb15.ctl	—
65	IO.Cell	$\overline{INT8}$	pb15.ctl
66	En.Cell	pb14.ctl	—
67	IO.Cell	$\overline{INT7}$	pb14.ctl
68	En.Cell	pb13.ctl	—
69	IO.Cell	$\overline{INT6}$	pb13.ctl
70	En.Cell	pb12.ctl	—
71	IO.Cell	$\overline{INT5}$	pb12.ctl
72	En.Cell	pb11.ctl	—
73	IO.Cell	$\overline{INT4}$	pb11.ctl
74	En.Cell	pb10.ctl	—
75	IO.Cell	$\overline{INT3}$	pb10.ctl
76	En.Cell	pb9.ctl	—
77	IO.Cell	$\overline{INT2}$	pb9.ctl
78	En.Cell	pb8.ctl	—
79	IO.Cell	$\overline{INT1}$	pb8.ctl
80	En.Cell	pb7.ctl	—
81	IO.Cell	TIN2	pb7.ctl
82	En.Cell	pb6.ctl	—
83	IO.Cell	TIN1	pb6.ctl
84	En.Cell	pb5.ctl	—
85	IO.Cell	$\overline{CTS}$	pb5.ctl
86	En.Cell	pb4.ctl	—
87	IO.Cell	$\overline{RTS}$	pb4.ctl
88	En.Cell	pb3.ctl	—
89	IO.Cell	RXD	pb3.ctl

Table 10-2. Boundary Scan Bit Definitions (Continued)

90	En.Cell	pb2.ctl	—	103	IO.Cell	D11	dhi.ctl
91	IO.Cell	TXD	pb2.ctl	104	IO.Cell	D10	dhi.ctl
92	En.Cell	pb1.pu	—	105	IO.Cell	D9	dhi.ctl
93	En.Cell	pb1.ctl	—	106	IO.Cell	D8	dhi.ctl
94	IO.Cell	SDA	pb1.ctl/ pb1.pu	107	En.Cell	dlo.ctl	—
95	En.Cell	pb0.pu	—	108	IO.Cell	D7	dlo.ctl
96	En.Cell	pb0.ctl	—	109	IO.Cell	D6	dlo.ctl
97	IO.Cell	SCL	pb0.ctl/ pb0.pu	110	IO.Cell	D5	dlo.ctl
98	En.Cell	dhi.ctl	—	111	IO.Cell	D4	dlo.ctl
99	IO.Cell	D15	dhi.ctl	112	IO.Cell	D3	dlo.ctl
100	IO.Cell	D14	dhi.ctl	113	IO.Cell	D2	dlo.ctl
101	IO.Cell	D13	dhi.ctl	114	IO.Cell	D1	dlo.ctl
102	IO.Cell	D12	dhi.ctl	115	IO.Cell	D0	dlo.ctl

p9-10: Sections 9.4.1 (EXTEST), 9.4.2 (SAMPLE/PRELOAD), and 9.4.3 (BYPASS) should state "the 116-bit boundary scan register" and not 117 bit.

p10-19: Section 10.3.7.1, Software Listing 1 - Mbus Master Software. The WRITE1 subroutine is missing a line which writes to the MBDR. It should be as follows:

```
WRITE1      BTST     #5,MBSR             TEST MBB BIT,
            BNE      WRITE1              AND WAIT UNTIL IT IS CLEAR
TXSTART
            BSET     #4,MBCR             SET TRANSMIT MODE
            BSET     #5,MBCR             SET MASTER MODE (GENERATE START)
            BSET     #6,MBCR             Enable MBUS Interrupts
            MOVE.B   (V_CHIPAD),MBDR     TRANSMIT THE SLAVE CHIP ADDRESS
            MOVE.W   #$2000,SR           ENABLE INTERRUPTS BY SETTING TO LEVEL 0

MBFREE      BTST     #5,MBSR             TEST MBB BIT,
            BEQ      MBFREE              If bus is still free, wait until busy
            RTS
```

p11-1: Section 11.1, Maximum Ratings. The table should include both standard operating temperature and extended operating temperature details:

Rating	Symbol	Value	Unit
Supply Voltage[1, 2]	V_{CC}	–0.3 to + 7.0	V
Input Voltage[1, 2]	V_{in}	–0.3 to + 7.0	V
Sandard Operating Temperatures	T_A	0 to 70	°C
Extended Operating Temperatures	"	–40 to 85	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

NOTES:
1. Permanent damage can occur if maximum ratings are exceeded. Exposure to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
2. Although sections of the device contain circuitry to protect against damage from high static voltages or electrical fields, normal precautions should be taken to avoid exposure to voltages higher than maximum-rated voltages.

This device contains protective circuitry against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

p12-1: Section 12.1, Standard Ordering Information. The temperature ranges are incorrect. The corrected values are as follows:

Package Type	Frequency (MHz)	Supply Voltage (V)	Temperature	Order Number
100-Pin Plastic Quad Flat Pack (FG Suffix)	16.67	5	0°C to 70°C	MC68307FG16
100-Pin Thin Quad Flat Pack (PU Suffix)	16.67	5	0°C to 70°C	MC68307PU16
100-Pin Plastic Quad Flat Pack (FG Suffix)	16.67	5	-40°C to 85°C	MC68307CFG16
100-Pin Plastic Quad Flat Pack (FG Suffix)	16.67	3.3	0°C to 70°C	MC68307FG16V
100-Pin Thin Quad Flat Pack (PU Suffix)	8.33	3.3	0°C to 70°C	MC68307PU8V
100-Pin Thin Quad Flat Pack (PU Suffix)	16.67	3.3	0°C to 70°C	MC68307PU16V

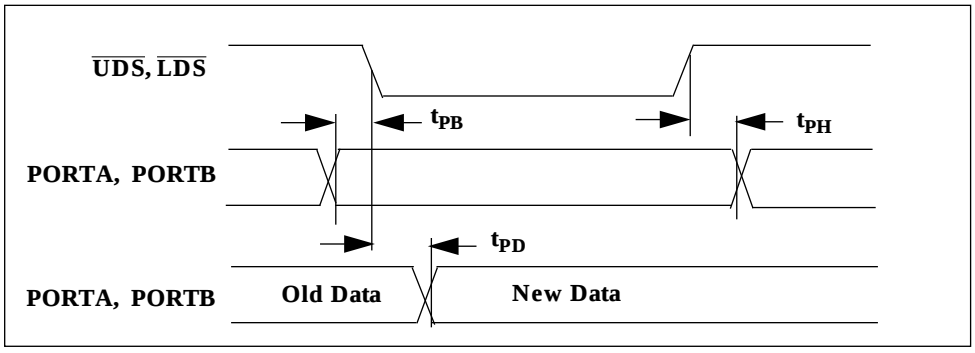
p11-16: Section 11.14, AC Electrical Characteristics - Port Timing. The 8MHz and 16.67MHz timing values should be changed and the tPD time referenced to UDS/LDS assertion as follows:

11.14 AC ELECTRICAL CHARACTERISTICS—PORT TIMING

(See Figure 11-13.)

Characteristic	Symbol	3.3V		3.3 V or 5 V		Unit
		8.33 MHz		16.67 MHz		
		Min	Max	Min	Max	
Port Input Setup Time to $\overline{UDS}$, $\overline{LDS}$ Asserted	t_{PS}	0	—	0	—	ns
Port Input Hold Time from $\overline{UDS}$, $\overline{LDS}$ Negated	t_{PH}	0	—	0	—	ns
Port Output Valid from $\overline{UDS}$, $\overline{LDS}$ Asserted	t_{PD}	—	20	—	10	ns

NOTE: Test conditions for port outputs: C_L = 50 pF, R_L = 27 kΩ to V_{CC}.



11-13. Port Timing

p11-17: Section 11.15, IEEE 1149.1 Electrical Characteristics. The 8MHz and 16.67MHz timing columns should be swapped as follow:

11.15 IEEE 1149.1 ELECTRICAL CHARACTERISTICS

(See Figure 11-14, Figure 11-15, and Figure 11-16.)

Num.	Characteristic	3.3V		3.3 V or 5 V		Unit
		8.33 MHz		16.67 MHz		
		Min	Max	Min	Max	
	TCK Frequency of Operation	0	5.0	0	10.0	MHz
1	TCK Cycle Time	200	—	100	—	ns
2	TCK Clock Pulse Width Measured at 1.5 V	45	—	45	—	ns
3	TCK Rise and Fall Times	0	10	0	5	ns
6	Boundary Scan Input Data Setup Time	30	—	15	—	ns
7	Boundary Scan Input Data Hold Time	30	—	15	—	ns
8	TCK Low to Output Data Valid	0	160	0	80	ns
9	TCK Low to Output High Impedance	0	160	0	80	ns
10	TMS, TDI Data Setup Time	30	—	15	—	ns
11	TMS, TDI Data Hold Time	30	—	15	—	ns
12	TCK Low to TDO Data Valid	0	60	0	30	ns
13	TCK Low to TDO High Impedance	0	60	0	30	ns

Change History:

Rev 1.0	Tue, 21st Feb 1995	Original Release
Rev 1.1	Thur, 31st Mar 1995	Update
Rev 1.2	Tues, 25th Mar 1995	Update