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Freescale Semiconductor, Inc.

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**MOTOROLA**Microprocessor and Memory
Technologies Group**MC68341**

UPDATE TO MC68341 Integrated Processor User's Manual and Addendum

November 3, 1995

1. Negation of $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ for Retry Sequence and Late Retry Sequence.

Figure 3-25 and Figure 3-26 on pages 3-46 and 3-47 respectively, should show $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ being negated one-half clock cycle earlier. The corrected drawings are shown in Figure 1 and Figure 2 of this document.

2. Addition to Port C Pin Assignment Register Description

Add the following to **4.3.5.8 Port C Pin Assignment Register (PPARC)** on page 4-38: Any set bit configures the corresponding pin as $\overline{\text{RDY2}}$, $\overline{\text{RDY1}}$, $\overline{\text{DDACK2}}$, $\overline{\text{DDACK1}}$, $\overline{\text{DTC}}$, and $\overline{\text{RTCOUT}}$; any cleared bit configures the corresponding pin as $\overline{\text{TIN}}$, $\overline{\text{TGATE}}$, $\overline{\text{DACK2}}$, $\overline{\text{DACK1}}$, $\overline{\text{FC3}}$, and $\overline{\text{RMC}}$.

3. Typo in Channel Status Register (CSR) description.

The last sentence for the $\overline{\text{IRQ}}$ bit description on page 6-28 should be changed to "The $\overline{\text{STR}}$ bit in the $\overline{\text{CCR}}$ cannot be set when this bit is set; all error status bits must be cleared before the $\overline{\text{STR}}$ bit can be set."

4. Typo in CPOL—Clock Polarity Bit Description

The last sentence in the CPOL—Clock Priority bit description on page 9-19 incorrectly references Figures 9-24–9-27. The correct references should be to Figures 12-22–12-25.

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SEMICONDUCTOR PRODUCT INFORMATION

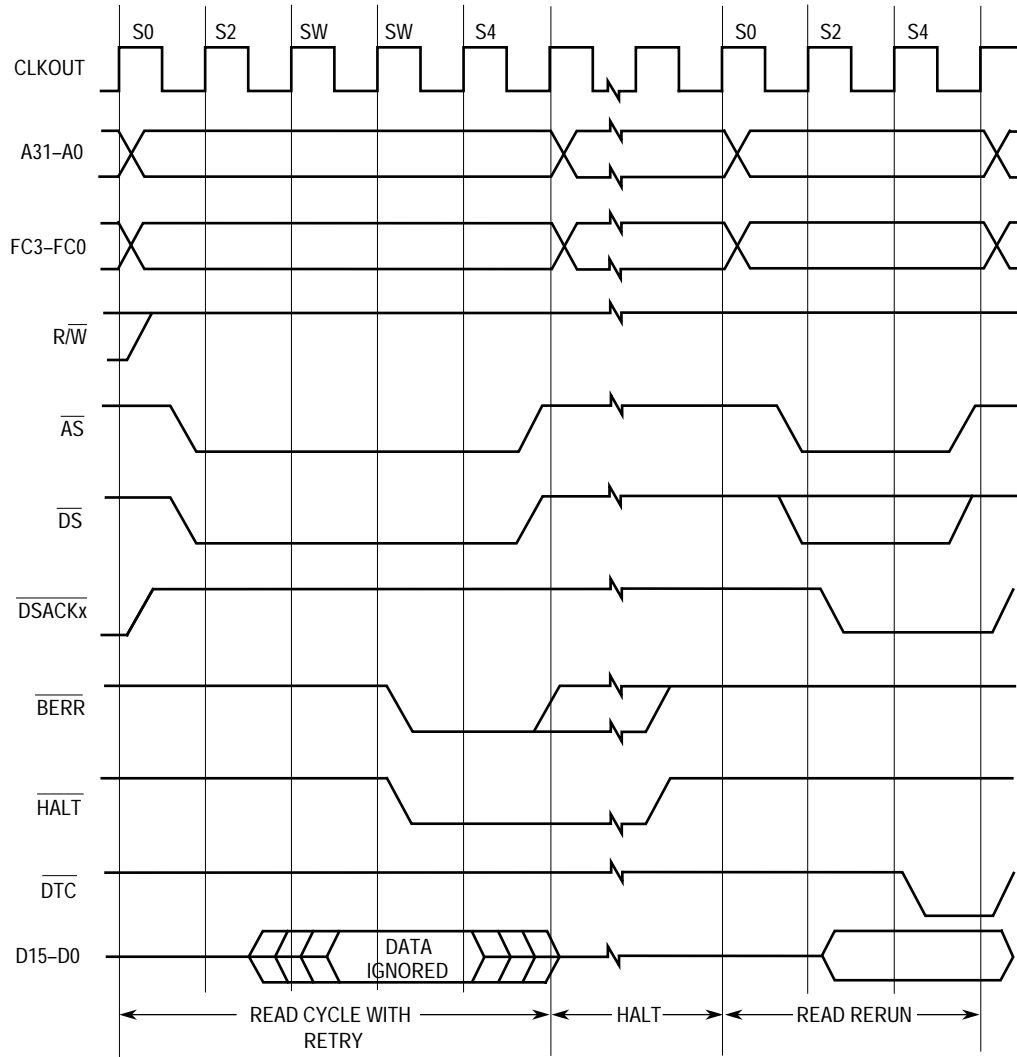


Figure 1. Retry Sequence

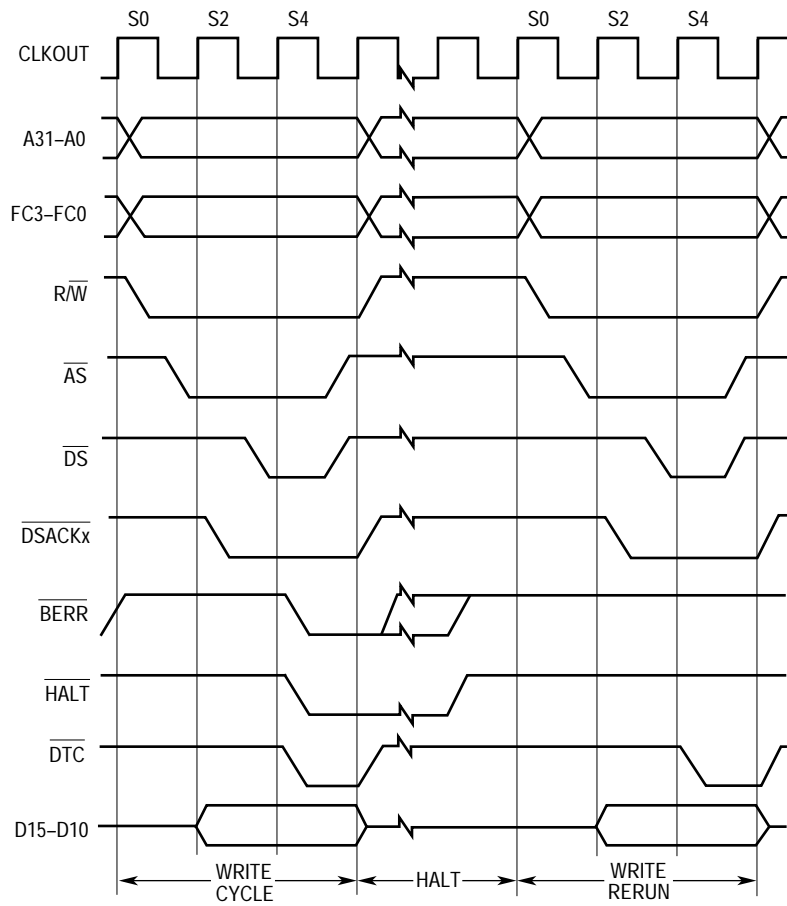



Figure 2. Late Retry Sequence



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