

Errata and Added Information to
**MC68LC302 Low Power Integrated Multiprotocol
Processor Reference Manual Rev 1**

February 21, 1997

Section 2– Configuration, Clocking, Low Power Modes, and Internal Memory Map

1. SCCE2 Register

In section 2-24, in Table 2-6, the SCCE2 register should be 8 bits wide, not 16 bits as shown.

Section 3 - System Integration Block

1. Periodic Interrupt Timer equation

In section 3.7.4.2, in the periodic interrupt timer period equation, the "+1" should be carried through the equations.

Section 5 - Signal Description

1. Bus Request Signal description

In section 5.8, the Bus Request signal is shown incorrectly in figure 5-7 and the description below the figure is incorrect. The pin is shown as bidirectional, but should be an output only. The description should read, "This signal is an open-drain output request signal from the IDMA and SDMA when the internal EC000 core is disabled."

2. Port A / Bootstrap Mode description

In section 5.14 in the "NOTE" section, "To enable Boot from SCC2" should be replaced with "To enable Boot from SCC1." The Bootstrap mode is only available on SCC1.



Section 6- Electrical Characteristics

1. Thermal Characteristic Values (θ_{ja} , θ_{jc})

In section 6.2 in the thermal characteristic table, the value for θ_{ja} should read 52.8, replacing TBD; also, the value for θ_{jc} should read 10.4, replacing TBD.

2. Junction Temperature (Tj) Equation

In section 6.2, the junction temperature equation should read:

$$T_j = 70C + (5.25V * 50mA * 52.8C/W) = 83.9C.$$

3. AC Electrical Specification Changes at 3.3V

In section 6.8 in the AC Electrical Specification Table, all information is for 5.0V only. The only value which changes at 3.3V is Spec 47, the Asynchronous Input Setup Time (t_{ASI}). This value should be 12ns, instead of 10ns, at both 16.67 and 20MHz. 25MHz is not supported at 3.3V.



Freescale Semiconductor, Inc.

Home Page:

www.freescale.com

email:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
(800) 521-6274
480-768-2130

support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)

support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 2666 8080

support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080

support.asia@freescale.com

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