M68SZ328ADS

Application Development System

User's Manual

Revision 1.2
January 29, 2002

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Motorola, Inc.

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Section 1
General Information

1.1 Introduction

1.2 Features

1.3 Related Documentation

1.4 Technical Support

1.4.1 M68SZ328ADS
1.4.2 Debugger

SECTION 1
Quick Installation Guide

1.1 OVERVIEW

The DragonBall™-SZ (MC68SZ328) Application Development System (M68SZ328ADS) is designed to supply users with an environment to develop MC68SZ328 based application software. Moreover, this board can be used as a reference for real-life product design. M68SZ328ADS provides several interface ports for application software and target board debug purpose. This document will discuss the usage and system details of the M68SZ328ADS.

Note:
This manual is used for the M68SZ328ADS Peripheral Board Ver1.1 only

1.2 FEATURES OF THE M68SZ328ADS

The features of the M68SZ328ADS include the following:

i) MC68SZ328 CPU

ii) Memory Subsystem
- -16 MB FLASH
- -32 MB SDRAM

iii) Debug Ports
- -Two RS232 serial ports interface to MC68SZ328 internal UARTs
- -One RS232 serial port for external UART
- -Direct logic analyzer interface to system bus

iv) LCD and Touch Panel Interface
- -MC68SZ328 LCD interface

vi) LED Indicators
- -Green LED for power
- -Red LED for system heart beat
- -Yellow LED for status of MC68SZ328 pin PN0
- -Yellow LED for status of MC68SZ328 pin PF1

vii) Switches
- -Two 8 ways Dip Switches for function control
- -Reset and Abort Switches

viii) Board Operation Mode Support
- -MC68SZ328 normal mode
- -MC68SZ328 bootstrap mode

xi) External Interface/Socket
- -USB receptable
- -SD card socket
- -Memory Stick card socket
- -Application Buttons
- -Single Tone Generator

x) VME Connectors
- -VME 3x32-pin female connector
- -VME 3x16-pin female connector

xi) Debug Monitor
- -MetroWerks Codewarrior Target Monitor using serial port
- -SDS source-level debugger monitor by Software Development Sys tem Inc. using Inc. using serial port

xii) Clock Source
- -32.768KHz for MC68SZ328 internal PLL

xiii) Power Adaptor
- -3.0V - 3.3V main power supply

1.3 RELATED DOCUMEMNTATION

The following documents can be used as references when using M68SZ328ADS.
- -MC68SZ328 User's Manual
- -MC68SZ328 Product Information

1.4 TECHNICAL SUPPORT

1.4.1 M68SZ328ADS

For getting the latest information, please visit our web page:

`http://www.motorola.com/dragonball`

1.4.2 Debugger

There are two source-level debuggers for DragonBall™-SZ. The contact information is listed below:

1. Metrowerks - `http://www.metrowerks.com`
2. Single Step Development - `http://www.sdsi.com`

Section 2
Quick Installation Guide

2.1 Overview

2.2 Equipments Required

2.3 Installation Procedure

2.3.1 Preparing MC68SZ328ADS board
2.3.2 Connecting MC68SZ328ADS to PC
2.3.3 Installing software debugger

SECTION 2
Quick Installation Guide

2.1 OVERVIEW

This section provides a description of the evaluation module, requirements, quick installation and test information. Detailed information on the M68SZ328ADS design and operation is provided in the remaining sections of this manual.

2.2 EQUIPMENTS REQUIRED

The following equipments are required to use with the M68SZ328ADS Application Development System, some of them are already bundled with the ADS package

Power adaptor – 3.0V-3.3V, 1500mA, with 2 mm female (inside positive) power connector.

RS-232 cable (DB9 male to DB9 female)

IBM PC compatible computer running Windows 95 or Window 98,with an RS-232 serial port capable of 9600-115200 bit per second operation.

2.3 INSTALLATION PROCEDURE

Please follow the procedure below to set up M68SZ328ADS:

1. Prepare M68SZ328ADS board.
2. Connect M68SZ328ADS board to PC and power supply.
3. Install software debugger.

2.3.1 Preparing M68SZ328ADS

Locate the DIP switches on the M68SZ328ADS board and select appropriate monitor and debug port for your debugger.

Figure 2-2 shows the factory default DIP switches settings. This setting selects Metroworks monitor and UART1 of DragonBall™Super VZ as the debug port. Other possible settings are shown in Figure 2-3, Figure 2-4 and Figure 2-5.

For detail description of each switch. Pls. refer to Table 3-1 and Table 3-2.

For additional information on the M68SZ328ADS and its components. Please refer to Section 3 .

Monitor and Port selection

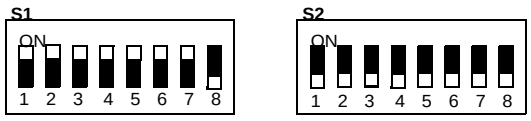
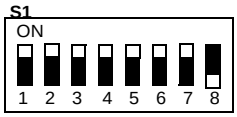


Figure 2.1 . Default Switch Setting
(MetroWerks Monitor using debug port)



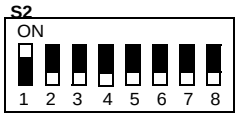


Figure 2.2. MetroWerks Monitor using UART 1

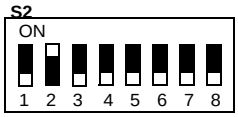
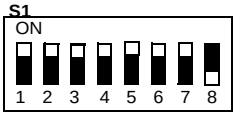


Figure 2.3. MetroWerks Monitor using UART 2



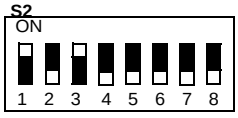


Figure 2.4. SDS Monitor using UART 1

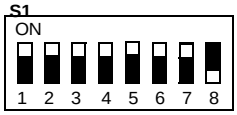


Figure 2.5. SDS Monitor using UART 2

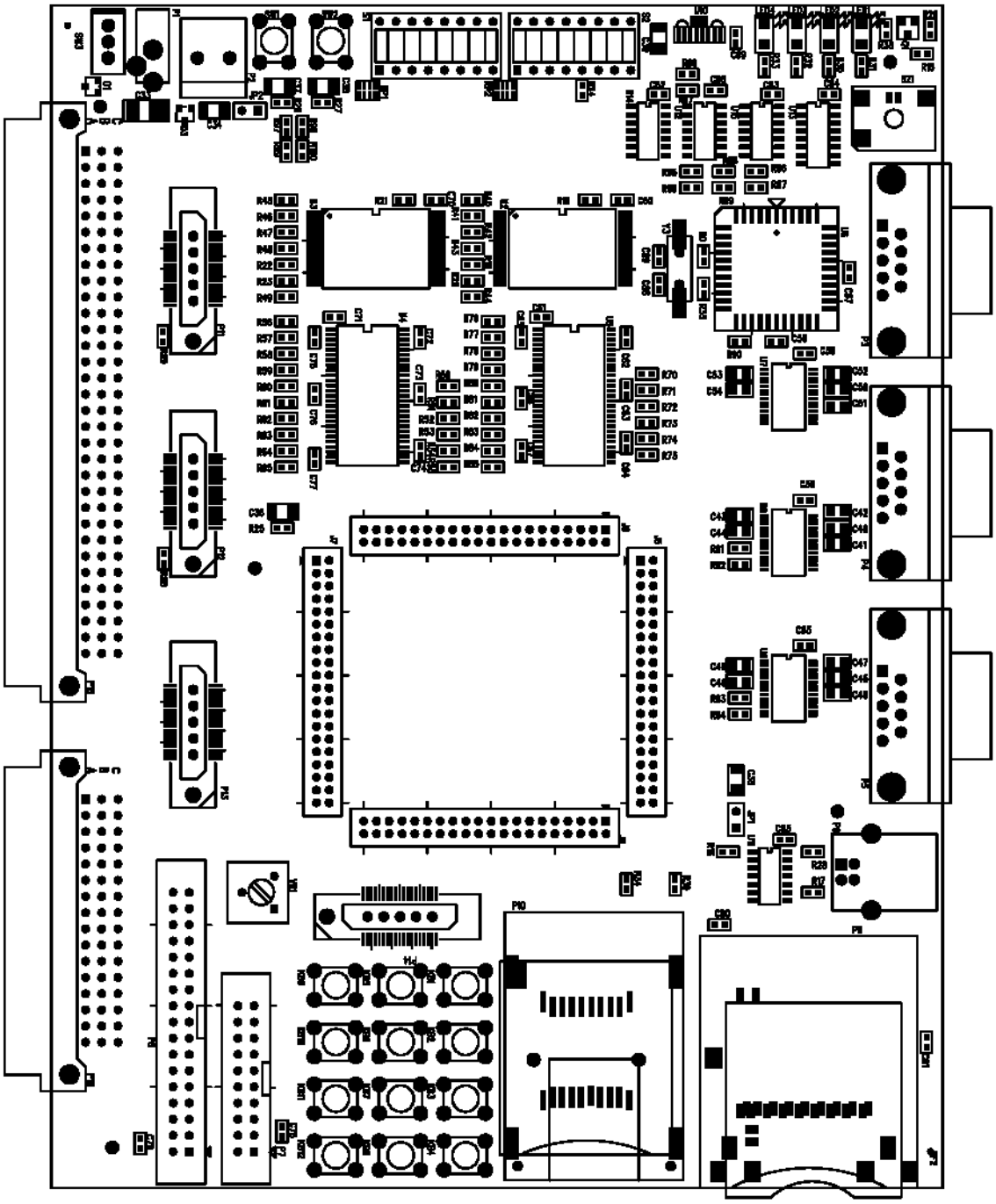


Figure 2-6. M68SZ328ADS Board Layout

2.3.2 Connecting M68SZ328ADS to PC

Figure 2-6 shows connections among the PC, the external power adaptor and the M68SZ328ADS board. Use the following steps to complete cable connections:

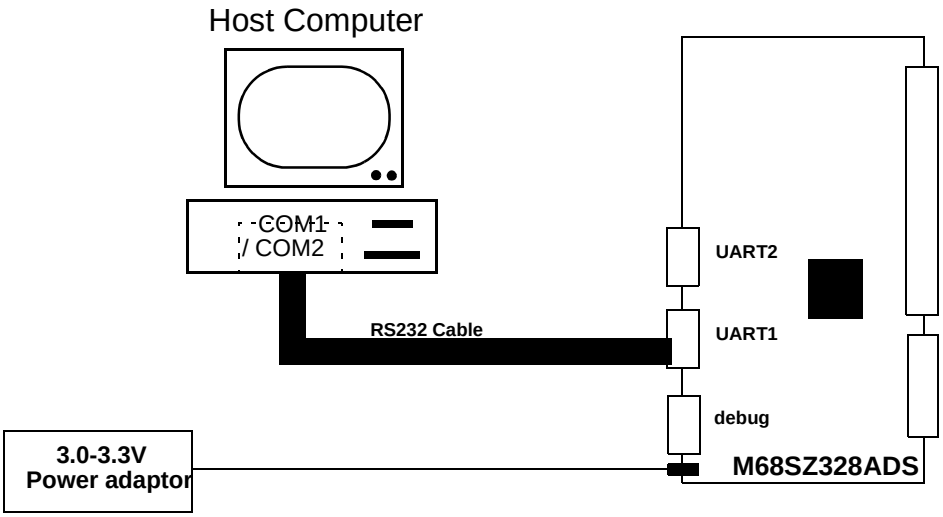


Figure 2-7. Connecting PC to UART1 of M68SZ328ADS

For most evaluation platforms, serial communication is the primary channel to link up PC with the target board. Both Microtek (SLD) and Software Development System (SDS) debug monitor support serial communication through UART port. The procedure is as follows.

1. Connect a RS232 cable from COM port (COM1 or COM2) to connector P4 of M68SZ328ADS.
2. Connect the power supply +3V or power adaptor to the P1 of M68SZ328ADS.
3. Turn on the power supply. The RED LED will flash and the GREEN LED will illuminate when power is correctly applied.

2.3.3 Installing software debugger

The following software debuggers support M68SZ328ADS:

1. MetroWerks Codewarrior
2. Single Step Development System

Metrowerks Codewarrior Setup Procedure

A simple procedure for using Metrowerks Codewarrior Target Monitor:

1. Install Metrowerks Codewarrior IDE.
2. Run Codewarrior IDE program.
3. Open a new project file with Embedded 68k Stationery.

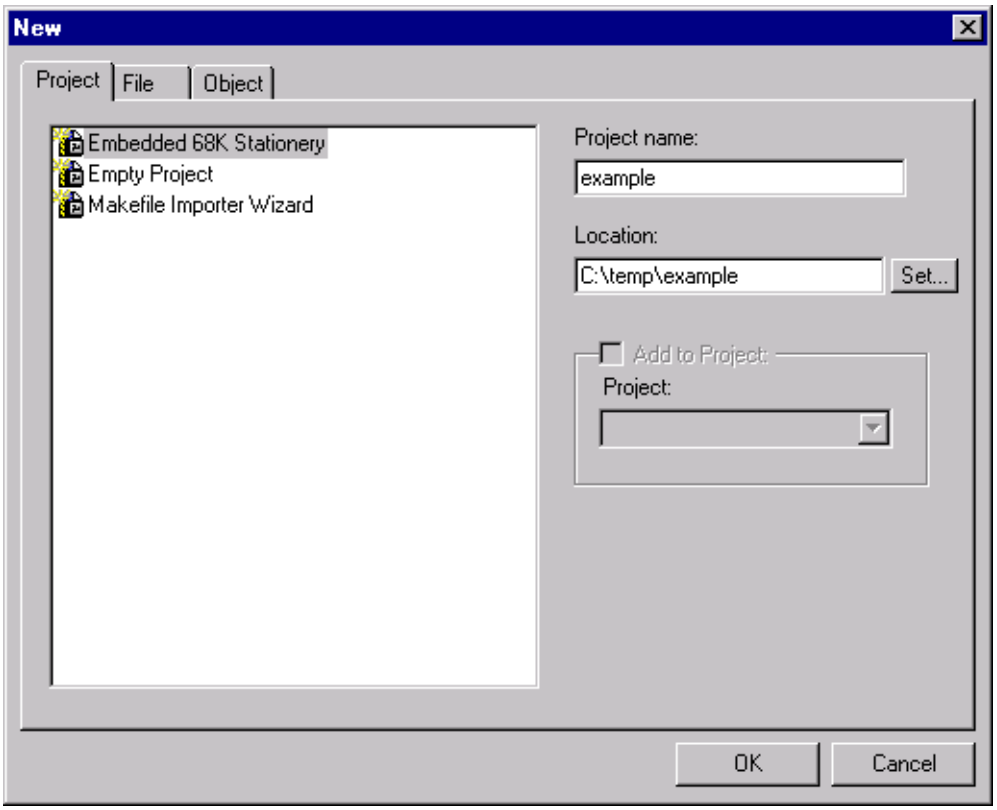


Figure 2-8. New Project in MetroWerks

4. Select ADS_68SZ328 Stationery for new project.

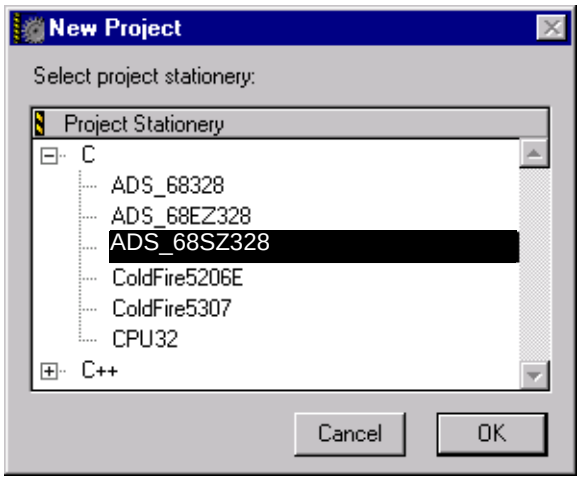


Figure 2-9. ADS_68SZ328 Stationery for new project

5. Choose "Enable Debugger" from the "Project" pull-down menu

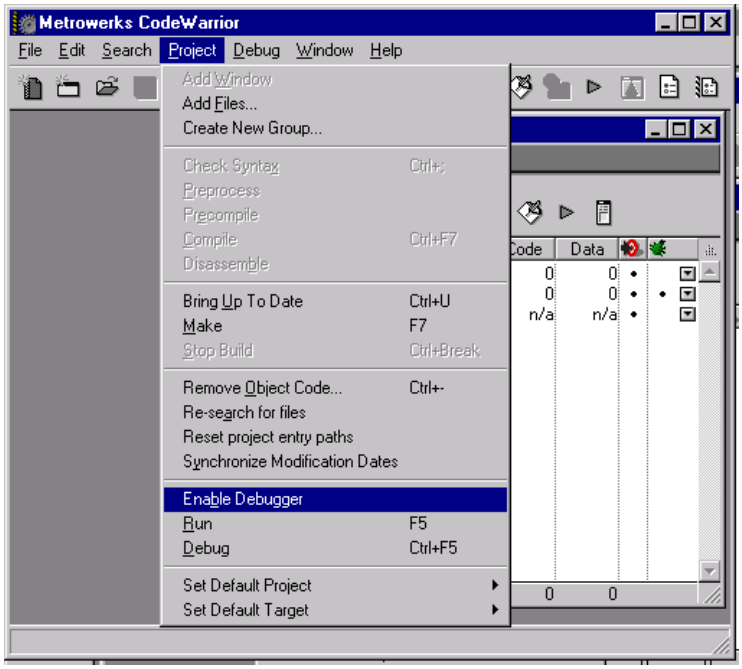


Figure 2-10. Enabling Debugger in MetroWerks

6. Change the connection settings in the Debug Settings Windows

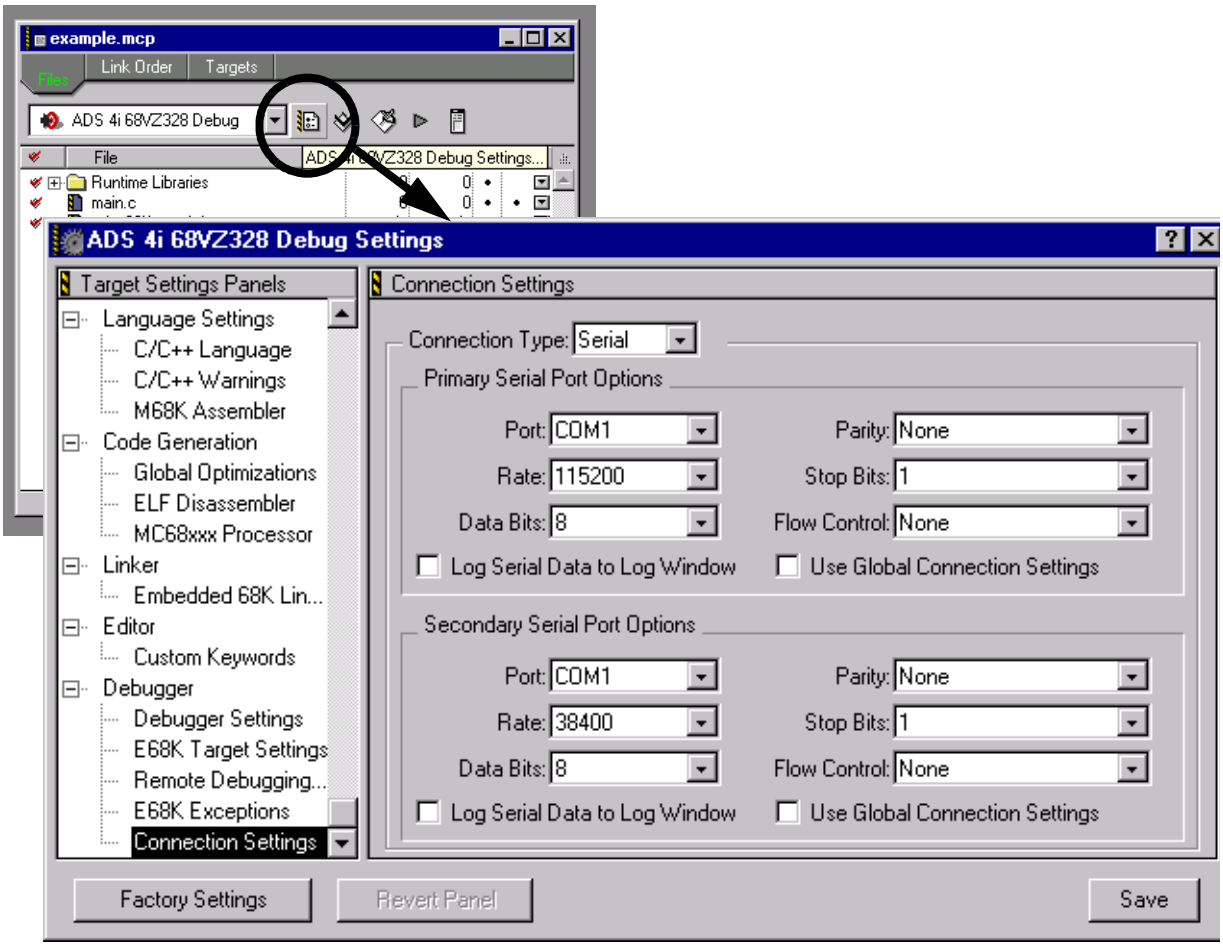


Figure 2-11. Settings in MetroWerks

7. Edit the code inside the Codewarrior IDE program.
8. .Press F5 to run the program.

Single Step Development System Setup Procedure

A simple procedure for using Single Step Debugger:

1. Install the Single Step Debugger on your PC.
2. Run Single Step Debugger.
3. Choose **Debug** in the **File** pull-down menu to open the **Debug** pop-up window.
4. Inside the **Debug** pop-up window, choose the object file to download or "debug without file" as shown in Figure 2-7, select the serial port (COM1 or COM2) according to the serial port of the PC connecting to the ADS, disable "hardware flow control" and the baud rate should be 115200bps as shown in Figure 2-8.
5. The file should be downloaded and then you can start your development. (For details, please refer to the SingleStep User's Manual).

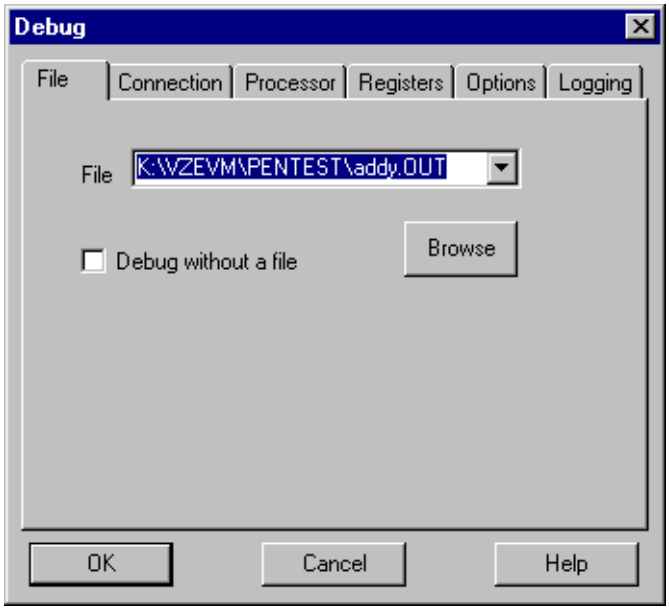


Figure 2-12. Debug Pop-Up Window of SDS v7.4

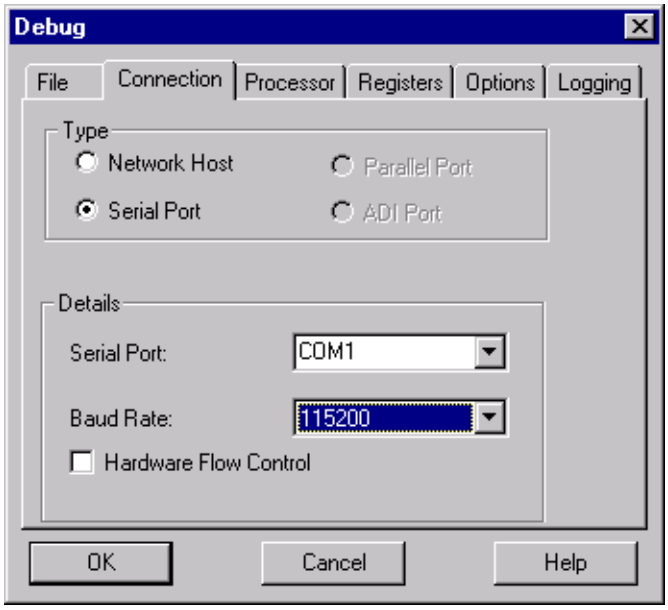


Figure 2-13. Connection Setting inside Debug Pop-Up Window for SDS v7.4

Section 3
Hardware Description and Board Operation

3.1 Overview

3.2 Control Switches

3.3 DIP Switches

3.4 Operating Modes

3.5 LED Indicators

3.6 Memory

- 3.6.1 Memory Map
- 3.6.2 Flash Memory
- 3.6.3 SDRAM

3.7 UART and IRDA

3.8 Debug Port

3.9 LCD and Touch Panel Interface

- 3.9.1 LCD Interface
- 3.9.2 Touch Panel Interface

3.10 Application Keys

3.11 MMC/SD and MemoryStick

3.12 Universal Serial Bus(USB

3.13 Single Tone Generator

3.14 Logic Analyzer Interface

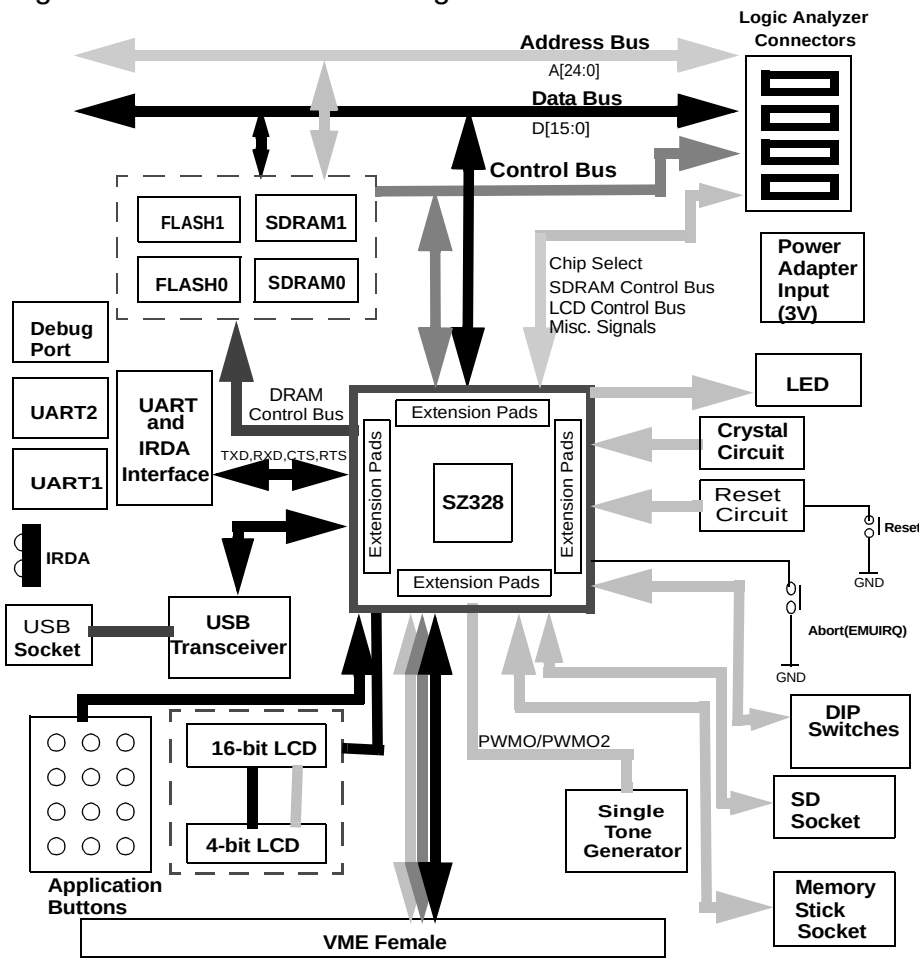
3.15 Expansion Connectors

3.16 Power Supply

SECTION 3
Hardware Description and Board Operation

3.1 OVERVIEW

Figure 3-1shows the block diagram of M68SZ328ADS:



3.2 CONTROL SWITCHES

There are two push buttons on the ADS which function as follows:

1. **Reset Switch (SW2)**: When pressed, a hardware reset is generated to the MC68SZ328 processor and resumes operation.
2. **Abort Switch (SW1):** This switch is used to generate a level 7 interrupt to the MC68SZ328 processor for aborting normal software execution and returning control.

3.3 DIP SWITCHES

There are two DIP switch packs on the ADS board, S1 and S2.S1 is used to configure the memory system and on-board peripheral such as buzzer and touch panel. S2 is used for mode selection, monitor and debug port selection and some other user-defined function. Table 3-1 and Table 3-2 show the description of each switch.

Table 3-1. DIP Switch pack S1 Setting

Switch	FUNCTION	ON	OFF
S1-1	CSA0 - FLASHCS0	Connected	Disconnected
S1-2	CSA1 - FLASHCS1	Connected	Disconnected
S1-3	CSE/SDCS0 - SDRAMCS0	Connected	Disconnected
S1-4	CSF/SDCS1 - SDRAMCS1	Connected	Disconnected
S1-5	PWMO - Buzzer	Connected	Disconnected
S1-6	UART1EN	Enabled	Stand-by
S1-7	UART2EN	Enabled	Stand-by
S1-8	IrDAEN	Enabled	Stand-by

Table 3-2. DIP Switch pack S2 Setting

Switch	FUNCTION	ON	OFF
S2-1	Monitor Select 1	0	1*
S2-2	Monitor Select 2	0	1*
S2-3	Monitor Select 3	SDS	MetroWerks*
S2-4	LCD Select	3.5 inch LCD*	3.9 inch LCD
S2-5	PB5	Tie GND	PB5*
S2-6	PB6	Tie GND	PB6*
S2-7	EMU	EMU mode(with S2-7 OFF)	Normal Mode*
S2-8	Bootstrap	Bootstrap Mode(with S2-6 OFF)	Normal Mode*

Note: * is the default setting mark

Below shows the selection of ports for debug monitors:

Table 3-3. Port Select for Monitor

DIP Switch S2-1	DIP Switch S2-2	Monitor port	Memory 0x0
0	0	Debug Port	SDRAM as 0x0
0	1	Uart1	SDRAM as 0x0
1	0	Uart2	SDRAM as 0x0
1	1	Debug port	ESRAM as 0x0

3.4 OPERATION MODES

M68SZ328ADS supports two operation modes of MC68SZ328: Normal Mode and Bootstrap Mode. Selection of those operation modes is controlled by set ting DIP switches S2-8. Operation mode has to be selected before resetting the system. Mode is not allowed to be changed during normal runing. Table 3-4 shows the operation mode configuration.

Table 3-4. Operation Mode Setting

DIP Switch S2-8	Operation Mode
ON	Bootstrap
OFF	Normal

Normal mode - After power up or system reset in this mode, CSA0 is default to cover the whole memory map except MC68SZ328 internal registers and EMU space. Also, as reset vector fetch is at the beginning of CSA0 space, CSA0 should be connected to the boot ROM in which the first two words are reset vectors. The default boot ROM of the M68SZ328ADS has been pro grammed with monitor when it is shipped out from factory. Pls. refer to Quick Installation part for detailed description on the selection of monitor and debug port.

Bootstrap mode - When this mode is selected, the DragonBall-SZ will start its embedded bootloader. User can use this mode to do simple debugging or reprogram the flash memories. Under this mode, the debug port cannot be used. For detailed bootstrap mode operation, please refer MC68SZ328 user¡fs manual.

3.5 LED INDICATORS

There are four LED indicators on the ADS which function as shown in Table 3-5

.

Table 3-5. Function of LED Indicators

Reference #	Color	Name	Function
LED1	Green	Power	Power is applied to the system with right polarity
LED2	Red	Heart Beat	Blinking heart beat indicates the system is "alive"
LED3	Yellow	PN0	Status of PN0
LED4	Yellow	PF1	Status of PF1

The LED2 is connected to a counter. The counter is toggled by address line A1.

3.6 MEMORY

M68SZ328ADS provides on-board Flash memory and SDRAM, for application development. They can be enabled or disabled individually by setting the cor responding DIP switches.

3.6.1 Memory Map

The default memory map of M68SZ328ADS in normal mode is shown in Table 3-6. The chip select range to all of the memory are software program-mable. Users can reconfigure the memory map for their applications.

Table 3-6. M68SZ328ADS Default Memory Map

System Address	Memory	Assigned Chip Select
$00000000-$00FFFFFF	16MB SDRAM BANK0	CSE
$01000000-$01FFFFFF	16MB SDRAM BANK1	CSF
$02000000-$03FFFFFF	Unused	-
$04000000-$047FFFFF	8MB FLASH BANK0	CSA0
$04800000-$04FFFFFF	8MB FLASH BANK1	CSA1
$05000000-$050187FF	98K ESRAM	CSG
$05018800-$FFFDFFFF	Unused	-
$FFFE0000-$FFFFFDFF	MC68SZ328 Internal Register	-

3.6.2 FLASH Memory

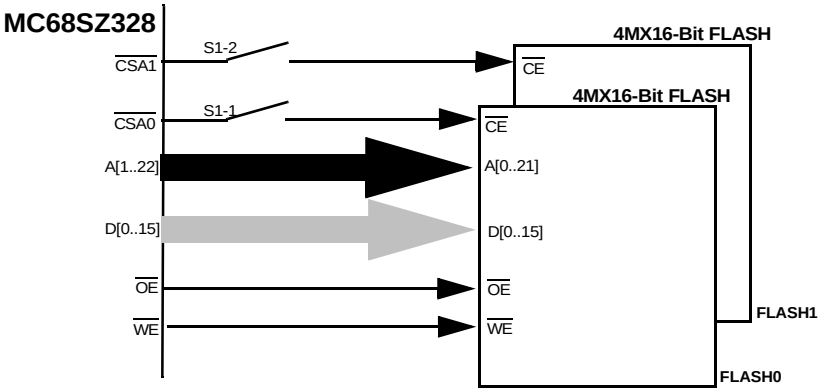


Figure 3-2. Interface of Flash Memories

M68SZ328ADS is equipped with two 8M-byte Flash memory chips. Figure 3-2. shows the interface of them. They are chip-selected by *CSA0 and *CSA1 signals. The connection of these *CSAx signals to the Flash memories is controlled by DIP switches S1-1 and S1-2.

For more details on flash memory programming, please refer to Appendix B

3.6.3 SDRAM

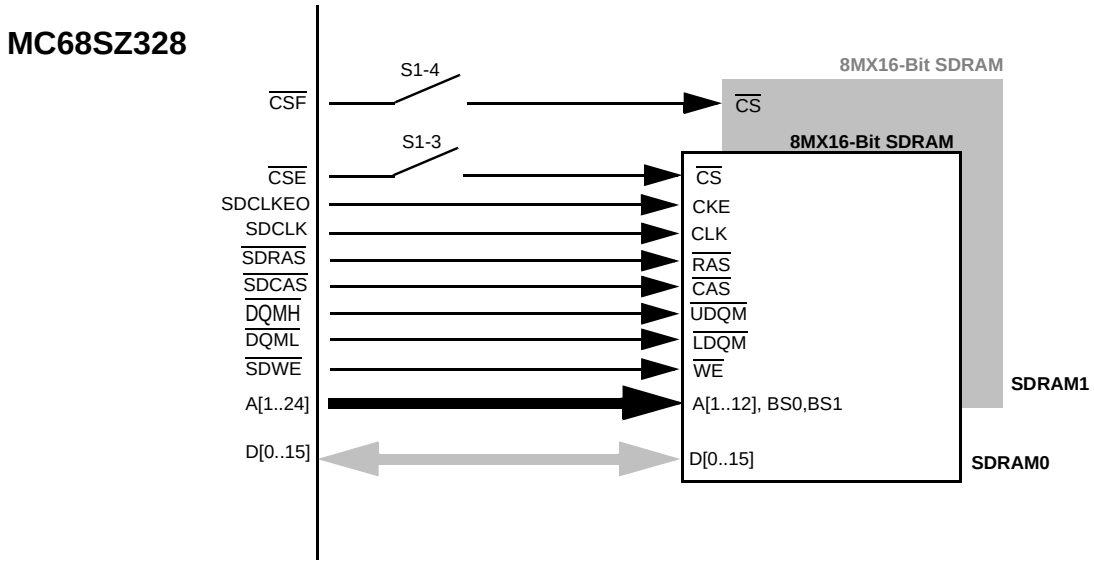


Figure 3-3. Interface of SDRAMs

Figure 3-3. shows the interface of SDRAMs. M68SZ328ADS supports two banks of 8Mx16-bit SDRAMs. Two banks are installed when the board is shipped out from the factory. These two banks of SDRAM are selected by *CSE and *CSF, and enabled by closing DIP switches S1-3 and S1-4.

3.7 UART AND IRDA

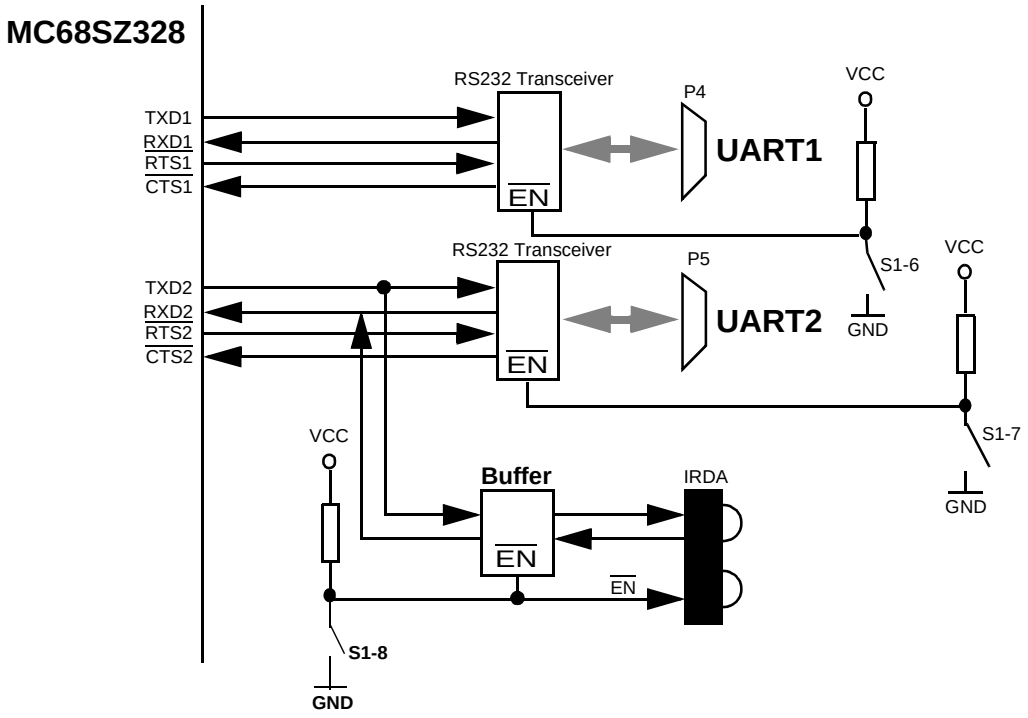


Figure 3-4. UART and IRDA Interface.

Figure 3-4 shows the UART and IRDA interface. The M68SZ328 has two RS232 serial ports, P4 and P5. P4 and P5 are using the UART1 and UART2 of MC68SZ328 respectively. Both P4 and P5 are 9-pin female D-Type connectors containing the signals as shown in Figure 3-5. The transceivers for UART1 and UART2 can be enabled by turning the DIP switch S1-6 and S1-7 on respectively.

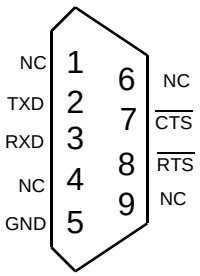


Figure 3-5. Serial Port Pin Assignment

The IRDA transceiver is connected to UART2 only with a buffer in between for controlling its ON/OFF. If IRDA is being used, S1-7 should be switched OFF and S1-8 should be switched ON.

3.8 DEBUG PORT

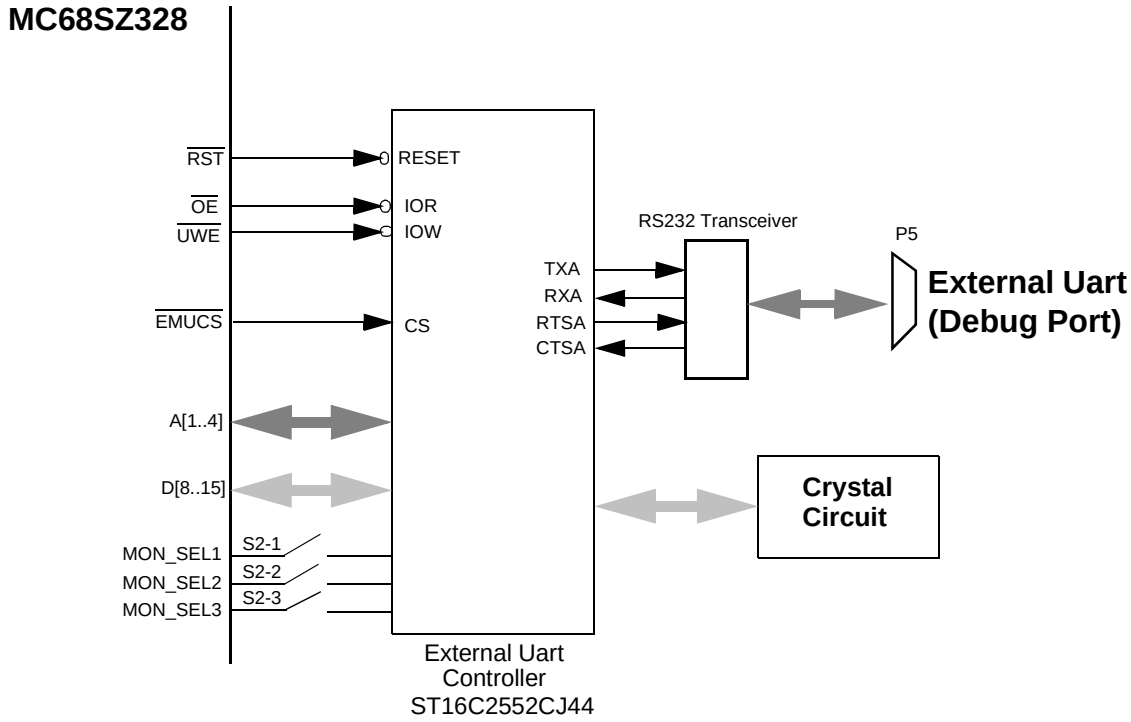


Figure 3-6. Debug Port Interface.

Figure 3-5 shows the inferface of External Uart with MC68SZ328 the external Uart controller, ST16C2552CJ44. There is a transceiver between the controller and the port connector and the controller has its own crystal circuit. This External Uart is mainly for debugging use.

3.9 LCD AND TOUCH PANEL INTERFACE

3.9.1 LCD Interface

M68SZ328ADS consists of two LCD panel connectors, P7 and P8. P8 is designed for 16-bit TFT LCD panel while P7 is for 4-bit LCD panel. P7 is fully compatible with the one used on M68VZ328ADS. The pin assignments of both LCD connectors are shown in Figure 3-7.

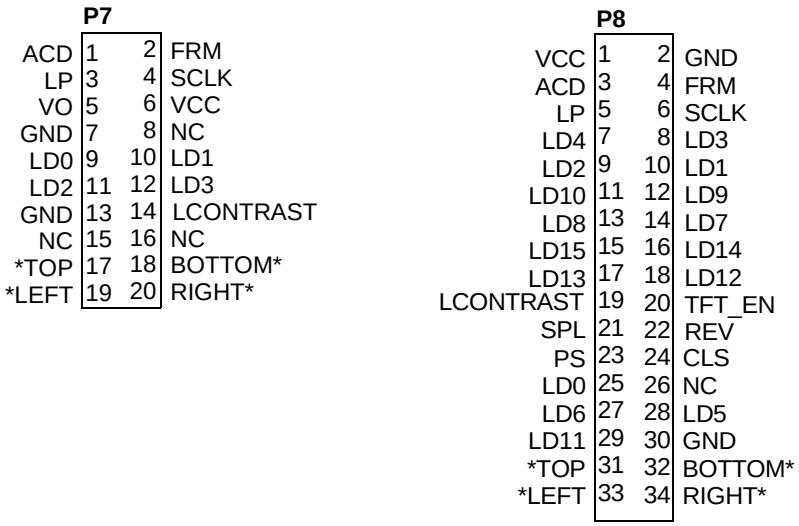


Figure 3-7. LCD and Touch Panel Connector Pin Assignment

For full description of the LCD signals, please refer to the MC68SZ328 User's Manual.

* Note : Those parts have been updated. For the latest information, please refer to the board update file in CD-ROM

3.9.2 Touch Panel Interface

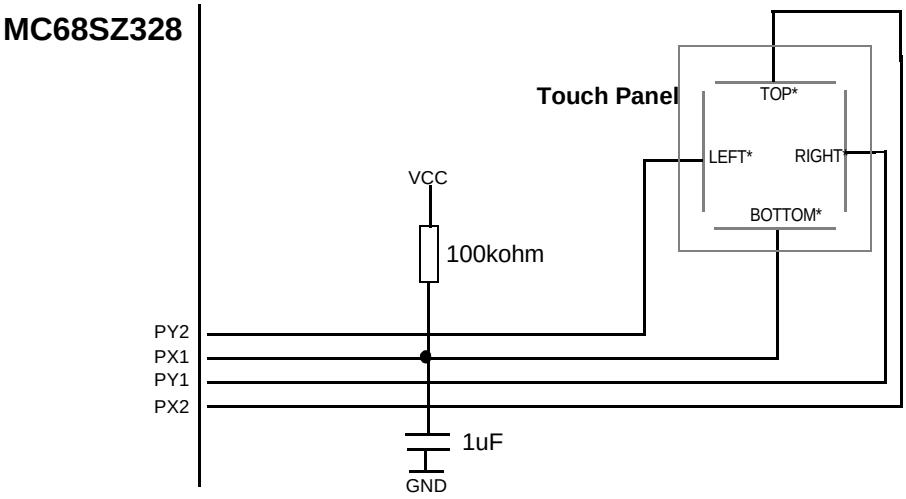


Figure 3-8. Touch Panel Controller Interface

Figure 3-7 shows the simple connection for the touch panel with MC68SZ328. A pull-up resister is needed to connect to PX1 for generating screen-touch interrupt signal while the capacitor is for reducing noise.

Note : Those parts have been updated. For the latest information, please refer to the board update file in CD-ROM

3.10 APPLICATION KEYS

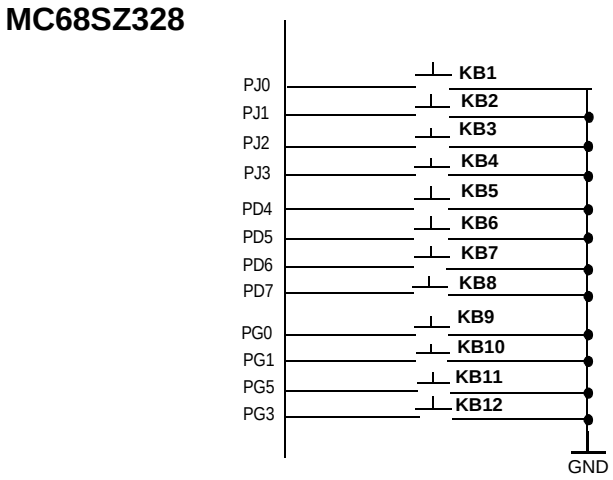


Figure 3-9. APPICATION KEYS

Figure 3-8 shows the application keys which are directly connected to MC68SZ328 and can be configured and programmed by the users directly.

3.11 MMC/SD AND MEMORY STICK

There are one MultiMedia Card(MMC)/Secure Digital Card(SD) socket and one Memory Stick (MS) on the M68SZ328ADS board. The signals of the MMC/SD and the Memory Stick are multiplexed together. Only one of them can be used at one time

3.12 UNIVERSAL SERIAL BUS(USB)

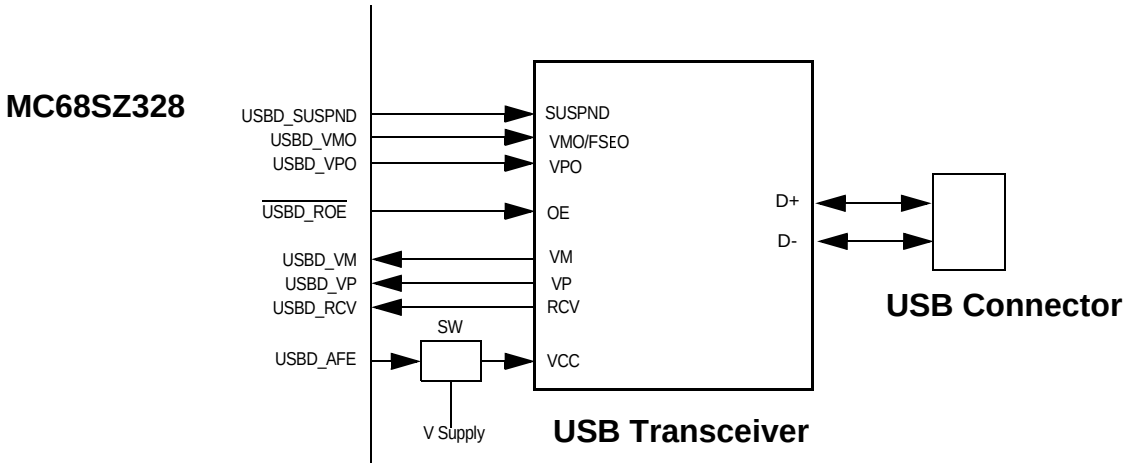


Figure 3-10. USB

Figure 3-9 shows the USB module connection with MC68SZ328. A USB transceiver is already built on board for interfacing with external USB host.

3.13 SINGLE TONE GENERATOR

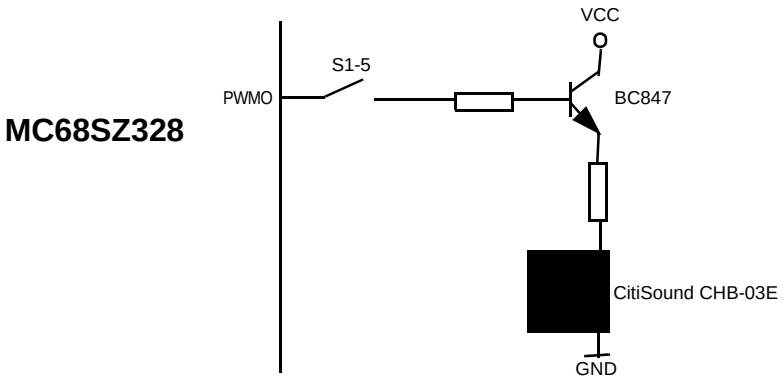


Figure 3-11. Single Tone Generator

The M68SZ328ADS is equipped with Citizen single tone generator CHB-03E. As shown in Figure 3-11, a simple transistor circuit is used to interface the CHB-03E with the PWMO pin of MC68SZ328.

3.14 LOGIC ANALYZER INTERFACE

To provide an convenient way of connecting on-board signals to a logic analyzer, ADS board provides four 38-pin headers for direct plug-in. Pin assign ments to these four headers are shown in Figure 3-12.

P11

NC	1	2	NC
GND	3	4	NC
NC	5	6	SDCLK
D15	7	8	SDCLK
D14	9	10	SDCLKE1
D13	11	12	SDCLKE0
D12	13	14	DWEB
D11	15	16	SDCASB
D10	17	18	SDRASB
D9	19	20	SDCS1B
D8	21	22	SDCS0B
D7	23	24	DQMH
D6	25	26	DQML
D5	27	28	MA11
D4	29	30	MA10
D3	31	32	CSB1B
D2	33	34	CSB0B
D1	35	36	CSA1B
D0	37	38	CSA0B

P12

NC	1	2	NC
GND	3	4	NC
NC	5	6	CLKO
A15	7	8	CLKO
A14	9	10	OEB
A13	11	12	WEB
A12	13	14	LWEB
A11	15	16	UWEB
A10	17	18	PG0
A9	19	20	RSTB
A8	21	22	A24
A7	23	24	A23
A6	25	26	A22
A5	27	28	A21
A4	29	30	A20
A3	31	32	A19
A2	33	34	A18
A1	35	36	A17
A0	37	38	A16

P13

NC	1	2	NC
GND	3	4	NC
NC	5	6	NC
REV	7	8	LD15
CLS	9	10	LD14
PS	11	12	LD13
SPL	13	14	LD12
LCONTRAST	15	16	LD11
ACD	17	18	LD10
SCLK	19	20	LD9
LP	21	22	LD8
FRM	23	24	LD7
PWMO1	25	26	LD6
MMC_DAT3	27	28	LD5
MMC_DAT2	29	30	LD4
MMC_DAT1	31	32	LD3
MMC_DAT0	33	34	LD2
MMC_CMD	35	36	LD1
MMC_CLK	37	38	LD0

P14

NC	1	2	NC
GND	3	4	NC
NC	5	6	NC
PJ2	7	8	PB5
PJ0	9	10	PB4
PJ1	11	12	CSC1B
PJ3	13	14	CSC0B
PWMO2	15	16	EMUCSB
PE0	17	18	EMUIRQB
PE1	19	20	PG5
CTS2B	21	22	PG3
RTS2B	23	24	USBD_AFE
TXD2	25	26	USBD_ROEB
RXD2	27	28	USBD_VMO
PE3	29	30	USBD_VPO
CTS1B	31	32	USBD_SUSPND
RTS1B	33	34	USBD_RCV
TXD1	35	36	USBD_VP
RXD1	37	38	USBD_VM

Figure 3-12. Logic Analyzer Connectors

3.15 EXPANSION CONNECTORS

The M68SZ328ADS provides basic features for software development and evaluation. If user wants to add application subsystem to M68SZ328ADS, it can utililize the signals provided on 32x3 local bus connector (P15) and 16x3 local bus connector (P16). Some of these MC68SZ328 signals are used by the on-board modules. If users want to use any of these signals for their daughter card, the corresponding on-board module may have to be disabled to avoid contention.

The pin assignments for extension connectors are shown in Table 3-7 and Table 3-8.

Table 3-7. Pin Assignments of P15

Pin#	A	B	C
1	GND	GND	GND
2	D0	D1	D2
3	D3	D4	D5
4	D6	D7	D8
5	D9	D10	D11
6	D12	D13	D14
7	D15	CSA0	CSA1
8	PB0/CSB0	PB1/CSB1	PB2/CSC0
9	PB3/CSC1	PB4/CSD0	PB5/CSD1
10	PB6/TIN1/TOUT1	PB7/PWMO1	PC0/LD0
11	PC1/LD1	PC2/LD2	PC3/LD3
12	PC4/FRM/VSYNC	PC5/LP/HSYNC	PC6/SCLK
13	PC7/ACD/OE	PD0/SPL/SPR	PD1/PS
14	PD2/CLS	PD3/REV	PD4/IRQ1
15	PD5/IRQ2	PD6/IRQ3	PD7/IRQ6
16	N.C.	N.C.	N.C.
17	PM4/SDWE/DWE	PE4/RXD1	PE5/TXD1
18	PE6/RTS1	PE7/CTS1	PF0/LCONTRAST
19	PE2/A24	PF2/CLKO	PG1/A0/MA0
20	A1/MA1	A2/MA2	A3/MA3
21	A4/MA4	A5/MA5	A6/MA6
22	A7/MA7	A8/MA8	A9/MA9
23	A10	A11	A12
24	A13	A14	A15
25	A16/SDBIA9	A17	A18
26	A19	PF3/A20	PF4/A21
27	PF5/A22	PF6/A23	PG2/EMUIRQ
28	PG3/P/D	PG4/EMUCS	PG5/EMUBRK
29	PG0/BUSW/DTACK	RST	OE
30	UWE/U	LWE/LB	N.C.
31	N.C.	PK1/R/W/WE	N.C.
32	VCC	VCC	VCC

Table 3-8. Pin Assignment of P16

Pin#	A	B	C
1	GND	GND	GND
2	PM0/SDCLK	PM1/SDCLKE0/DOE	PM2/DQM0
3	PM3/DQM1	PM6/MA10	PM7/MA11
4	PK4/LD4	PK5/LD5	PK6/LD6
5	PK7/LD7	PJ4/RXD2	PJ5/TXD2
6	PJ6/RTS2	PJ7/CTS2	PJ0/MOSI
7	PJ1/MISO	PJ2/SPICLK	PJ3/SS
8	PK0/DATA_READY/PWMO2	PP0/LD8	PP1/LD9
9	PP2/LD10	PP3/LD11	PP4/LD12
10	PP5/LD13	PP6/LD14	PP7/LD15
11	PG6/CSE/SDCS0/RAS0	PG7/CSF/SDCS1/RAS1	PM5/SDCLKE1
12	PK2/SDRAS/CAS0	PK3/SDCAS/CAS1	PF1/TIN2/TOUT2
13	PE3/UCLK	PE1/SCL	PE0/SDA
14	NC	NC	NC
15	NC	NC	NC
16	VCC	VCC	VCC

3.16 POWER SUPPLY

There are two power input connectors on the ADS, P1 and P2. P1 is designed for external 3V DC main power supply, which supplies power to the MC68SZ328 processor and most of the on-board components. P2 is used to supply power for memory modules. Figure 3-13 locates the power connectors and their polarity.

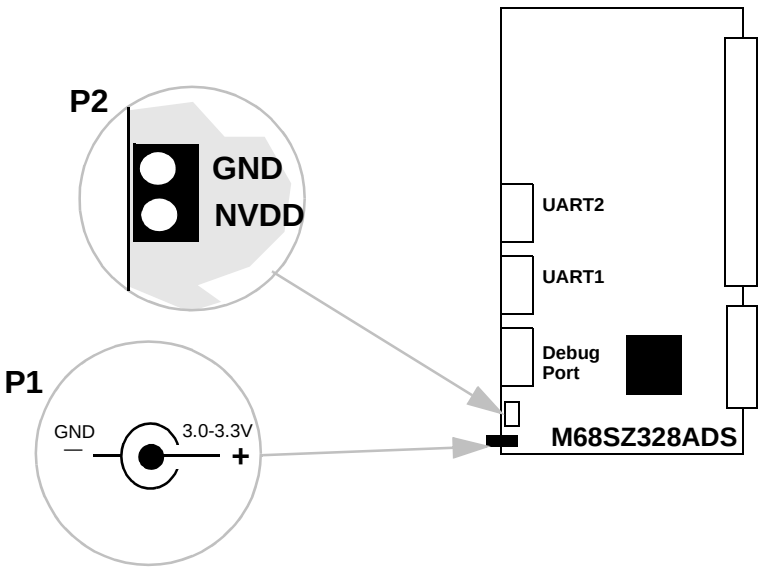


Figure 3-13. Power Connectors

Section 4
Appendix

Appendix A	**Resistive Touch Panel Operation**
Appendix B	**Programming On-board Flash Memory**
Appendix C	**Monitor Initialization Code**
Appendix D	**M68SZ328ADS Schematic**
Appendix E	**Difference between SZADS Ver1.0 and Ver1.1**
Appendix F	**How to Use BBUG Windows Version**

APPENDIX A
RESISTIVE TOUCH PANEL OPERATION

A.1 OVERVIEW

M68SZ328ADS features pen input through a resistive-film sensing panel. This type of panel provides high flexibility by accepting input form any kind of stimulus including fingers, which is most suitable for portable use. User can select a specific touch panel or order an LCD module which includes a touch resistive panel. This section describes the basic concepts of pen input and the required interface with the M68SZ328ADS.

A.2 GENERAL CONCEPTS OF RESISTIVE PANELS

Basically, resistive panel consists of two transparent resistive layers separated by insulating spacers as shown in Figure 1

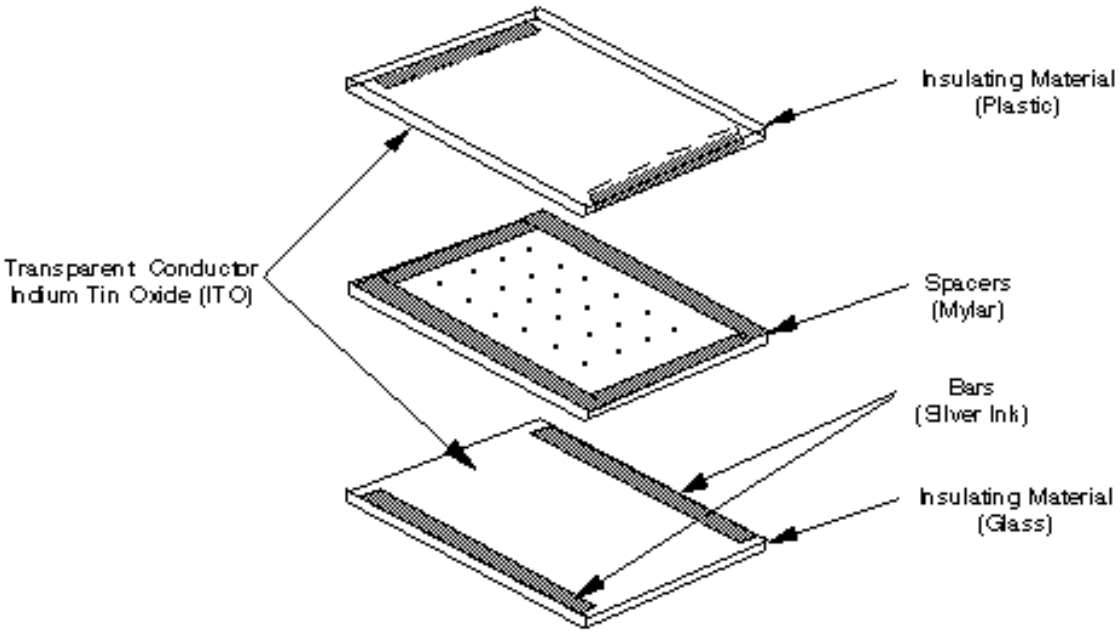


Figure A-1. Resistive Touch Panel

Transparent Resistive Layer

-resistive material such as an indium tin oxide (ITO) film is coated on dielectric (insulating) substrate, usually glass on bottom and plastic on top for actuation.

Bars

-highly conductive material such as silver ink, about 1000 times more conductive than ITO.

Spacers

-The resistive panel works by applying a voltage gradient across one conductive layer and measuring the voltage at the point of contact with the opposing conductive layer. For instance, as shown in Figure 2, the resistive film acts as a series of resistors.

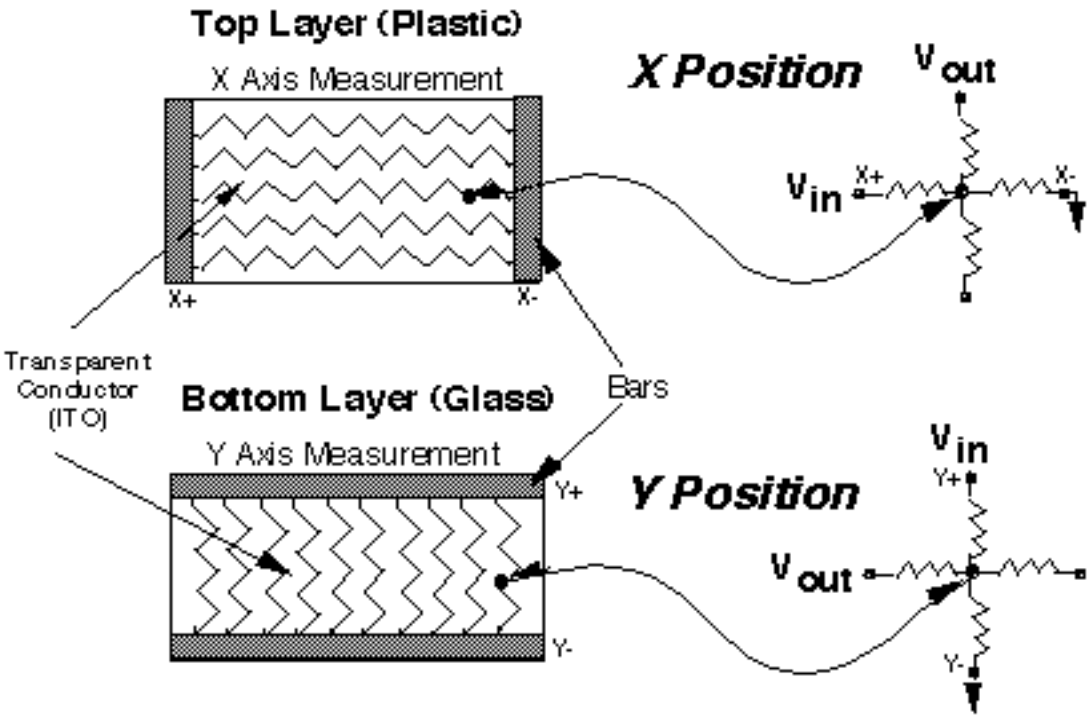


Figure A-2. Determination of X,Y Position

When a point is contacted, it means the two opposing conductive layers come into electrical contact. The x position of actuation can be determined by mea suring the output voltage of the y layer. At the same time, the y position can be find out by measuring the x layer. The exact position can be determined by referencing the output voltage to the distance relationship.

APPENDIX B
PROGRAMMING ON-BOARD FLASH MEMORY

B.1 OVERVIEW

The Flash memory on the ADS board cannot be written directly. A special program command sequence is required to unlock it before starting the write process. A flash program is therefore provided with the ADS board for helping users to do re-programming. The sections below will describe the program and provide further information about the process and other required elements.

It is recommended that user should have a basic understanding of bootstrap mode operation of MC68SZ328 before reading the material below. For more details on Bootstrap mode, please refer to the MC68SZ328 user's manual.

B.2 ELEMENTS FOR PROGRAMMING THE FLASH

The following files are necessary for programming the Flash memory

1. SZADSTOOLS including BBUGSZ.EXE and STOB.EXE

2. INIT.B - b-record for initialize the ADS

3. FLASHNML.B - b-record for programming flash. ROM image is copied from RAM area to the Flash memory area

4. ROM.B - ROM image of user program in b-record/s-record format.

B.3 METHOD

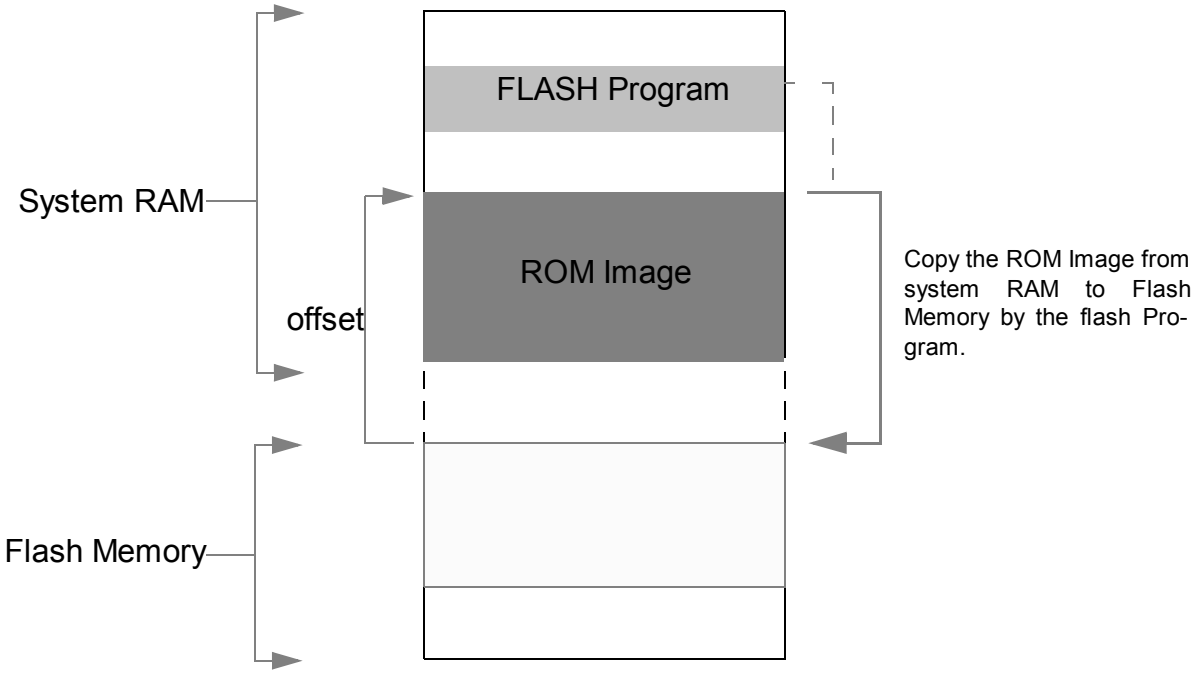


Figure B-1. Method of programming on-board Flash memory

Flash memory can be programmed in bootstrap mode. First, a ROM image and a flash program are downloaded to the system memory by loading their b-records. Then, run the flash program. It will execute the Flash program com mand sequence and copy the ROM image from the system RAM to the Flash memory. The detailed steps are as follows.

1. Force the MC68SZ328 into bootstrap mode by turning S2-8 on and pressing RESET switch once.

2. Use BBUGSZ.EXE or TERMINAL program to communicate with the M68SZ328ADS through RS232 port of a PC.

3. Initialize the internal registers of DragonBall-SZ by loading the INIT.B.

2. Use BBUGSZ.EXE or TERMINAL program to communicate with the M68SZ328ADS through RS232 port of a PC.

4. Load FLASHNML.B (the Flash Program) and ROM.B (the ROM image) to system RAM (SDRAM on M68SZ328ADS).

5. Execute the Flash Program by using the execution B-record. For example, if the starting address of Flash Program is 0x2000, the execution B-record is then "0000200000".

B.4 OFFSET ADDRESS OF ROM IMAGE

Figure 1The ROM image is first put to the system RAM before it is copied to Flash. In order to create S-record/B-record with download address different from its execution address, an OFFSET is sometimes required to be specified in downloader program.
For example, when using SDS's DOWN.EXE to generate the s-record, the "-w offset" parameter can be used to specify this offset value. Please refer to the SingleStep User Guide for using this command.

B.5 FLASH PROGRAM

Listed below is the source code of the flash Program which contains the necessary steps to write the flash memory. It executes the flash program command sequence and copies the ROM image from RAM area to the Flash memory area on ADS board. Figure 2 show the flow chart of this program. Different brands of Flash memory may have different program command sequences.

```
;       -Code to copy data from memory into Fujitsu MBM29DL640E flash.
;       -It assumes 1 flash chip in word mode.
;       -This code assumes a top-boot device.
;       -It also assumes that the starting flash address is at the beginning of a sector.

FLASH_BASE      .equ            $04000000

        .section .flashinit
        .extern ___FBUF_START
        .extern ___FBUF_END
        .extern ___FLASH_START
        .globalcopy_to_flash

copy_to_flash:

        ;
        ; Set up registers:
        ;a0 - flash image source start addr (in RAM)
        ;a1 - flash image source end addr (in RAM)
        ;a2 - flash image dest addr (in FLASH)
        ;
```

```
        move.l    #___FBUF_START,a0; source addr of flash image
        move.l    #___FBUF_END,a1  ; end addr of source flash image
        move.l    #___FLASH_START,a2; dest addr of flash image

        move.l    #$555*2,d1                ; load command offset 1 to d1
        move.l    #$2aa*2,d2                ; load command offset 2 to d2


        ;
        ; Erase the next sector.  Each sector must be erased before it
        ; can be programmed.
        ;

erase_loop:
        cmp.l     a0,a1                     ; if done copying, verify
        ble       do_compare

        move.l    a2,d0
        and.l     #$ff800000,d0             ; calc. base addr of current chip
        move.l    d0,a3

        move.w    #$aa,(d1.l,a3)            ; unlock step 1
        move.w    #$55,(d2.l,a3)            ; unlock step 2
        move.w    #$80,(d1.l,a3)            ; sector erase setup
        move.w    #$aa,(d1.l,a3)            ; unlock step 1
        move.w    #$55,(d2.l,a3)            ; unlock step 2
        move.w    #$30,(a2)                 ; erase current sector

erase_verify_loop:
        move.w    (a2),d0                   ; check sector data
        cmp.w     #$ffff,d0                 ; erased?
        bne.s     erase_verify_loop         ; if not, keep checking


do_program:
        ; Get the sector size, which depends on the sector offset.
        ; This code assumes a top-boot device.  It also assumes
        ; that the starting flash address is at the beginning
        ; of a sector.

        move.l    a2,d0
        sub.l     a3,d0                     ; get offset of sector
```

```
        cmp.l#$00010000,d0          ; is it sa8 or higher?
        bge.scheck_sa134            ; if so, do more tests
        brasize_8k                  ; otherwise, size is 8K

check_sa134
        cmp.l#$007f0000,d0          ; is it sa134 or higher?
        bge.ssize_8k                ; if so, size is 8K
        brasize_64k                 ; otherwise, size is 64K

size_8k
        move.l#$00002000,d0         ; otherwise, size is 8K
        braprogram_loop

size_64k
        move.l#$00010000,d0         ; otherwise, size is 64K
        braprogram_loop

program_loop:

        move.w  #$aa,(d1.l,a3)      ; unlock step 1
        move.w  #$55,(d2.l,a3)      ; unlock step 2
        move.w  #$a0,(d1.l,a3)      ; program command

        move.w  (a0),d3
        move.w  d3,(a2)             ; write data to flash

program_verify_loop:
        cmp.w   (a2),d3             ; data written?
        bne.s   program_verify_loop ; if not, wait

        add.l   #2,a0               ; next word
        add.l   #2,a2               ; next word

        cmp.l   a0,a1               ; done copying?
        ble.s   do_compare          ; if so, verify

        sub.l   #2,d0               ; next word
        beq     erase_loop          ; if end of sector, erase next
        bra.s   program_loop        ; otherwise, copy next word


        ; Verify that the flash contents were written correctly.
do_compare:
```

```
        move.l  #___FBUF_START,a0       ; source addr of flash image
        move.l  #___FBUF_END,a1         ; end addr of source flash image
        move.l  #___FLASH_START,a2      ; dest addr of flash image

compare_loop:
        cmp.w   (a0)+,(a2)+
        bne     prog_fail

        cmp.l   a0,a1                   ; is entire image verified?
        bgt     compare_loop            ; if not, repeat

        trap    #0                      ; done
        nop

prog_fail:
        trap    #1                      ; failed
        nop
```

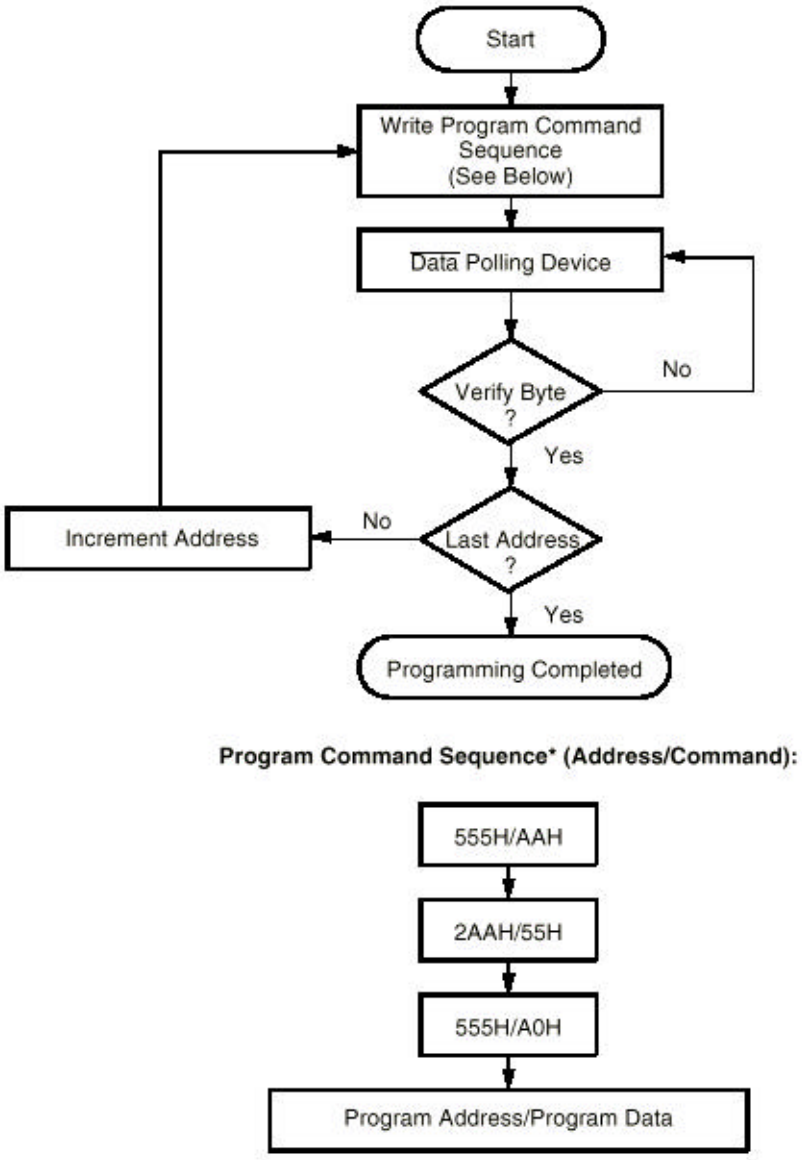


Figure B-2. Flash Program Algorithm

APPENDIX C
MONITOR INITIALIZATION CODE

C.1 OVERVIEW

The M68SZ328ADS Board default has a monitor programmed inside for debugging or other purpose. The monitors include Metrowerks(MW) and Single Step Developement(SDS) and it is chosen by DIP switches. The purpose of this section is to teach user how to program the monitor in order that it can be reloaded in case of any changes in flash memory. The procedures will be provided in the following sub-section.
If the user would like to get a source code for reference, it can be found under the CD-ROM:<SZADSTOOLS installed folder>\sourcecode\monitor\

1. *Metrowerks Source code with serial port selection.(Reset_SZADS_128NI.s)*
2. *Metrowerks Source code using default serial port. (Reset_SZADS_128NI_Px.s)*
3. *SDS Source code. (Sdsnml.h)*

The programming process described in this section is a multiboot monitor.(i.e.SDS and MW are included). Apart from it, there are different preferences on chosing monitor. For the detail description on other preferences, and the files, please refer to the file “SZADStools_readme.txt” in the CD-ROM.

C.2 PROCEDURES FOR BURNING MW AND SDS MONITORS

This process requires you to run the BBUGSZ program from the SZADS tools suite. BBUGSZ.EXE is a 16-bit application, so it is better to use it with MS-DOS or Microsoft Windows 95/98/NT, if the O.S. is Windows 2000.
it is recommended to use BBUG for Windows.

1. Power the board off and connect the P3(UART Port) of M68SZ328ADS board to COM1 or COM2 of your host PC using a standard serial cable.

2. Move switch S2-8 (BOOTSTRAP) to the ON position. Without this switch, BBUG will report an error. For detail information about DIP switch setting, please refer Section 3 "Hardware description and Board Operation¨.

3. Copy the S-record file generated by MetroWerks(*.S19) to directory: <SZADSTOOLS installed folder>\sourcecode\monitor\mwsds, rename the file as following:

SZADS_128NI_P0.elf.s19	=>	MWNML0.s19
SZADS_128NI_P1.elf.s19	=>	MWNML1.s19
SZADS_128NI_P2.elf.s19	=>	MWNML2.s19
SZADS_ESRAM_P3.elf.s19	=>	MWNML3.s19

If SDS is purchased, run SDSNMlx.bat in folder: <SZADSTOOLS installed folder>\sourcecode\monitor\SDSNML

4. Execute MWSDS.bat to generate MWSDS.b, copy MWSDS.b to <SZADSTOOLS installed folder>\exe.

5. Power on the M68SZ328ADS board, launch BBUGSZ.EXE on PC host.

6. Enter the command under BBUGSZ,

a. Select the communications port: "1" "1";
b. Change baud rate to 115200: "cb" "2";
c. Load b recorder of boot image "in mwsds.b";

At this point, BBUGSZ will begin downloading and programming the MetroTRK (and SDS monitor) to the M68SZ328ADS board.

d. Load b recorder of user-defined boot image: "in UserBoot.b",

At this point, BBUGSZ will begin downloading and programming the user-defined boot image to the M68SZ328ADS board.

7. Power off the board and set switch S2-8 (BOOTSTRAP) to the OFF position, set switch S2-1,S2-2 and S2-3 to select monitor type and communicating port.

8. Power the board on. If MetroTRK or SDS was successfully installed, the red LED(beat) will blink.

9. To connect the CodeWarrior debugger to the M68SZ328ADS board, connect the serial cable to the appropriate port for the MetroTRK image you used(see list of targets in burn_monitor.txt). Be sure to exit BBUG in order to free the port on the host PC.

APPENDIX D
M68SZ328ADS SCHEMATICS

The Schematics are divided into two parts :

1. The MC68SZ328 CPU Board Ver 1.1 Schematics
2. The M68SZ328ADS Peripheral Board Ver 1.1 Schematics

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2 Dai King Street, Tai Po Industrial Estate, Tai Po, NT, Hong Kong.

Motorola Semiconductors Suzhou Design Centre.

11F CCB 27 Shishan Road, SND, Suzhou, Jiangsu, China.

Product Name: **M68SZ328ADS CPU Board**

Version: 1.1

File Name: SZADS_CPU_Ver11.DSN
Designer: Shark Wu
Last Updated: Dec 17, 2001

Motorola Semiconductors Hong Kong Ltd
2 Dai King Street,Tai Po Industrial Estate, Tai Po, NT, Hong Kong.

Motorola Suzhou Technology Centre.
11F CCB 27 Shishan Road, SND, Suzhou, Jiangsu, China.

Title: M68SZ328ADS CPU Board		
Size: A	Document Number: SZADS_CPU_Ver11.DSN	Rev: 1.1
Date: Thursday, January 11, 2001	Sheet 1 of 4	

Revision History:

Version 1.0: Released for M68SZ328ADS CPU board Ver1.0 PCB.

Version 1.1: Replaced R9 with a 0 ohm resistor.

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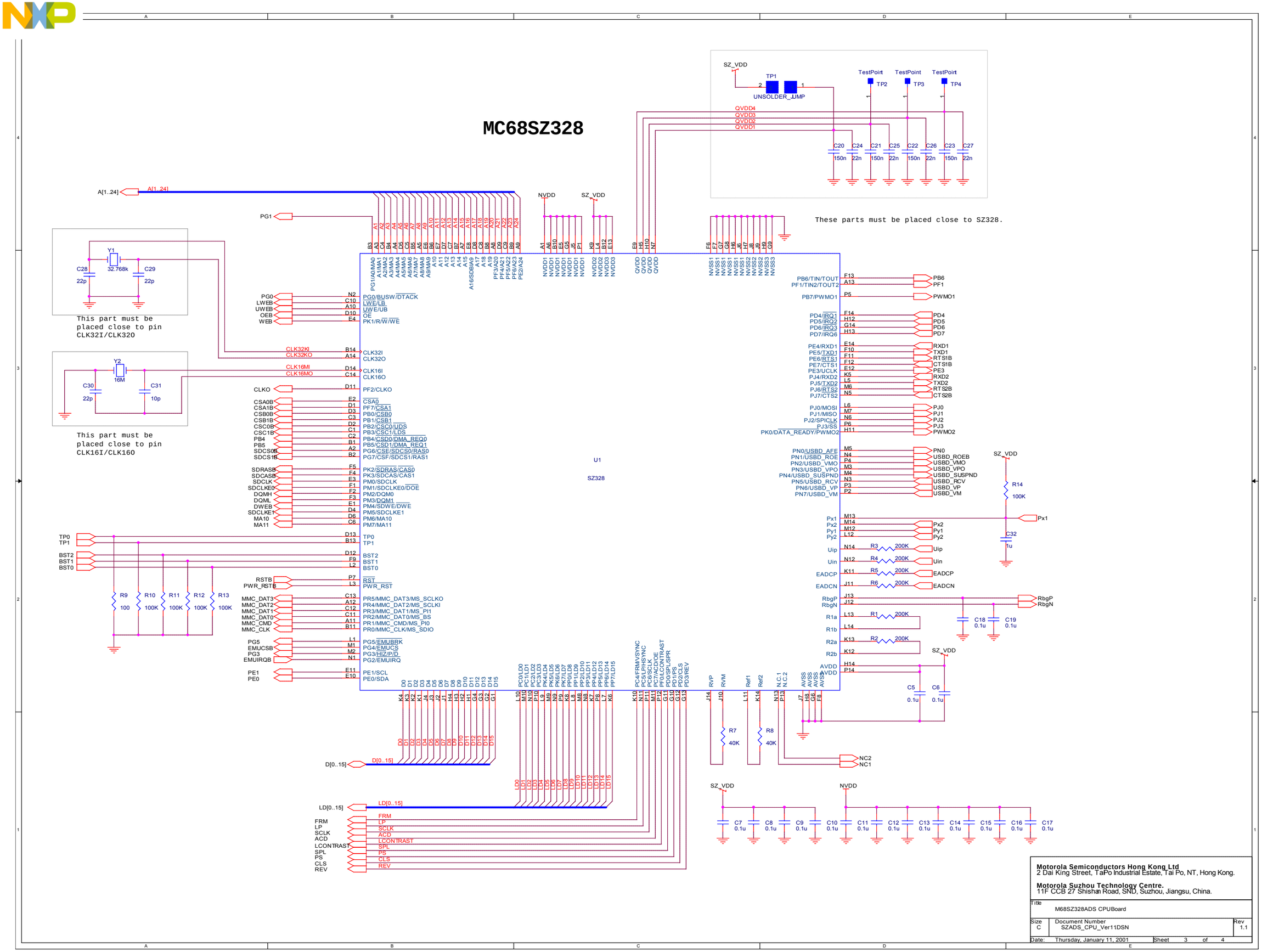
Title: M68SZ328ADS CPU Board		
Size: A	Document Number: SZADS_CPU_Ver11.DSN	Rev: 1.1
Date: Thursday, January 11, 2001	Sheet 2 of 4	



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Motorola Suzhou Technology Centre.
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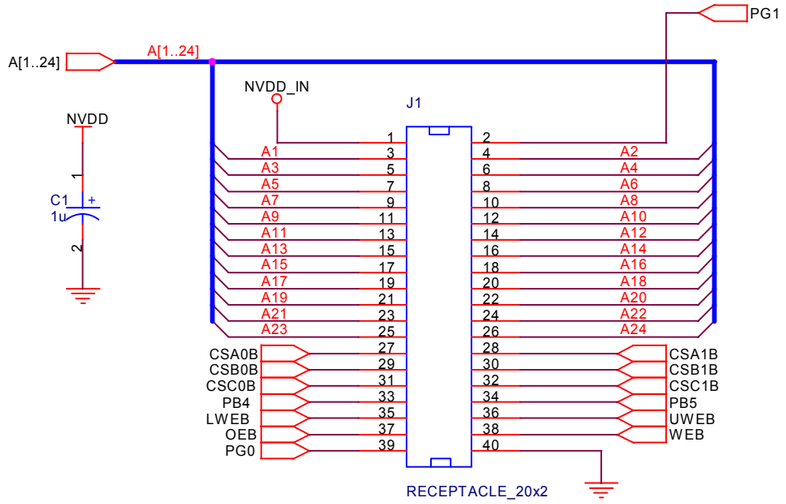
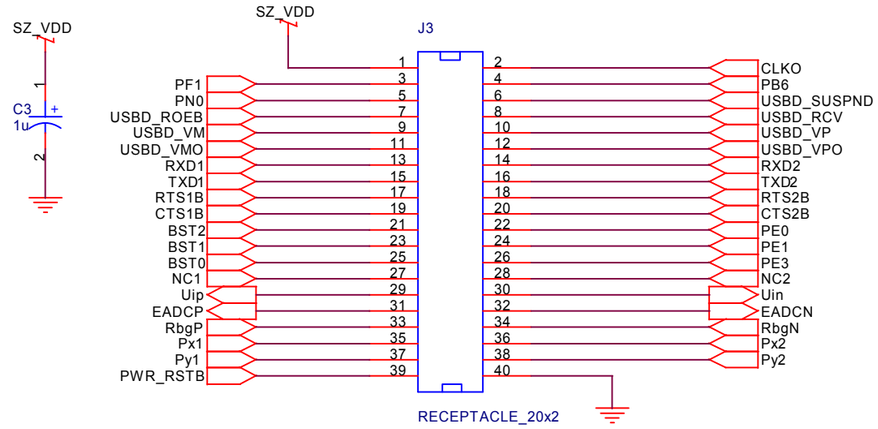
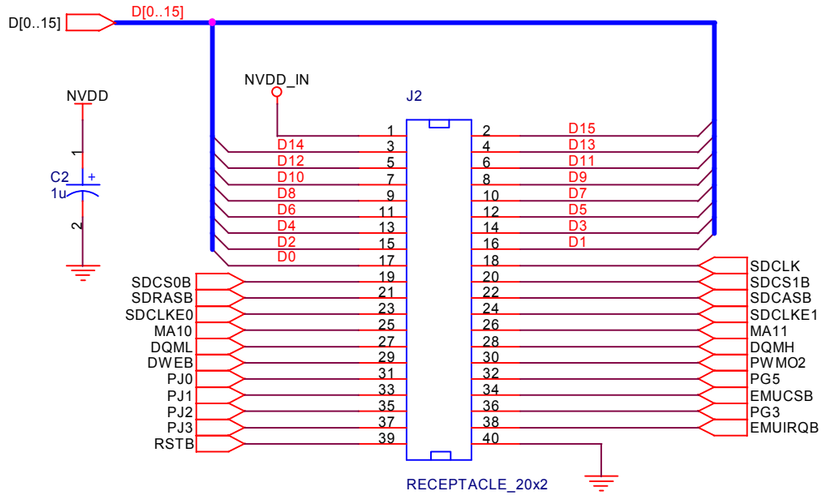
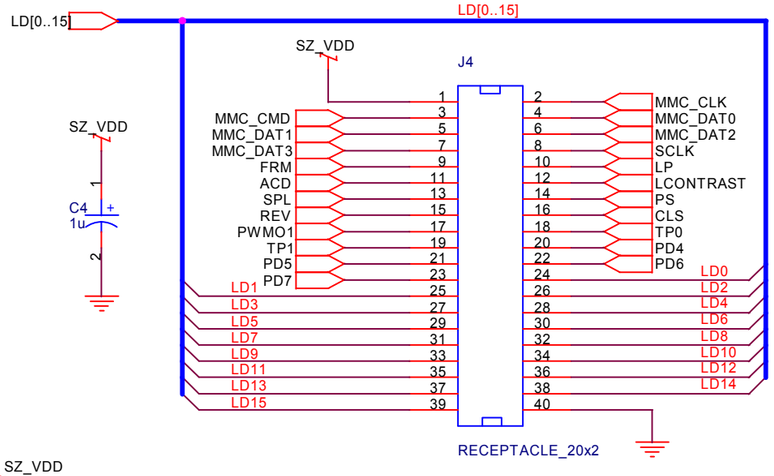
Title	M68SZ328ADS CPUBoard	
Size C	Document Number SZADS_CPU_Ver11DSN	Rev 1.1
Date: Thursday, January 11, 2001	Sheet 3 of 4	

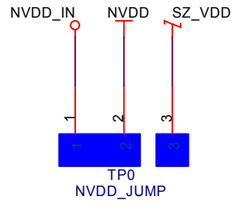
Extension Sockets











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Title: M68SZ328ADS CPU Board		
Size: B	Document Number: SZADS_CPU_Ver11.DSN	Rev: 1.1
Date: Thursday, January 11, 2001	Sheet 4 of 4	

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Motorola Semiconductors Suzhou Design Centre.

11F CCB 27 Shishan Road, SND, Suzhou, Jiangsu, China.

Product Name: **M68SZ328ADS Peripheral Board**

Version: 1.1

File Name: SZADS_Peripheral_Ver11.DSN
Designer: Shark Wu
Last Updated: Sep 28, 2001

Motorola Semiconductors Hong Kong Ltd
2 Dai King Street,Tai Po Industrial Estate, Tai Po, NT, Hong Kong.

Motorola Suzhou Technology Centre.
11F CCB 27 Shishan Road, SND, Suzhou, Jiangsu, China.

Title	M68SZ328ADS Peripheral Board	
Size: A	Document Number: SZADS_Peripheral_Ver11.DSN	Rev: 1.1
Date: Thursday, January 11, 2001	Sheet 1 of 11	

Revision History:

Version 1.0: Released for M68SZ328ADS peripheral board Ver1.0 PCB.

Version 1.1: Fix the errors of Ver10: changed the resistor value of power-reset from 10K to 510K, three pull-up resistors were added for the MONSELx, ASP assignment for touch panel was fixed.

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Title	M68SZ328ADS Peripheral Board	
Size: A	Document Number: SZADS_Peripheral_Ver11.DSN	Rev: 1.1
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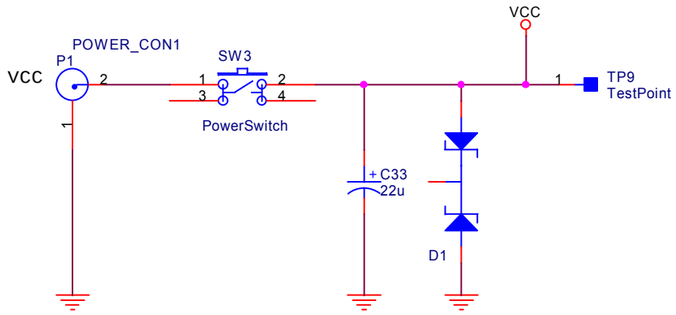
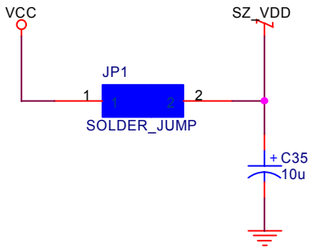
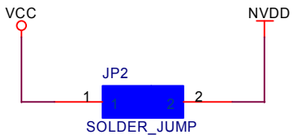
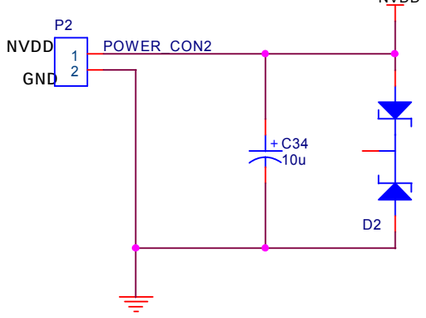
POWER CIRCUIT

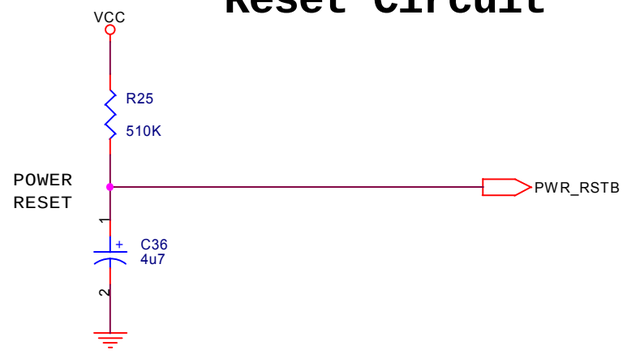


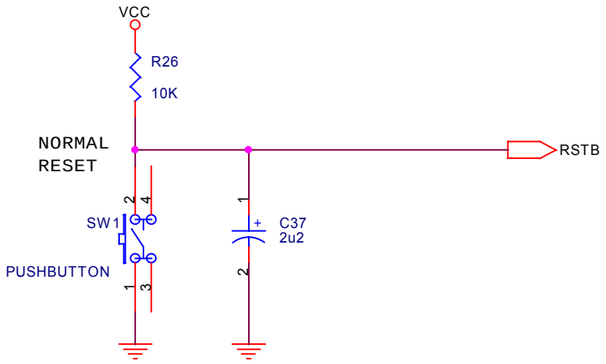


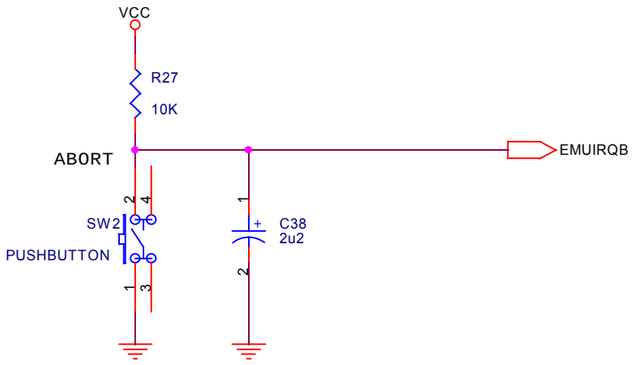




Reset Circuit







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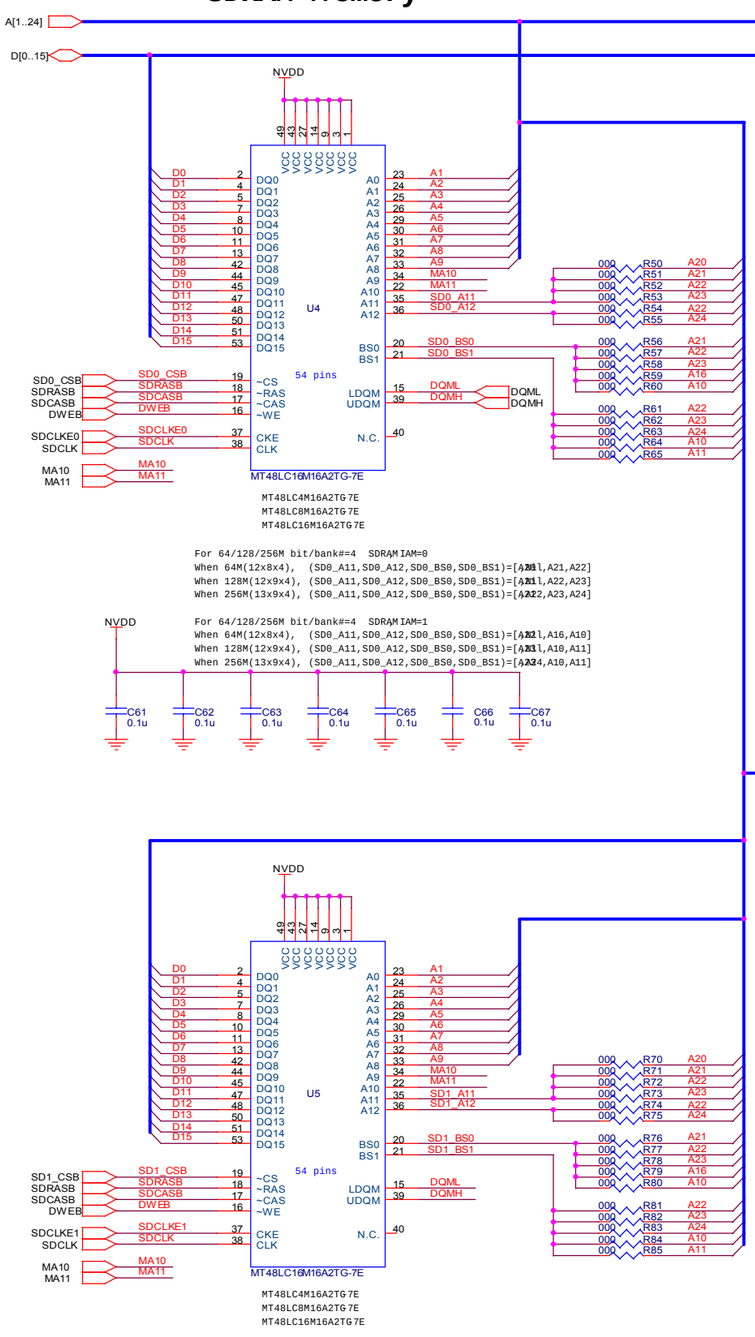
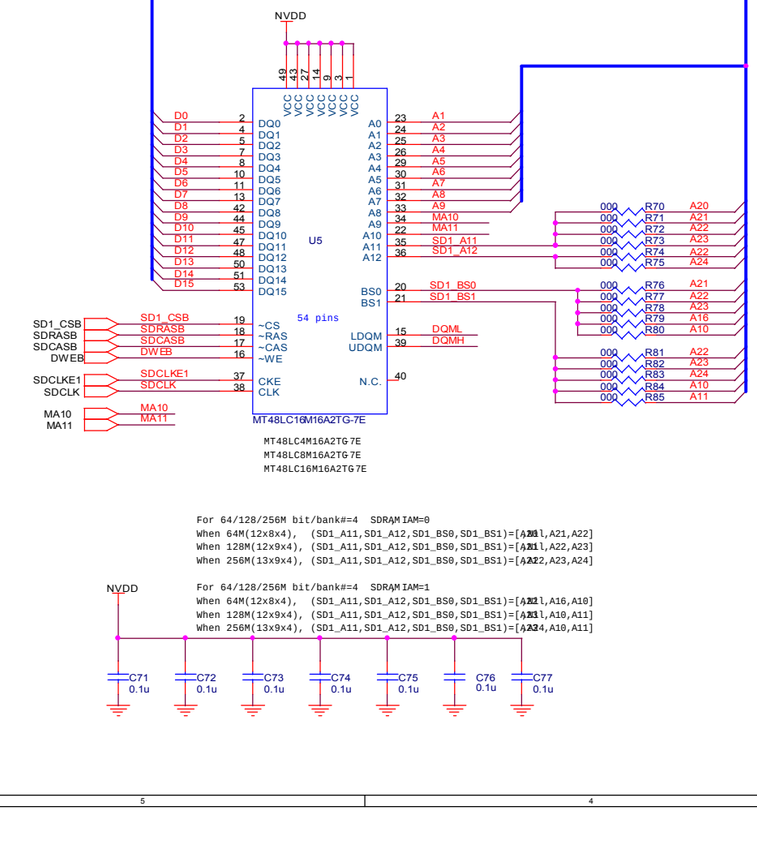
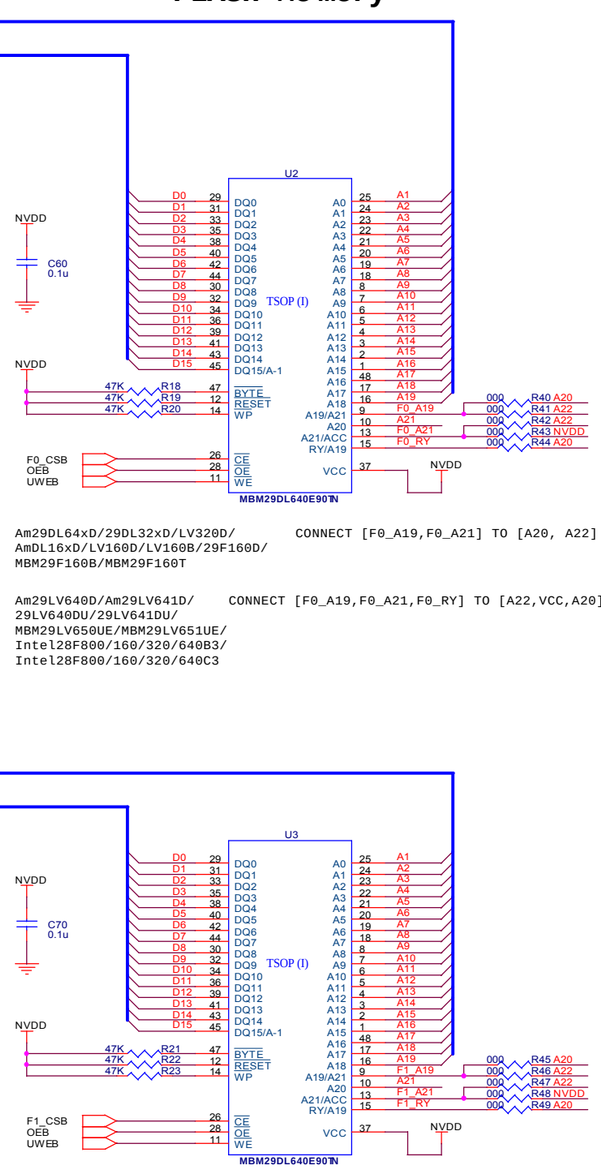
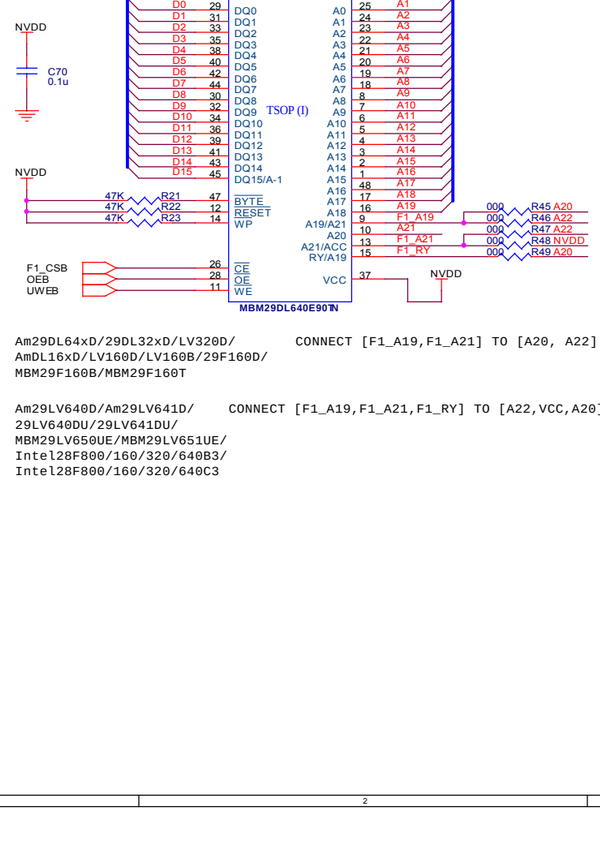
SDRAM Memory





FLASH Memory





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Size C	Document Number SZADS_Peripheral_Ver11.DSN		Rev 1.1
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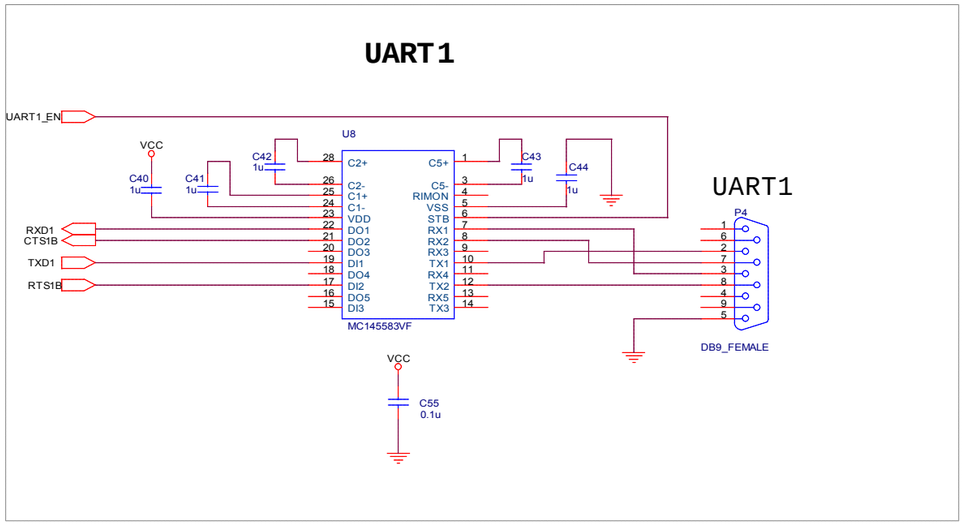
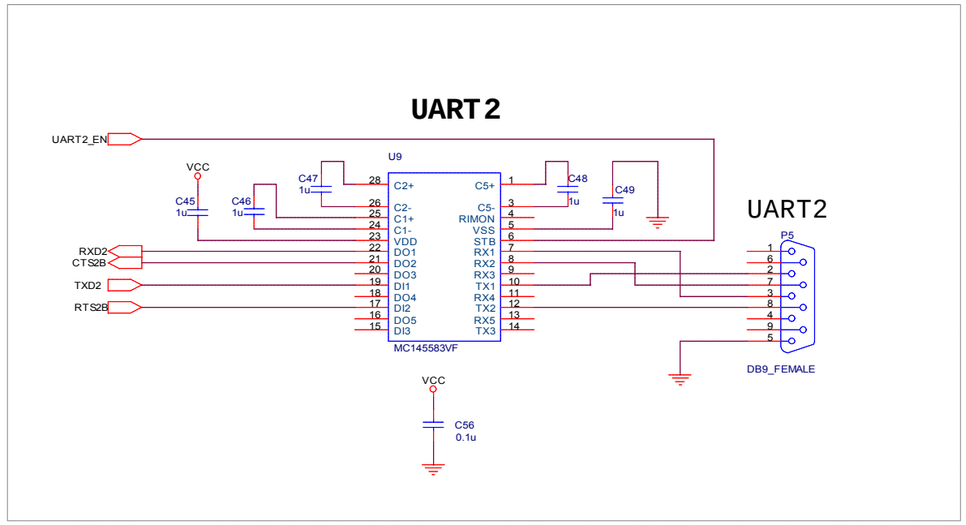
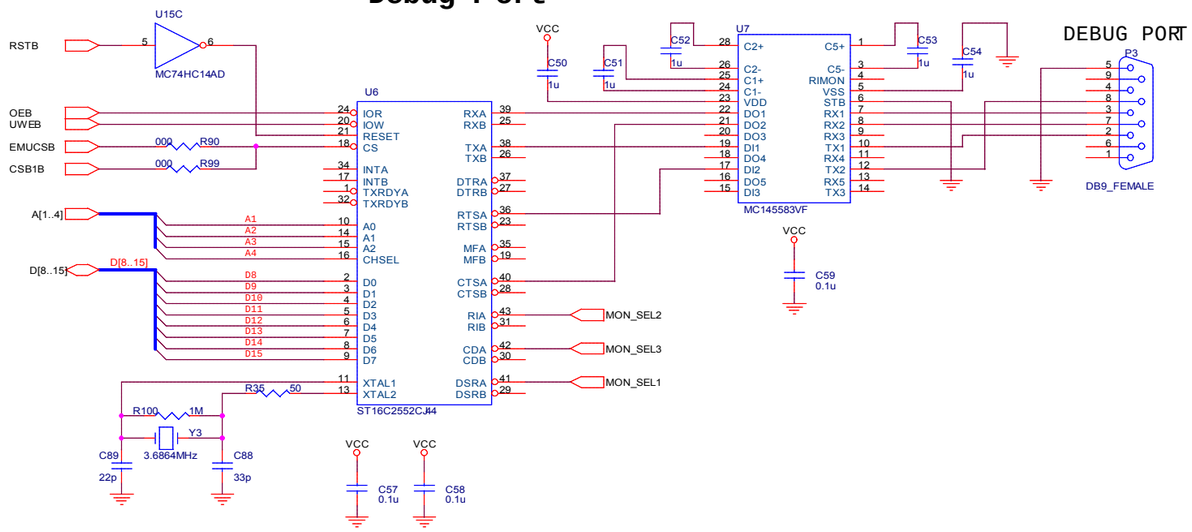
UART1



UART2

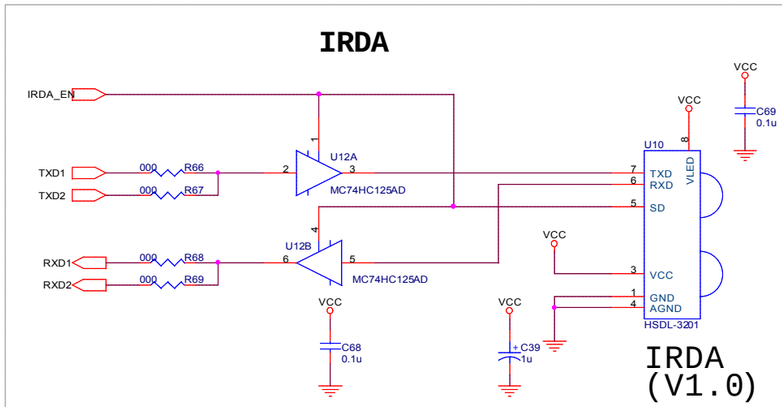


Debug Port



PIN#	SIGNAL
2	TXD
3	RXD
7	CTS
8	RTS
5	GND

IRDA



1uf Cap should be placedbetween HSDL-3201 VCC andGND.

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Title	M68SZ328ADS Peripheral Board	
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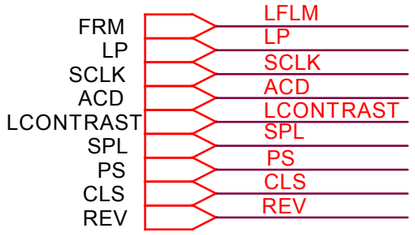
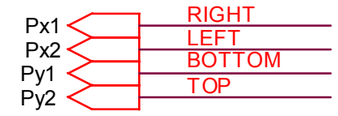
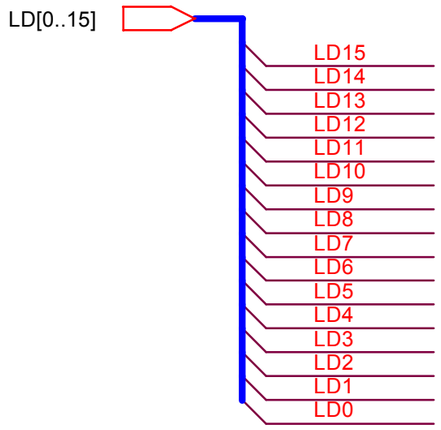
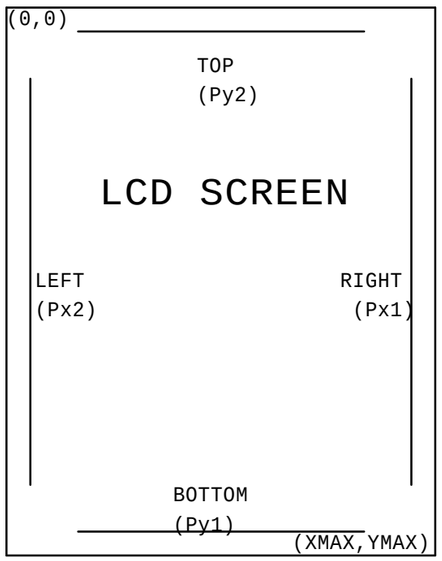
Touch Panel & LCD

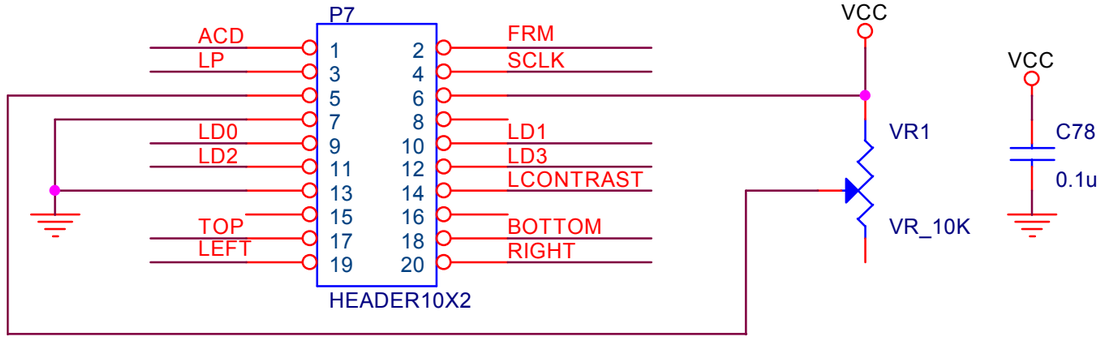




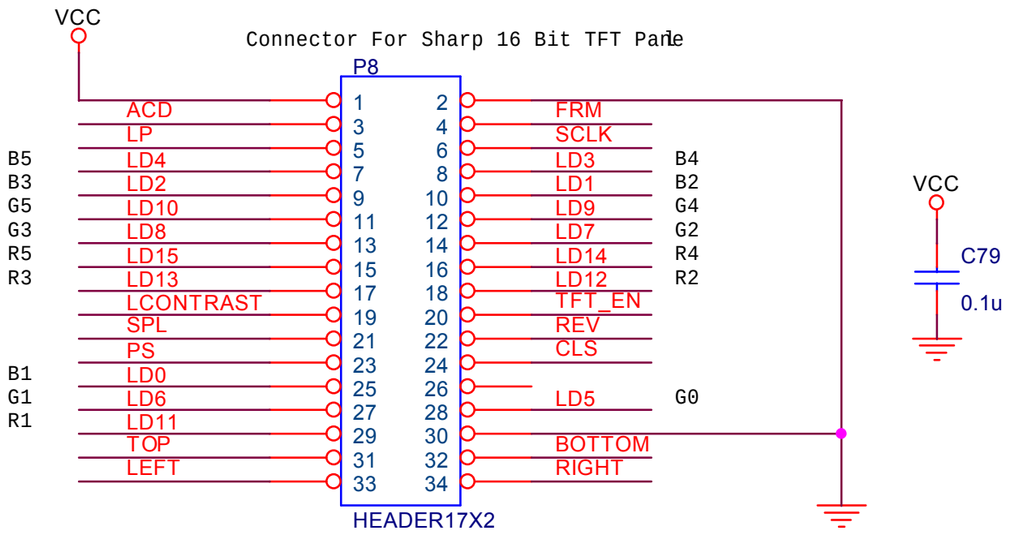




Connector for 4-Bit LCD



Connector For Sharp 16 Bit TFT Panle



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Title	M68SZ328ADS Peripheral Board	
Size A	Document Number SZADS_Peripheral_Ver11.DSN	Rev 1.1
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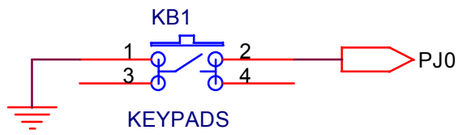
Keypads

KEYPAD1



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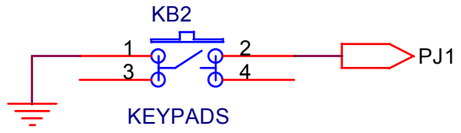

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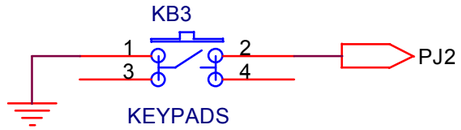

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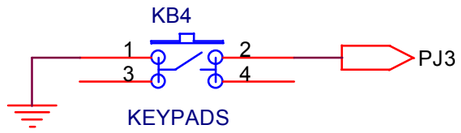

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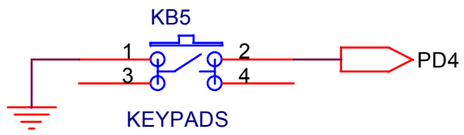

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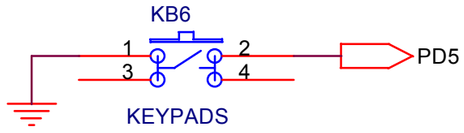
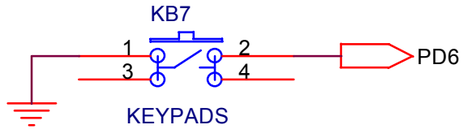


KEYPAD7



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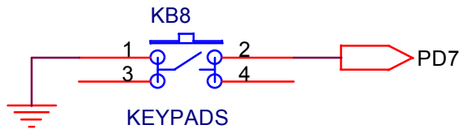

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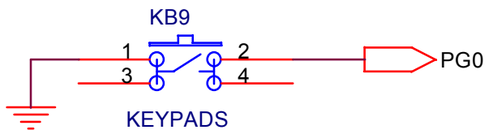

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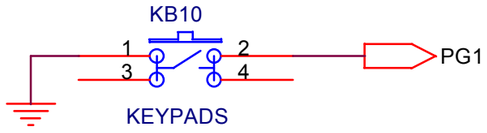

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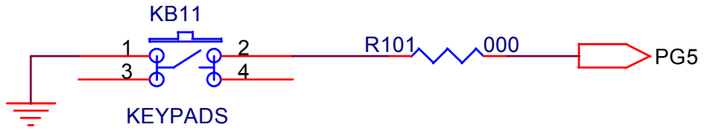

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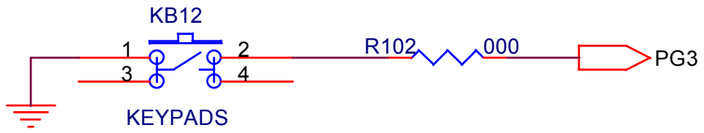

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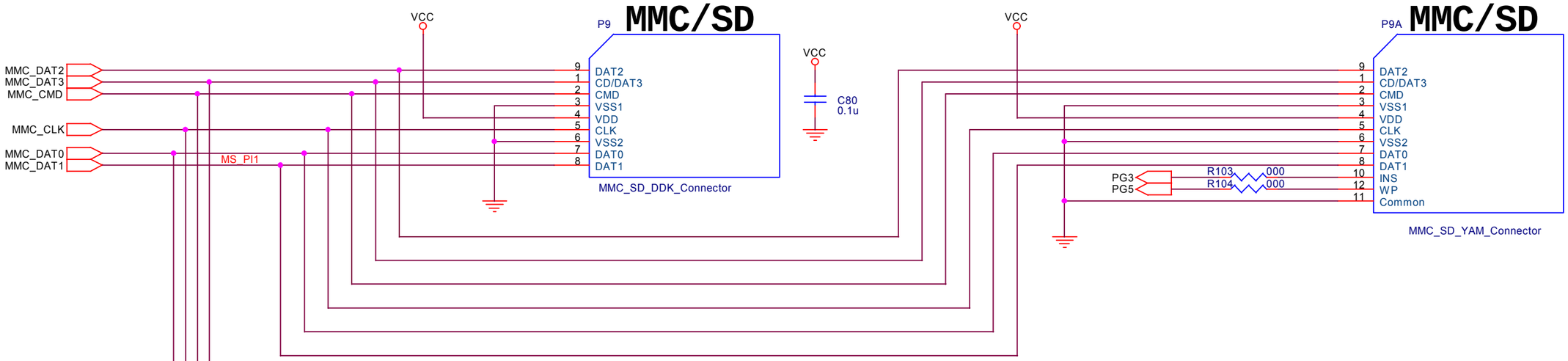
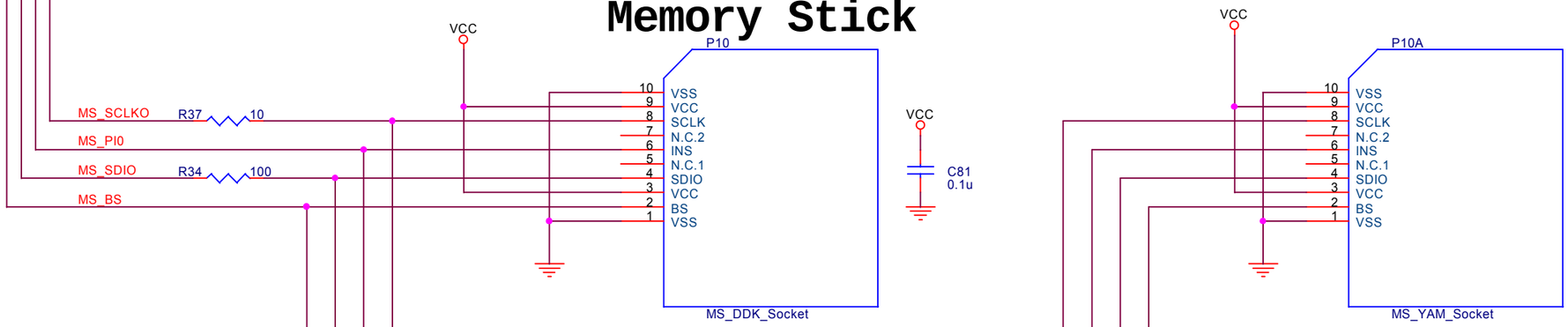
Memory Card Sockets



Memory Stick



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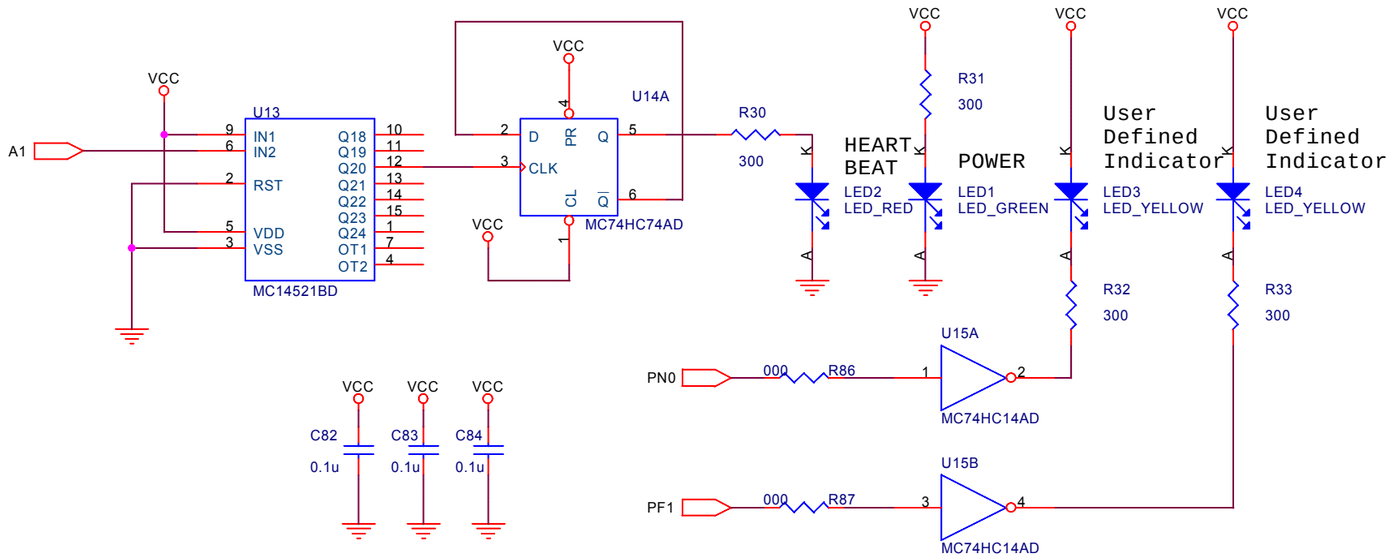
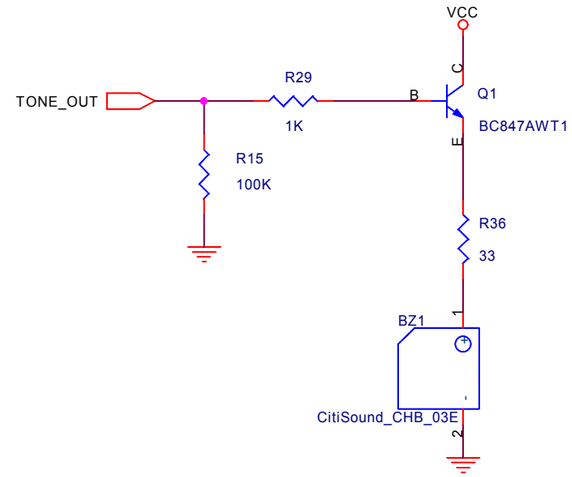
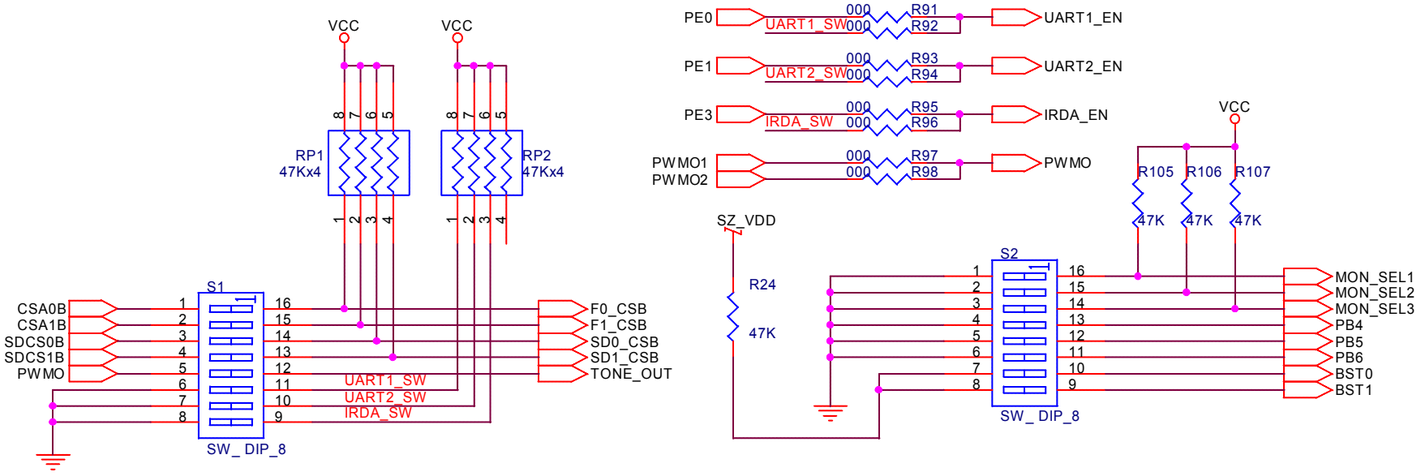
LED Indicators



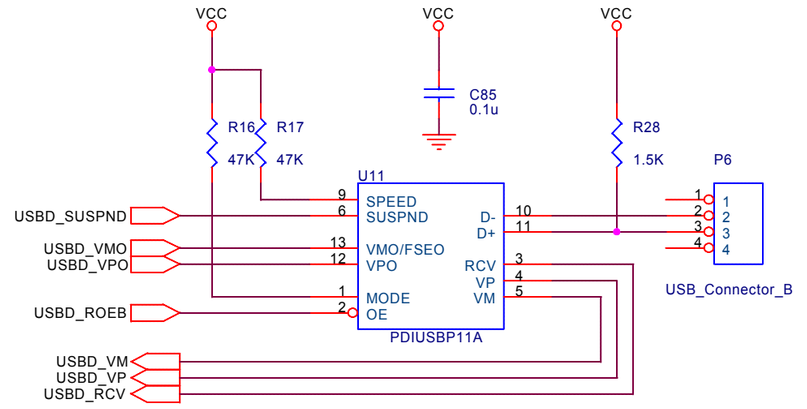
Single Tone Generato r



DIP Switches



USBD Port



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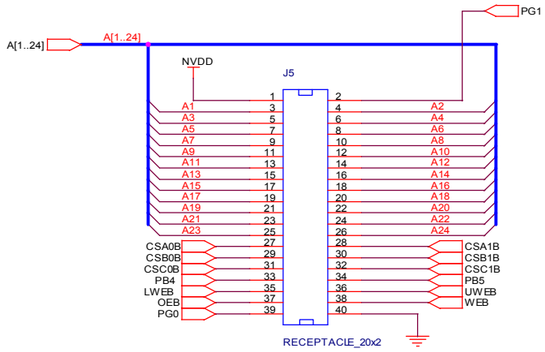
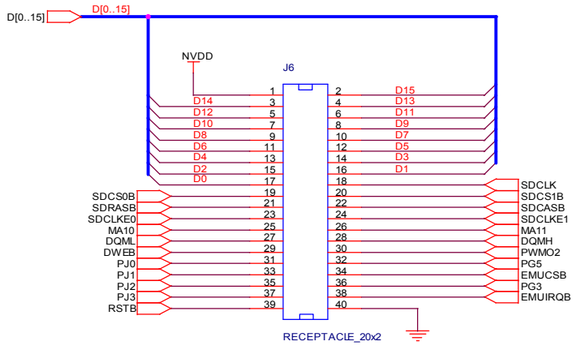
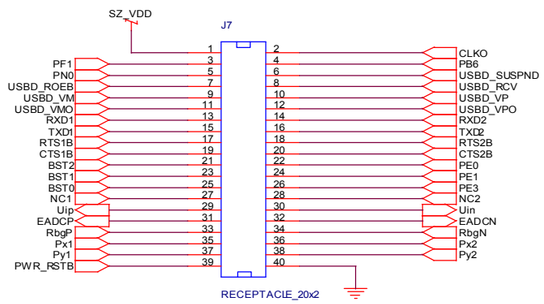
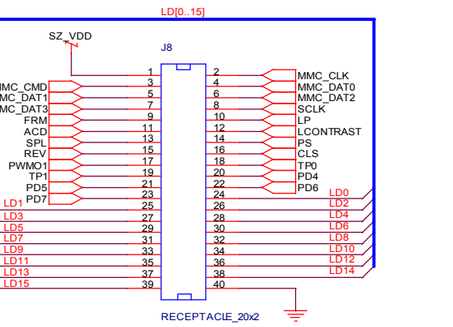
Extension Sockets

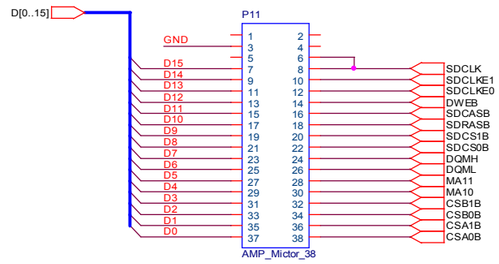


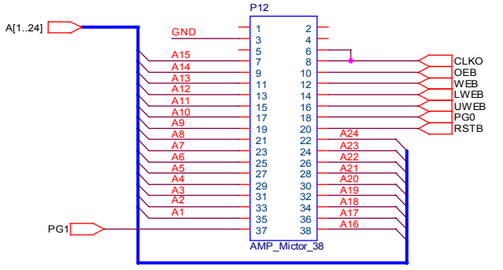


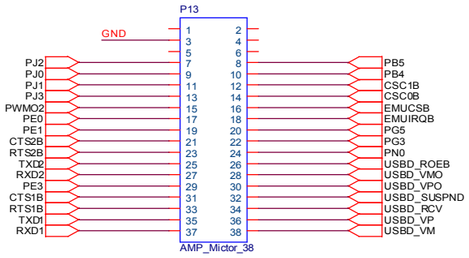


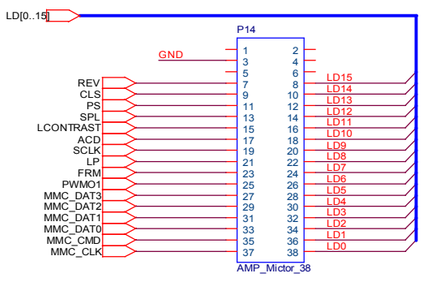


LA Connectors

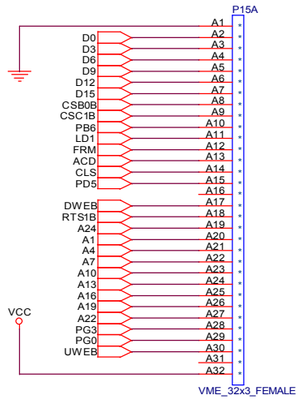


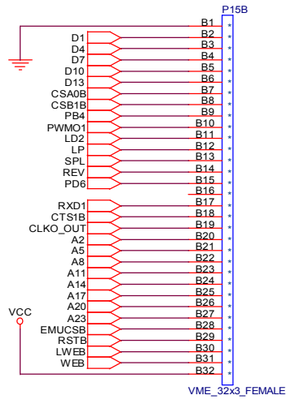


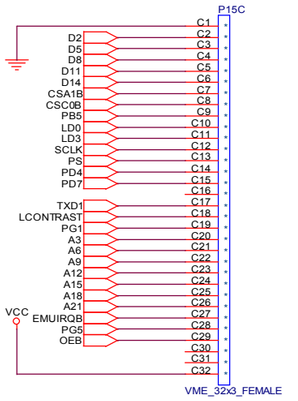


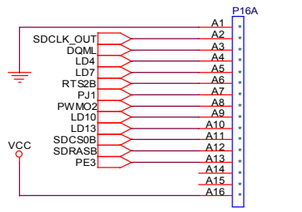


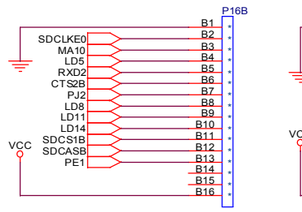
VME Connectors

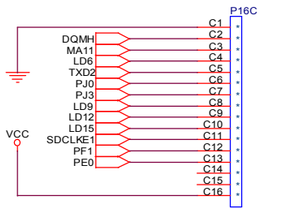


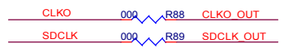












These two resistors must be placed near LA connectors.

In all 196 pins of SZ328, besides 32 power pins and ground pins , CLK32I/CLK32O/CLK16I/CLK16O/Ref1/Ref2/RV/RVM/R1a/R1b/R2a/R2b are not connected to extension connectors.

In all 152 pins of SZ328 extension sockets, besides all 12 analogous signals, PWR_RSTB/TP0/TP1/BST0/BST1/BST2/PF1/PB6/PD4/PD5/PD6/PD7 are not connected to LA connectors.

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Pin Assignments for VME Connector P15

PIN#	A	B	C
1	GND	GND	GND
2	D0	D1	D2
3	D3	D4	D5
4	D6	D7	D8
5	D9	D10	D11
6	D12	D13	D14
7	D15	CSA0B	PF1/CSA1B
8	PB0/CSB0B	PB1/CSB1B (SDWEB)	PB2/CSC0B (SDRASB)
9	PB3/CSC1B (SDCASB)	PB4/CSD0B (CSD0B)	PB5/CSD1B (CSD1B)
10	PB6/TIN1/TOUT1 (TIN_TOUT)	PB7/PWM01 (PWM0)	PC0/LD0
11	PC1/LD1	PC2/LD2	PC3/LD3
12	PC4/FRM/VSYNC	PC5/LP/HSYNC	PC6/SCLK
13	PC7/ACD/OE	PD0/SPL/SPR (INT0B)	PD1/PS (INT1B)
14	PD2/CLS (INT2B)	PD3/REV (INT3B)	PD4/IRQ1B
15	PD5/IRQ2B	PD6/IRQ3B	PD7/IRQ6B
16	(SPMTXD)	(SPMRXD)	(SPMCLK)
17	PM4/SDWEB/DWEB (DWEB)	PE4/RXD1	PE5/TXD1
18	PE6/RTS1B	PE7/CTS1B	PF0/LCONTRAST
19	PE2/A24 (IRQ5B)	PF2/CLKO	PG1/A0/MA0
20	A1/MA1	A2/MA2	A3/MA3
21	A4/MA4	A5/MA5	A6/MA6
22	A7/MA7	A8/MA8	A9/MA9
23	A10	A11	A12
24	A13	A14	A15
25	A16/SDBIA9	A17	A18
26	A19	PF3/A20	PF4/A21
27	PF5/A22	PF6/A23	PG2/EMUIRQB
28	PG3/P_DB	PG4/EMUCSB	PG5/EMUBRKB
29	PG0/BUSW/DTACKB	RSTB	OEB
30	UWEB/UB	LWEB/LB	(LDSB)
31	(UDSB)	PK1/R/WB/WEB	
32	VCC	VCC	VCC

Pin Assignments for VME Connector P16

PIN#	A	B	C
1	GND	GND	GND
2	PM0/SDCLK	PM1/SDCLKE0/DOEB (SDCE)	PM2/DQM0
3	PM3/DQM1	PM6/MA10 (SDA10)	PM7/MA11 (DM0EB)
4	PK4/LD4	PK5/LD5	PK6/LD6
5	PK7/LD7	PJ4/RXD2	PJ5/TXD2
6	PJ6/RTS2B	PJ7/CTS2B	PJ0/MOSI
7	PJ1/MISO	PJ2/SPICLK	PJ3/SSB
8	PK0/DATA_READYB/PWM02 (N.C.)	PP0/LD8 (N.C.)	PP1/LD9 (N.C.)
9	PP2/LD10 (N.C.)	PP3/LD11 (N.C.)	PP4/LD12 (N.C.)
10	PP5/LD13 (N.C.)	PP6/LD14 (N.C.)	PP7/LD15 (N.C.)
11	PG6/CSE/SDCS0B/RAS0B (N.C.)	PG7/CSF/SDCS1B/RAS1B (N.C.)	PM5/SDCLKE1 (N.C.)
12	PK2/SDRASB/CAS0B (N.C.)	PK3/SDCASB/CAS1B (N.C.)	PF1/TIN2/TOUT2 (N.C.)
13	PE3/UCLK (N.C.)	PE1/SCL (N.C.)	PE0/SDA (N.C.)
14			
15			
16	VCC	VCC	VCC

1. Text included in "()" are the signal names of M68VZ328ADS which is different from M68SZ328ADS.

2. Although some signals of SZADS look similar to VZADS, they have different usage.
    a. MA10 is different from SDA10, MA10 is usually coonected to SDRAM(x16bits) A9, while SDA10 is usually connected to A10.
    b. CSD0B/CSD1B of VZADS can be used as chip-select SDRAM or RAS of EDO DRAM, while CSD0B/CSD1B of SZADS can't.

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APPENDIX E
DIFFERENCE BETWEEN SZADS VER1.0 AND VER1.1

E.1 OVERVIEW

The section below will describe the difference between the Super VZ ADS board Version 1.0 and Version 1.1

E.2 DIFFERENCE BETWEEN TWO VERSIONS

There are 4 main differences between SZADS Ver1.0 and SZADS Ver1.1:

1. PB4 of SZADS is used to select the 3.9/3.5 inch LCD panel in SZADS ver1.1, while reserved in ver1.0;

2. Signal arrangement of Sharp 16bit TFT LCD panel connector - P8 is now the same as that of LCD panel, while in the ver1.0, the sigal of touch panel is twist.

3. Monitor select/1/2/3 of S2 is pull up, while float in ver1.0.

4. Memory stick connector is replaced with a push-push type connector.

APPENDIX F
HOW TO USE BBUG WINDOWS VERSION

F.1 OVERVIEW

BBUG is an application used for programming the monitor or other debugging purpose. The past version is an 16-bit application running under the MS-DOS or Microsoft Windows 95/98/NT environment. For the Windows 2000 environment, it is recommended to use BBUG Windows Version.
The section below will show step by step how to use the BBUG windows version. The application file is included in the CD-ROM called ¡§ WBBUG.EXE.

F.2 PROCEDURES USING BBUG WINDOWS VERSION

1. Reset SZ ADS.

2. Select PC's COM1 or COM2, if feedback error, please check PC's COMx.

3. Select UART1 or UART2. If feedback error, please check the cable connecting between ADS UART1 or UART2 and PC's COMx. If there is no connecting problem , reset SZ ADS.

4. Select Baud rate 19200bps, 57600bps or 115200bps.

5. A) If Wbbug.exe, init.b, flash0.b and flash1.b files are in the same directory, use the Button "Lo init", "Lo flash0" and "Lo flash1".

   B) Also use the Button "Browser..." to select the file that you want to download, then use the Button "download" to download the file to ADS borad.

C) Memory Display section: you may write address and count area, then use the Button "Display" to display data.

D) Memory Modify section: you may write address area, then use the Button "Read" to read data from that address; Or you may write value area, then use the Button "Modify" to modify data in the address.

E) Program Execute section: the file that you download to ADS may execute, you may write address area, then use the Button "Go" to execute it.

6. Use the Button "Exit Bbugsz" to shutdown the program.