

# MCF52259 Reference Manual Errata

by: Microcontroller Solutions Group

This errata document describes corrections to the *MCF52259 Reference Manual*, order number MCF52259RM. For convenience, the addenda items are grouped by revision. Please check our website at <http://www.freescale.com> for the latest updates.

The current available version of the *MCF52259 Reference Manual* is Revision 4.

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# 1 Errata for Revision 4

Table 1. MCF52259 Reference Manual Rev. 4 Errata

Location	Description
<p>Chapter "Clock Module"/Section "Block Diagram"/Figure "Clock Module Block Diagram"</p>	<p>Updated "Clock Module Block Diagram".below.                      The figure in Rev. 4 shows that FlexCAN clock is sourced by the system clock (<math>f_{sys}</math>) or by EXTAL. Also, it incorrectly showed that the USB module can be sourced by EXTAL.                      This figure needs to be improved as given below.</p> <p>The diagram illustrates the clock module architecture. It starts with three external oscillators: a kHz oscillator (RTC_EXTAL), a MHz oscillator (RTC_XTAL), and an ON-CHIP 8 MHz oscillator (BWT_Clk1). These are selected by the OSCSEL1 multiplexer. The selected clock passes through a Pre-Divider (CCHR) to become the Reference Clock (Ref Clock). This Ref Clock is then processed by a PLL (Phase-Locked Loop) and a Low Power Divider (LPD[3:0]). The PLL output is selected by the OSCSEL0 multiplexer. The Low Power Divider output is selected by the CLKSRC multiplexer. The resulting System Clock (<math>f_{sys}</math>) is divided by 2 and distributed to various modules. The distribution is controlled by PPMRL (Peripheral Prescaler Multiplier Register Low) and PPMRH (Peripheral Prescaler Multiplier Register High) registers. Modules include ColdFire V2, BDM, USB, FlexCAN, DMA, UARTs, FEC, Mini-FlexBus, WDOG, Interrupt Controllers, DMA Timers, QSPI, I<sup>2</sup>Cs, DMA, UARTs, DMA, FEC, Mini-FlexBus, WDOG, CFM, PWM, GPT, ADC, PITs, Edge Port, GPIO/Ports, RTC, and BWT.</p>

**Table 1. MCF52259 Reference Manual Rev. 4 Errata (continued)**

Location	Description
Chapter "Universal Serial Bus, OTG Capable Controller" / Section "USB Control Register (USB_CTRL)" / Table "USB_CTRL field descriptions"	In Table "USB_CTRL field descriptions", in field "1-0 CLK_SRC", the clock source is incorrectly described as follows: 00 USB_ALT_CLK pin (External clock that can feed in from PTG0) 01 External OSC on EXTAL pin 10 Reserved 11 System clock source (MCGPLLCLK) It should be as follows: 00 USB_ALT_CLK pin (External clock that can feed in from PTG0) 01 PLL Bypass Clock 10 Reserved 11 System clock source ( $f_{sys}$ )
Chapter "FlexCAN" / Section "FlexCAN Control Register (CANCTRL)" / Table "CANCTRL field descriptions" / Equation 32-1	In Equation 32-1, the S clock frequency equation is incorrectly shown as $S \text{ clock frequency} = \frac{f_{sys} \text{ or EXTAL}}{PRESDIV + 1}$ It should be as follows: $S \text{ clock frequency} = \frac{f_{sys}/2 \text{ or PLL bypass clock}}{PRESDIV + 1}$
Chapter "FlexCAN" / Section "FlexCAN Control Register (CANCTRL)" / Table "CANCTRL field descriptions"	In Table "CANCTRL field descriptions", bit 13 "CLK_SRC", the clock source is incorrectly described as 0 Clock source is EXTAL 1 Clock source is the internal bus clock, $f_{sys}$ It should be as follows: 0 Clock source is PLL bypass clock 1 Clock source is the internal bus clock, $f_{sys}/2$
Chapter "FlexCAN" / Section "FlexCAN Control Register (CANCTRL)" / Figure "CAN engine clocking scheme"	In Figure "CAN engine clocking scheme" "Oscillator Clock (EXTAL)" needs to be changed to PLL bypass clock In Equation 32-6, a. $f_{sys}$ needs to be changed to $f_{sys}/2$ b. "EXTAL" needs to be changed to PLL bypass clock

## 2 Revision History

Table 2 provides a revision history for this document.

**Table 2. Revision History Table**

Rev. Number	Substantive Changes	Date of Release
1.0	Initial release. Incorporated changes in the following chapters: <ul style="list-style-type: none"> <li>• Clock Module</li> <li>• Universal Serial Bus, OTG Capable Controller</li> <li>• FlexCAN</li> </ul>	12/2011

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