This errata document describes corrections to the *MCF52259 Reference Manual*, order number MCF52259RM. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com for the latest updates.

The current available version of the *MCF52259 Reference Manual* is Revision 4.
Errata for Revision 4

1 Errata for Revision 4

Table 1. MCF52259 Reference Manual Rev. 4 Errata

<table>
<thead>
<tr>
<th>Location</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chapter “Clock Module”/Section “Block Diagram”/Figure “Clock Module Block Diagram”</td>
<td>Updated “Clock Module Block Diagram”. The figure in Rev. 4 shows that FlexCAN clock is sourced by the system clock (f_sys) or by EXTAL. Also, it incorrectly showed that the USB module can be sourced by EXTAL. This figure needs to be improved as given below.</td>
</tr>
</tbody>
</table>

![Clock Module Block Diagram](image)

ADC auto-standby Clk

System Clock (f_sys)
Table 2 provides a revision history for this document.

Table 2. Revision History Table

<table>
<thead>
<tr>
<th>Rev. Number</th>
<th>Substantive Changes</th>
<th>Date of Release</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>Initial release. Incorporated changes in the following chapters:</td>
<td>12/2011</td>
</tr>
<tr>
<td></td>
<td>• Clock Module</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Universal Serial Bus, OTG Capable Controller</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• FlexCAN</td>
<td></td>
</tr>
<tr>
<td></td>
<td>In Figure “CAN engine clocking scheme” “Oscillator Clock (EXTAL)” needs to be changed to PLL bypass clock</td>
<td></td>
</tr>
<tr>
<td></td>
<td>In Equation 32-6,</td>
<td></td>
</tr>
<tr>
<td></td>
<td>a. fsys needs to be changed to fsys/2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>b. “EXTAL” needs to be changed to PLL bypass clock</td>
<td></td>
</tr>
</tbody>
</table>

Chapter “Universal Serial Bus, OTG Capable Controller”/Section “USB Control Register (USB_CTRL)”/Table “USB_CTRL field descriptions” In Table “USB_CTRL field descriptions”, in field “1-0 CLK_SRC”, the clock source is incorrectly described as follows:
00 USB_ALT_CLK pin (External clock that can feed in from PTG0)
01 External OSC on EXTAL pin
10 Reserved
11 System clock source (MCGPLLCLK)

It should be as follows:
00 USB_ALT_CLK pin (External clock that can feed in from PTG0)
01 PLL Bypass Clock
10 Reserved
11 System clock source (fsys)

Chapter “FlexCAN”/Section “FlexCAN Control Register (CANCTRL)”/Table “CANCTRL field descriptions”/Equation 32-1
In Equation 32-1, the S clock frequency equation is incorrectly shown as
\[
\text{S clock frequency} = \frac{f_{\text{sys}} \text{ or EXTAL}}{\text{PRESDIV} + 1}
\]

It should be as follows:
\[
\text{S clock frequency} = \frac{f_{\text{sys/2}} \text{ or PLL bypass clock}}{\text{PRESDIV} + 1}
\]

Chapter “FlexCAN”/Section “FlexCAN Control Register (CANCTRL)”/Figure “CAN engine clocking scheme”
In Figure “CAN engine clocking scheme” “Oscillator Clock (EXTAL)” needs to be changed to PLL bypass clock
In Equation 32-6,
  a. fsys needs to be changed to fsys/2
  b. “EXTAL” needs to be changed to PLL bypass clock